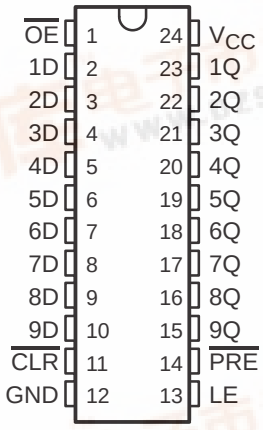
9-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

SCBS022C – FEBRUARY 1989 – REVISED NOVEMBER 1993

- **BiCMOS Process With CMOS Inputs and TTL Outputs Substantially Reduces Standby Current**
- **Input Has 50 kΩ**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (NT)**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN74BCT29843 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing wider buffer registers, I/O ports, bidirectional bus drivers with parity, and working registers.

The nine latches are transparent D-type latches. When the latch-enable (LE) input is high, the Q outputs are complementary to the noninverting data (D) inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the nine outputs in either a normal logic state (high or low level) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pull-up components.

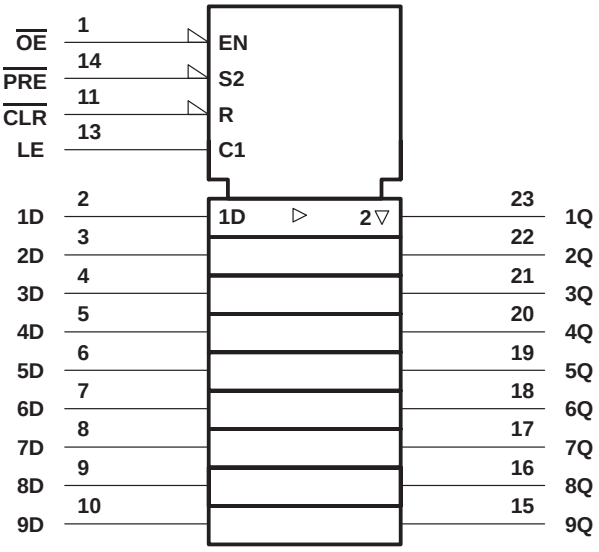
The output enable ($\overline{OE}$) does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74BCT29843 is characterized for operation from 0°C to 70°C.

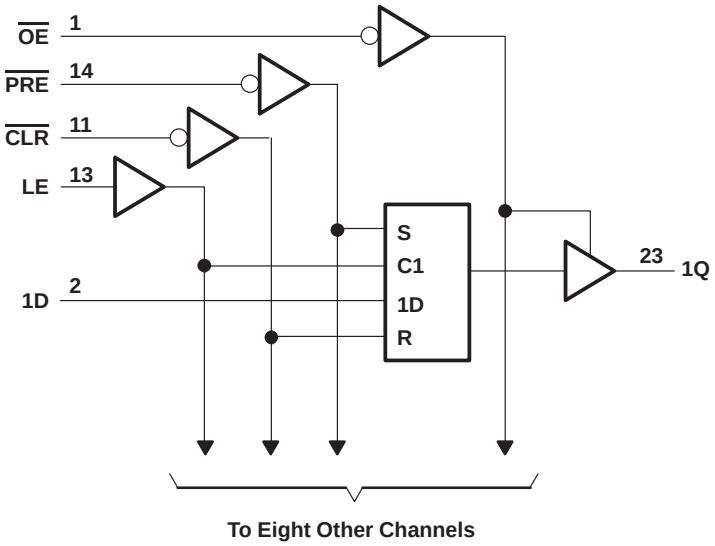
FUNCTION TABLE

INPUTS					OUTPUT
$\overline{PRE}$	$\overline{CLR}$	$\overline{OE}$	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q_0
X	X	H	X	X	Z

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . – 0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . – 0.5 V to 7 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . – 0.5 V to 7 V
Voltage range applied to any output in the high state, V_O . . . . . – 0.5 V to V_{CC}
Input clamp current, I_{IK} (V_I < 0) . . . . . –30 mA
Current into any output in the low state, I_O . . . . . 96 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . – 65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions beyond those indicated in the “recommended operating conditions” section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High-level output current			– 24	mA
I_{OL}	Low-level output current			48	mA
T_A	Operating free-air temperature	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2	V
V_{OH}	V_{CC} = 4.5 V	I_{OH} = –15 mA	2.4	3.2		V
		I_{OH} = –24 mA	2			
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 48 mA		0.35	0.55	V
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V	–10		–75	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.2	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0	–75		–275	mA
I_{CCL}	V_{CC} = 5.5 V,	Outputs open		24	35	mA
I_{CCH}	V_{CC} = 5.5 V,	Outputs open		3	7	mA
I_{CCZ}	V_{CC} = 5.5 V,	Outputs open		3	7	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			MIN	MAX	UNIT
t_w	Pulse duration	$\overline{PRE}$ low	7		ns
		$\overline{CLR}$ low	5		
		LE high	4		
t_{su}	Setup time, data before LE↓	High or low	1.5		ns
		$\overline{PRE}$ or $\overline{CLR}$ inactive	2		
t_h	Hold time, data after LE↓	High or low	3.5		ns

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	$\overline{D}$	Q	1.5	4.5	7	1.5	8	ns
t_{PHL}			1.5	5.7	8	1.5	9	
t_{PLH}	LE	Q	1.5	6	8	1.5	10	ns
t_{PHL}			1.5	6	8	1.5	10	
t_{PLH}	$\overline{PRE}$	Q	1.5	6	8	1.5	12	ns
t_{PHL}			1.5	6	10	1.5	12	
t_{PLH}	$\overline{CLR}$	Q	1.5	6	10	1.5	12	ns
t_{PHL}			1.5	6	10	1.5	12	
t_{PZH}	$\overline{OE}$	Q	2	10	13	2	15	ns
t_{PZL}			2	10	13	2	15	
t_{PHZ}	$\overline{OE}$	Q	2	5	7	2	8	ns
t_{PLZ}			2	5	7	2	8	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

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