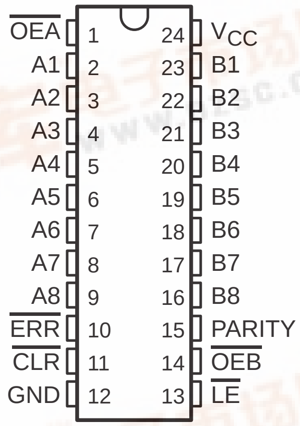
# SN74BCT29854
# 8-BIT TO 9-BIT PARITY BUS TRANSCEIVER

SCBS257 – SEPTEMBER 1987 – REVISED NOVEMBER 1993

- **BiCMOS Process With TTL Inputs and Outputs**
- **State-of-the-Art BiCMOS Design Significantly Reduces Standby Current**
- **Flow-Through Pinout (All Inputs on Opposite Side From Outputs)**
- **Functionally Equivalent to AMD Am29854**
- **High-Speed Bus Transceiver With Parity Generator/Checker**
- **Parity-Error Flag With Open-Collector Output**
- **Latch for Storage of the Parity-Error Flag**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (NT)**

**DW OR NT PACKAGE**
**(TOP VIEW)**



## description

The SN74BCT29854 is an 8-bit to 9-bit parity transceiver designed for asynchronous communication between data buses. When data is transmitted from the A to B bus, a parity bit is generated. When data is transmitted from the B to A bus with its corresponding parity bit, the parity-error ($\overline{\text{ERR}}$) output will indicate whether or not an error in the B data has occurred. The output-enable ($\overline{\text{OEA}}$, $\overline{\text{OEB}}$) inputs can be used to disable the device so that the buses are effectively isolated.

A 9-bit parity generator/checker generates a parity-odd (PARITY) output and monitors the parity of the I/O ports with an open-collector parity-error ($\overline{\text{ERR}}$) flag. $\overline{\text{ERR}}$ can be either passed, sampled, stored, or cleared from the latch using the latch-enable ($\overline{\text{LE}}$) and clear ($\overline{\text{CLR}}$) control inputs. When both $\overline{\text{OEA}}$ and $\overline{\text{OEB}}$ are low, data is transferred from the A bus to the B bus and inverted parity is generated. Inverted parity is a forced error condition which gives the designer more system diagnostic capability. The SN74BCT29854 provides inverting logic.

The SN74BCT29854 is characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**

| INPUTS | | | | | | OUTPUT AND I/O | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{\text{OEB}}$ | $\overline{\text{OEA}}$ | $\overline{\text{CLR}}$ | $\overline{\text{LE}}$ | Ai $\sum$ of H's | Bi[†] $\sum$ of L's | A | B | PARITY | $\overline{\text{ERR}}$[‡] | |
| L | H | X | X | Odd<br>Even | NA | NA | $\overline{\text{A}}$ | H<br>L | NA | $\overline{\text{A}}$ data to B bus and generate parity |
| H | L | X | L | NA | Odd<br>Even | $\overline{\text{B}}$ | NA | NA | H<br>L | $\overline{\text{B}}$ data to A bus and check parity |
| H | L | H | H | NA | X | X | NA | NA | N–1 | Store error flag |
| X | X | L | H | X | X | X | NA | NA | H | Clear error-flag register |
| H | H | H<br>L<br>X<br>X | H<br>H<br>L<br>L | X<br>X<br>L Odd<br>H Even | X | Z | Z | Z | NC<br>H<br>L<br>H | Isolation[§] |
| L | L | X | X | Odd<br>Even | NA | NA | $\overline{\text{A}}$ | L<br>H | NA | $\overline{\text{A}}$ data to B bus and generate inverted parity |

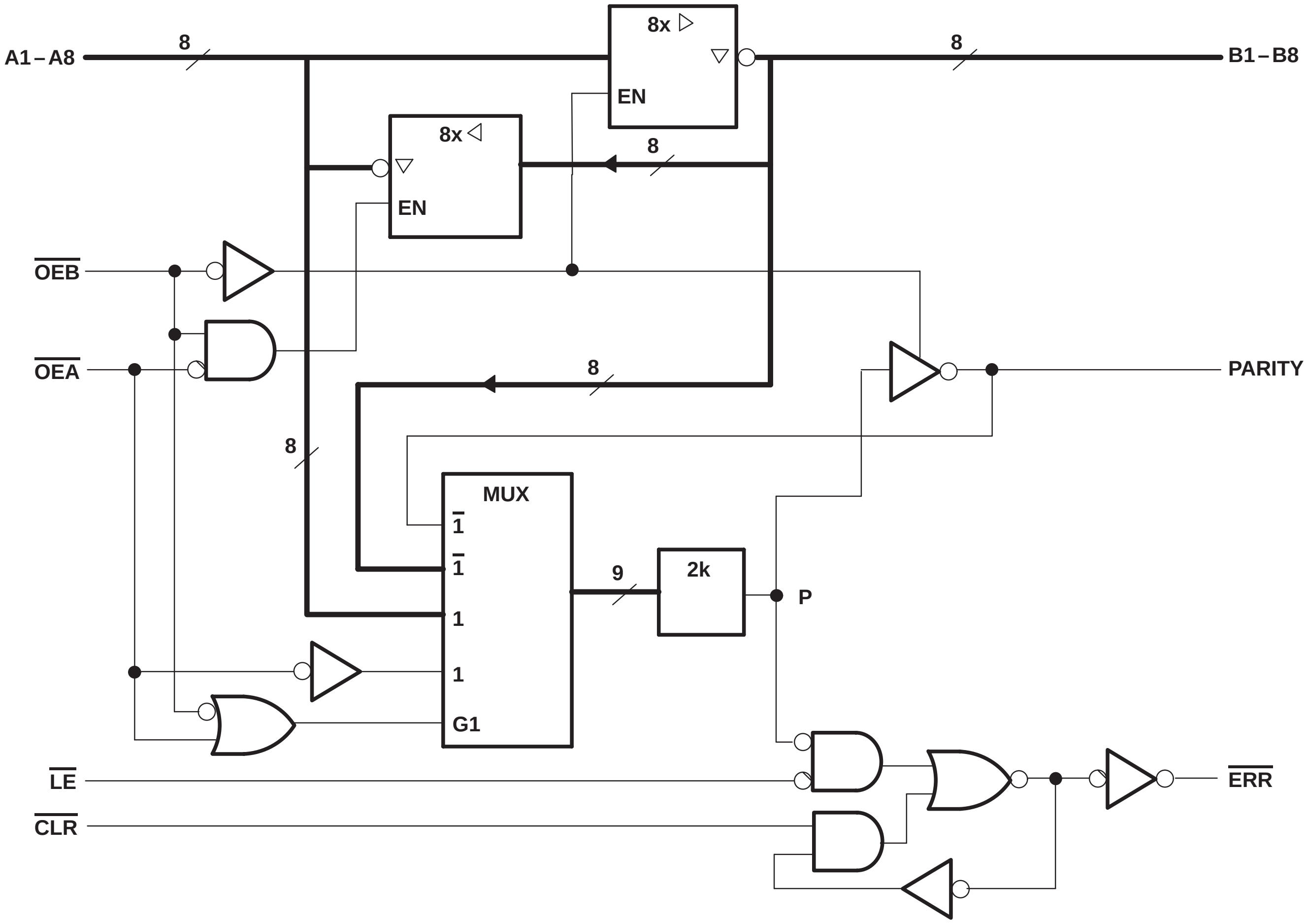
NA = not applicable, NC = no change, X = don't care

[†] Summation of low-level inputs includes PARITY along with Bi inputs.

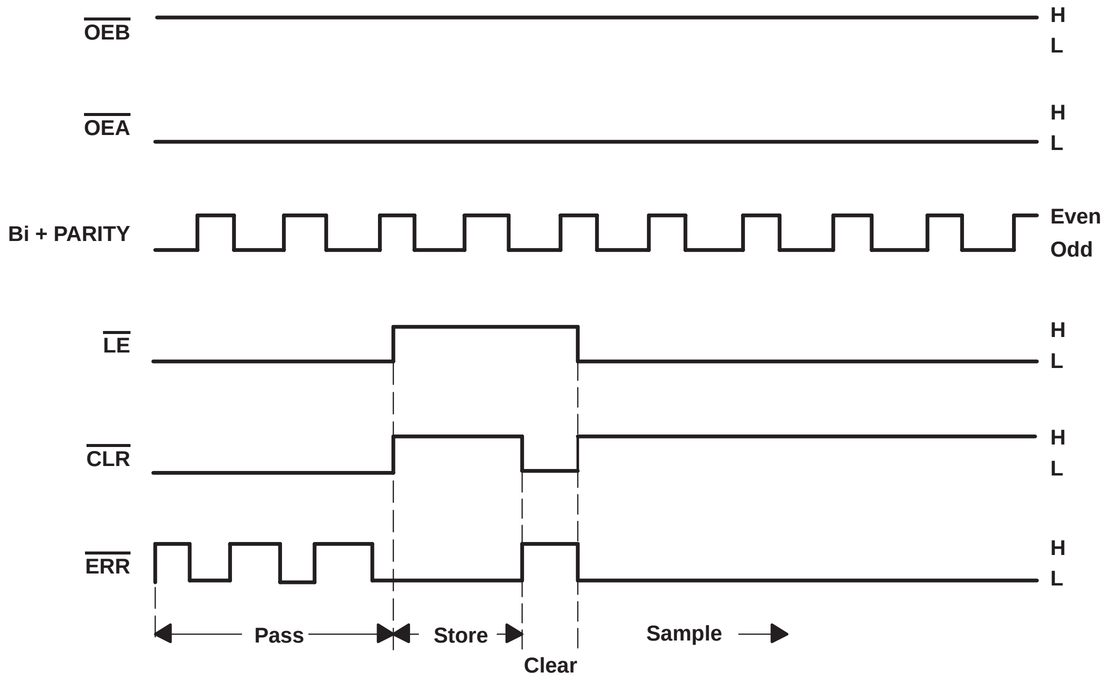
[‡] Output states shown assume the $\overline{\text{ERR}}$ output was previously high.

[§] In this mode, the $\overline{\text{ERR}}$ output, when enabled, shows noninverted parity of the A bus.

## logic diagram (positive logic)



## error-flag waveforms



**ERROR-FLAG FUNCTION TABLE**

| INPUTS | | INTERNAL TO DEVICE | OUTPUT PRESTATE | OUTPUT | FUNCTION |
|---|---|---|---|---|---|
| $\overline{LE}$ | $\overline{CLR}$ | POINT P | $\overline{ERR}_{n-1}$ † | $\overline{ERR}$ | |
| L | L | L<br>H | X | L<br>H | Pass |
| L | H | L<br>X<br>H | X<br>L<br>H | L<br>L<br>H | Sample |
| H | L | X | X | H | Clear |
| H | H | X | L<br>H | L<br>H | Store |

† $\overline{ERR}_{n-1}$ represents the state of the $\overline{ERR}$ output before any changes at $\overline{CLR}$, $\overline{LE}$, or point P.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|---|
| Supply voltage, $V_{CC}$ | 7 V |
| Input voltage, $V_I$ | 7 V |
| Voltage applied to a disabled I/O port | 5.5 V |
| Operating free-air temperature range | 0°C to 70°C |
| Storage temperature range | –65°C to 150°C |

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | V |
| $V_{OH}$ | High-level output voltage | $\overline{\text{ERR}}$ | | | 2.4 | V |
| $I_{OH}$ | High-level output current | | | | – 24 | mA |
| $I_{OL}$ | Low-level output current | | | | 48 | mA |
| $T_A$ | Operating free-air temperature | | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 4.5 V, | $I_I$ = –18 mA | | | –1.2 | V |
| $V_{OH}$ | All inputs/outputs except $\overline{\text{ERR}}$ | $V_{CC}$ = 4.5 V | $I_{OH}$ = – 15 mA | 2.4 | | | V |
| | | | $I_{OH}$ = – 24 mA | 2 | | | |
| $I_{OH}$ | $\overline{\text{ERR}}$ | $V_{CC}$ = 4.5 V, | $V_{OH}$ = 2.4 V | | | 20 | µA |
| $V_{OL}$ | | $V_{CC}$ = 4.5 V, | $I_{OL}$ = 48 mA | | 0.35 | 0.5 | V |
| $I_I$ | | $V_{CC}$ = 5.5 V, | $V_I$ = 5.5 V | | | 0.1 | mA |
| $I_{IH}$‡ | | $V_{CC}$ = 5.5 V, | $V_I$ = 2.7 V | | | 20 | µA |
| $I_{IL}$‡ | Data | $V_{CC}$ = 5.5 V, | $V_I$ = 0.4 V | | | – 0.2 | mA |
| | Control | | | | | – 0.75 | |
| $I_{OS}$§ | | $V_{CC}$ = 5.5 V, | $V_O$ = 0 | –75 | | – 250 | mA |
| $I_{CCL}$ | | $V_{CC}$ = 5.5 V, | Outputs open | | 55 | 80 | mA |
| $I_{CCZ}$ | | $V_{CC}$ = 5.5 V, | Outputs open | | 30 | 45 | mA |

† All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
‡ These parameters include off-state output current for I/O ports only.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

## timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $t_w$ | Pulse duration | $\overline{\text{LE}}$ low | 10 | | ns |
| | | $\overline{\text{CLR}}$ low | 10 | | |
| $t_{su}$ | Setup time before $\overline{\text{LE}}$↓ | Bi and PARITY | 18 | | ns |
| $t_h$ | Hold time after $\overline{\text{LE}}$↓ | Bi and PARITY | 8 | | ns |

### switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 50 pF (unless otherwise noted) (see Note 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 5 V, $T_A$ = 25°C | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | | | |
| $t_{PLH}$ | A or B | B or A | 1 | 5 | 7 | 1 | 8 | ns |
| $t_{PHL}$ | | | 1 | 5 | 7 | 1 | 8 | |
| $t_{PLH}$ | A | PARITY | 1.5 | 10 | 13 | 1.5 | 15 | ns |
| $t_{PHL}$ | | | 1.5 | 10 | 13 | 1.5 | 15 | |
| $t_{PZH}$ | $\overline{\text{OEA}}$ or $\overline{\text{OEB}}$ | A or B | 2 | 12 | 15 | 2 | 17 | ns |
| $t_{PZL}$ | | | 2 | 13 | 16 | 2 | 19 | |
| $t_{PHZ}$ | $\overline{\text{OEA}}$ or $\overline{\text{OEB}}$ | A or B | 2 | 8 | 11 | 2 | 15 | ns |
| $t_{PLZ}$ | | | 2 | 10 | 14 | 2 | 17 | |
| $t_{PLH}$ | $\overline{\text{CLR}}$ | ERR | 1.5 | 11 | 13 | 1.5 | 15 | ns |
| $t_{PHL}$ | $\overline{\text{LE}}$ | | 1.5 | 5 | 7 | 1.5 | 9 | |
| $t_{PLH}$ | $\overline{\text{OEA}}$ | PARITY | 1.5 | 10 | 13 | 1.5 | 15 | ns |
| $t_{PHL}$ | | | 1.5 | 10 | 13 | 1.5 | 16 | |
| $t_{PLH}$ | Bi / PARITY | $\overline{\text{ERR}}$ | 1.5 | 15 | 18 | 1.5 | 20 | ns |
| $t_{PHL}$ | | | 1.5 | 10 | 13 | 1.5 | 15 | |

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

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