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DISCRETE SEMICONDUCTORS

DATA SHEET

BF904; BF904R N-channel dual gate MOS-FETs

Product specification

Supersedes data of 1997 Sep 05

1999 May 17

N-channel dual gate MOS-FETs**BF904; BF904R****FEATURES**

- Specially designed for use at 5 V supply voltage
- Short channel transistor with high transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Superior cross-modulation performance during AGC.

APPLICATIONS

- VHF and UHF applications with 3 to 7 V supply voltage such as television tuners and professional communications equipment.

DESCRIPTION

Enhancement type field-effect transistor in a plastic microminiature SOT143B and SOT143R package. The transistor consists of an amplifier MOS-FET with source

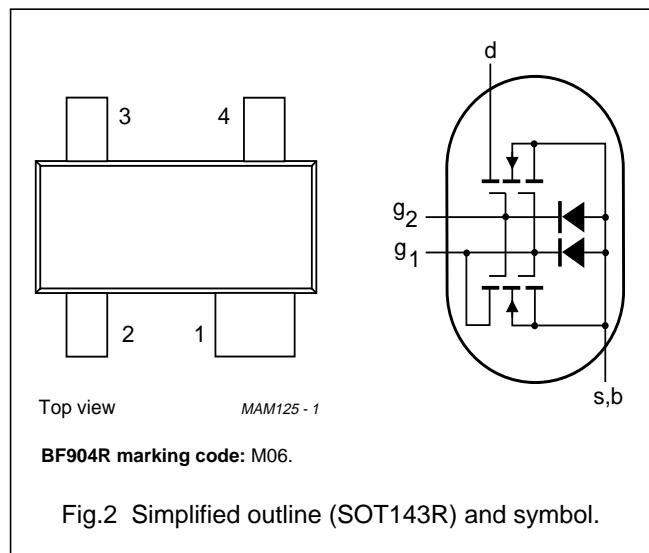
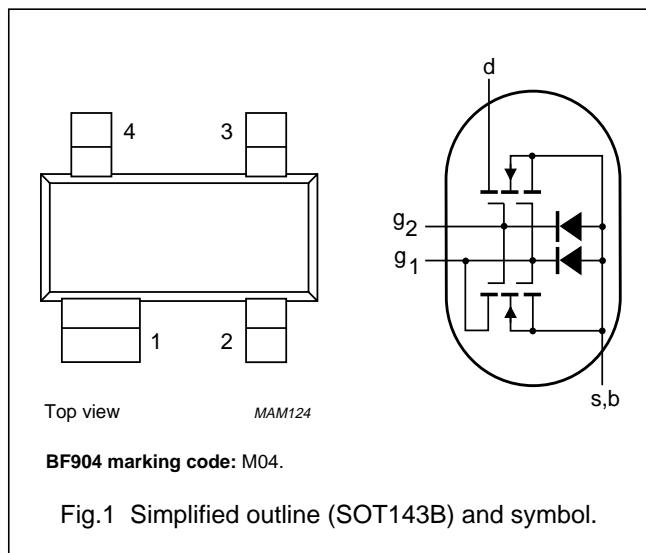
and substrate interconnected and an internal bias circuit to ensure good cross-modulation performance during AGC.

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

PINNING

PIN	SYMBOL	DESCRIPTION
1	s, b	source
2	d	drain
3	g ₂	gate 2
4	g ₁	gate 1

**QUICK REFERENCE DATA**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{DS}	drain-source voltage		-	-	7	V
I _D	drain current		-	-	30	mA
P _{tot}	total power dissipation		-	-	200	mW
T _j	operating junction temperature		-	-	150	°C
y _{fs}	forward transfer admittance		22	25	30	mS
C _{ig1-s}	input capacitance at gate 1		-	2.2	2.6	pF
C _{rs}	reverse transfer capacitance	f = 1 MHz	-	25	35	fF
F	noise figure	f = 800 MHz	-	2	-	dB

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	7	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	± 10	mA
I_{G2}	gate 2 current		–	± 10	mA
P_{tot}	total power dissipation BF904 BF904R	see Fig.3 $T_{amb} \leq 50^\circ\text{C}$; note 1 $T_{amb} \leq 40^\circ\text{C}$; note 1	– –	200 200	mW mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. Device mounted on a printed-circuit board.

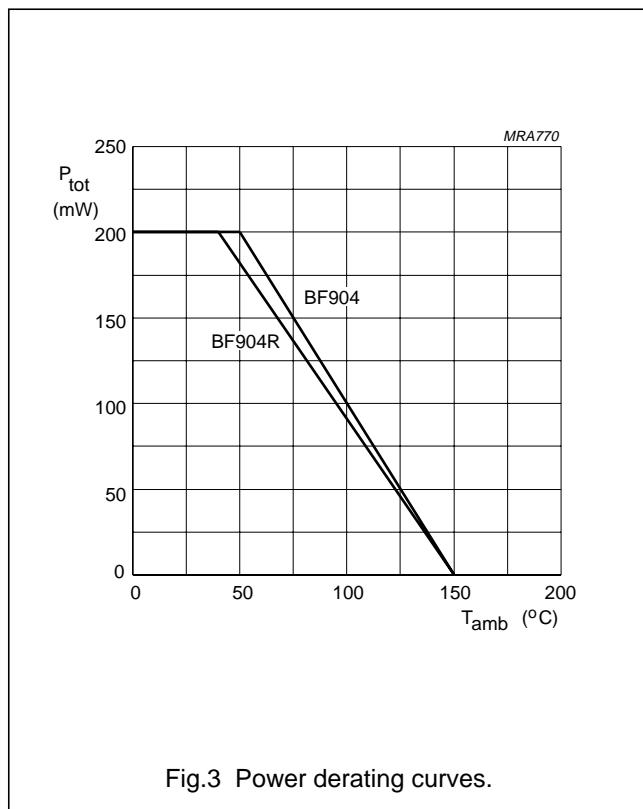


Fig.3 Power derating curves.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient BF904 BF904R	note 1	500	K/W
			550	K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point BF904 BF904R	note 2 $T_s = 92^\circ C$ $T_s = 78^\circ C$	290	K/W
			360	K/W

Notes

1. Device mounted on a printed-circuit board.
2. T_s is the temperature at the soldering point of the source lead.

STATIC CHARACTERISTICS

 $T_j = 25^\circ C$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$; $I_{G1-S} = 10 \text{ mA}$	6	15	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 10 \text{ mA}$	6	15	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$; $I_{S-G1} = 10 \text{ mA}$	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$; $I_{S-G2} = 10 \text{ mA}$	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	$V_{G2-S} = 4 \text{ V}$; $V_{DS} = 5 \text{ V}$; $I_D = 20 \mu\text{A}$	0.3	1	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = V_{DS} = 5 \text{ V}$; $I_D = 20 \mu\text{A}$	0.3	1.2	V
I_{DSX}	drain-source current	$V_{G2-S} = 4 \text{ V}$; $V_{DS} = 5 \text{ V}$ $R_{G1} = 120 \text{ k}\Omega$; note 1	8	13	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$; $V_{G1-S} = 5 \text{ V}$	—	50	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; $V_{G2-S} = 5 \text{ V}$	—	50	nA

Note

1. R_{G1} connects gate 1 to $V_{GG} = 5 \text{ V}$; see Fig.20.

DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25^\circ C$; $V_{DS} = 5 \text{ V}$; $V_{G2-S} = 4 \text{ V}$; $I_D = 10 \text{ mA}$; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25^\circ C$	22	25	30	mS
C_{ig1-s}	input capacitance at gate 1	$f = 1 \text{ MHz}$	—	2.2	2.6	pF
C_{ig2-s}	input capacitance at gate 2	$f = 1 \text{ MHz}$	1	1.5	2	pF
C_{os}	drain-source capacitance	$f = 1 \text{ MHz}$	1	1.3	1.6	pF
C_{rs}	reverse transfer capacitance	$f = 1 \text{ MHz}$	—	25	35	fF
F	noise figure	$f = 200 \text{ MHz}$; $G_S = 2 \text{ mS}$; $B_S = B_{Sopt}$	—	1	1.5	dB
		$f = 800 \text{ MHz}$; $G_S = G_{Sopt}$; $B_S = B_{Sopt}$	—	2	2.8	dB

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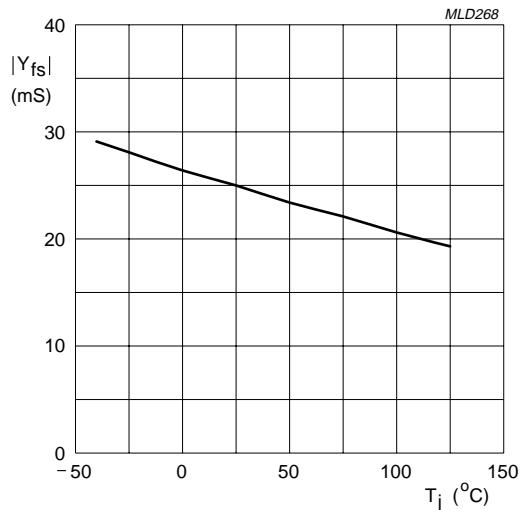
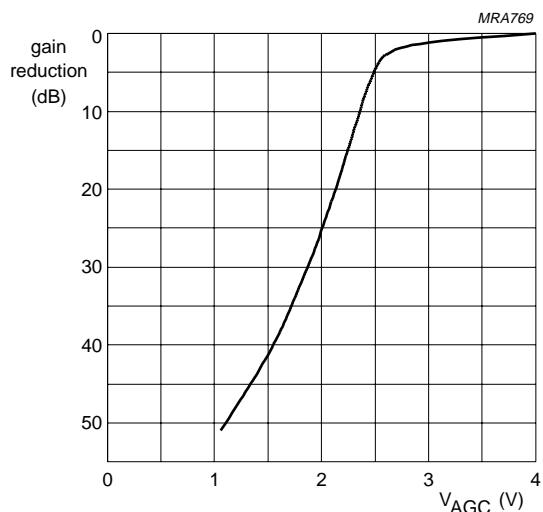
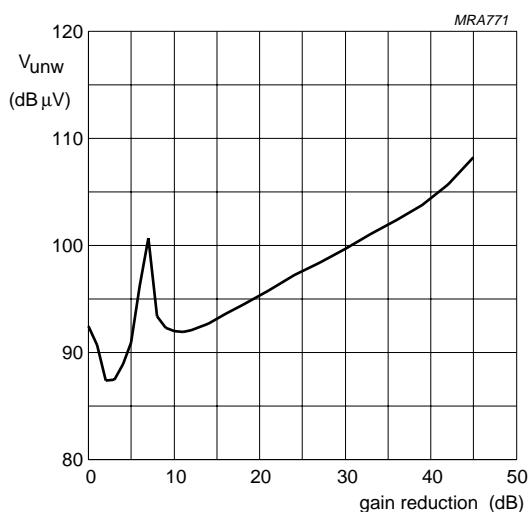


Fig.4 Transfer admittance as a function of the junction temperature; typical values.



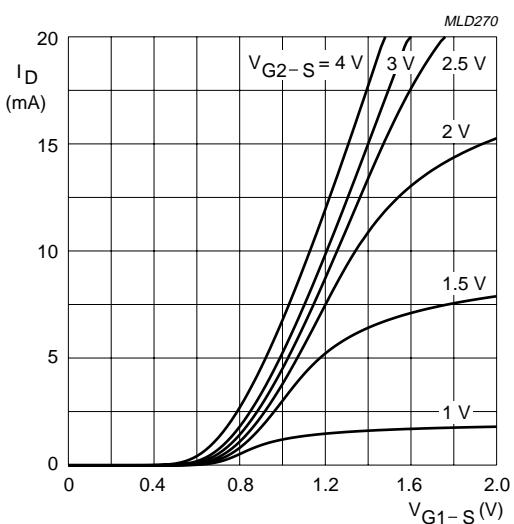
$f = 50$ MHz.

Fig.5 Typical gain reduction as a function of the AGC voltage.



$V_{DS} = 5$ V; $V_{GG} = 5$ V; $f_w = 50$ MHz.
 $f_{unw} = 60$ MHz; $T_{amb} = 25$ °C; $R_{G1} = 120$ kΩ.

Fig.6 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; see Fig.20.

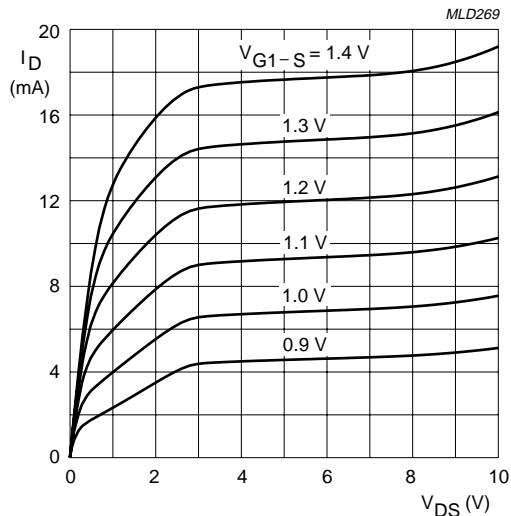


$V_{DS} = 5$ V.
 $T_j = 25$ °C.

Fig.7 Transfer characteristics; typical values.

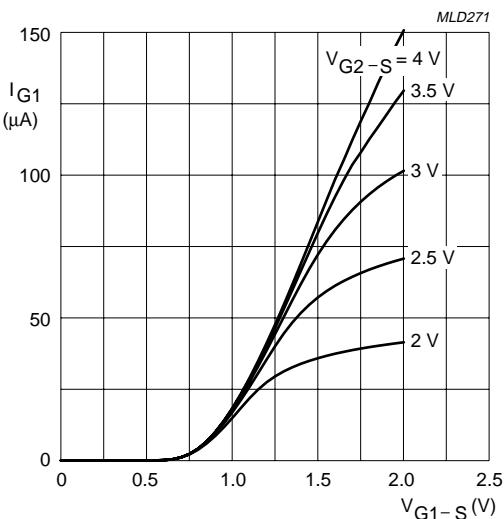
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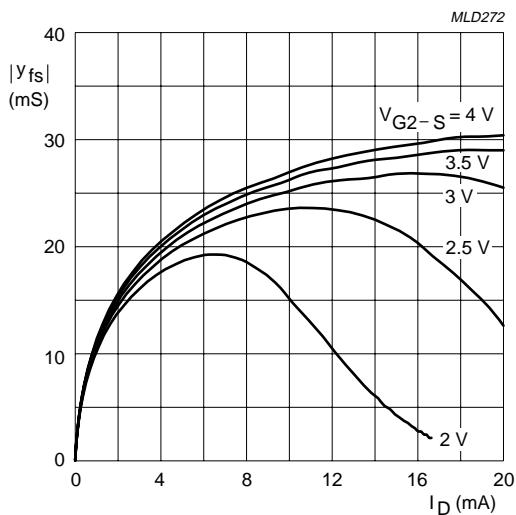
$V_{G2-S} = 4$ V.
 $T_j = 25$ °C.

Fig.8 Output characteristics; typical values.



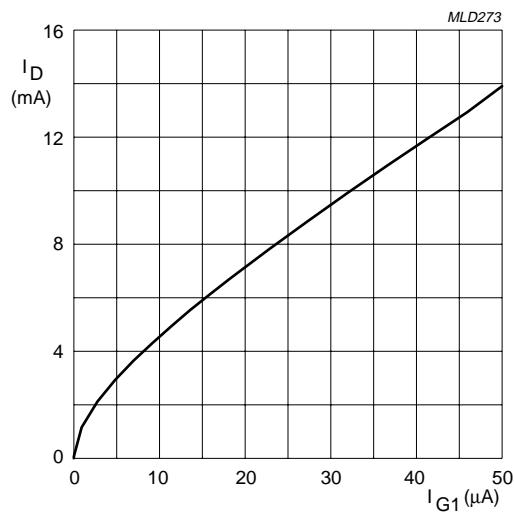
$V_{DS} = 5$ V.
 $T_j = 25$ °C.

Fig.9 Gate 1 current as a function of gate 1 voltage; typical values.



$V_{DS} = 5$ V.
 $T_j = 25$ °C.

Fig.10 Forward transfer admittance as a function of drain current; typical values.

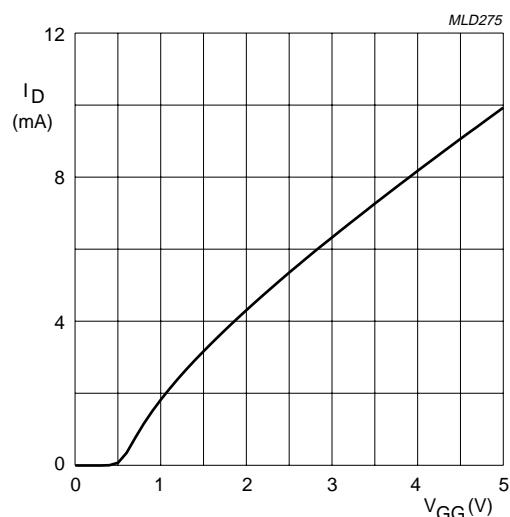


$V_{DS} = 5$ V.
 $V_{G2-S} = 4$ V.
 $T_j = 25$ °C.

Fig.11 Drain current as a function of gate 1 current; typical values.

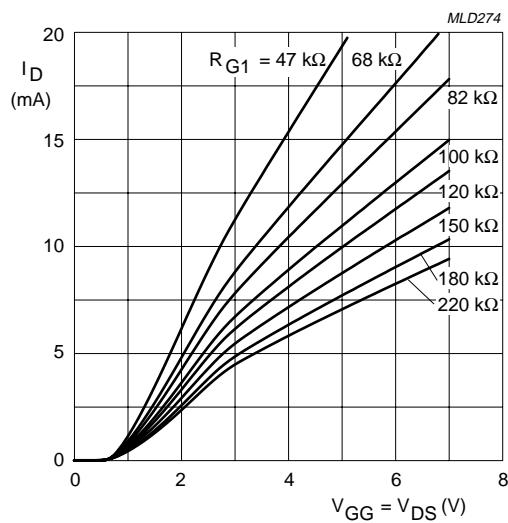
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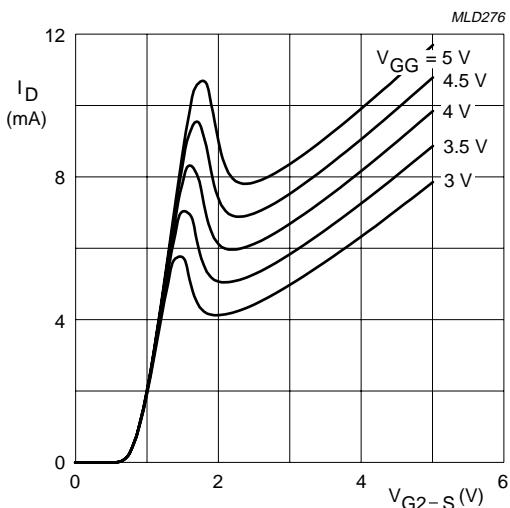
$V_{DS} = 5$ V; $V_{G2-S} = 4$ V.
 $R_{G1} = 120$ k Ω (connected to V_{GG}); $T_j = 25$ °C.

Fig.12 Drain current as a function of gate 1 supply voltage (= V_{GG}); typical values; see Fig.20.



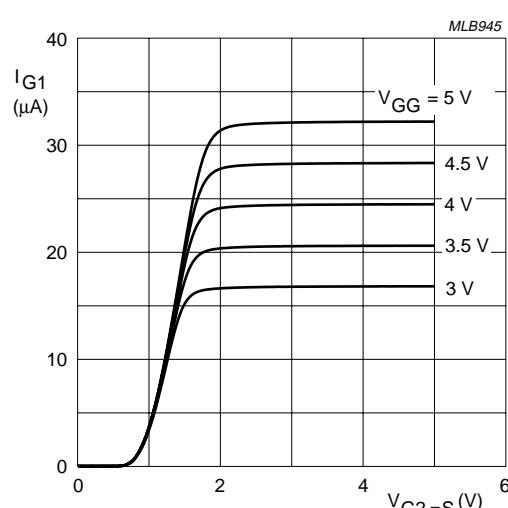
$V_{G2-S} = 4$ V.
 R_{G1} connected to V_{GG} ; $T_j = 25$ °C.

Fig.13 Drain current as a function of gate 1 (= V_{GG}) and drain supply voltage; typical values; see Fig.20.



$V_{DS} = 5$ V; $T_j = 25$ °C.
 $R_{G1} = 120$ k Ω (connected to V_{GG}).

Fig.14 Drain current as a function of gate 2 voltage; typical values; see Fig.20.

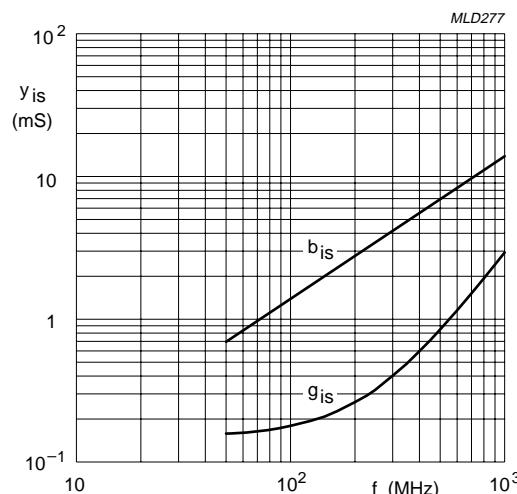


$V_{DS} = 5$ V; $T_j = 25$ °C.
 $R_{G1} = 120$ k Ω (connected to V_{GG}).

Fig.15 Gate 1 current as a function of gate 2 voltage; typical values; see Fig.20.

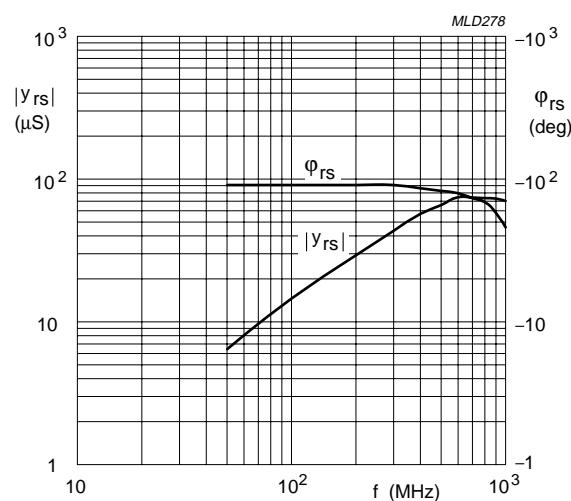
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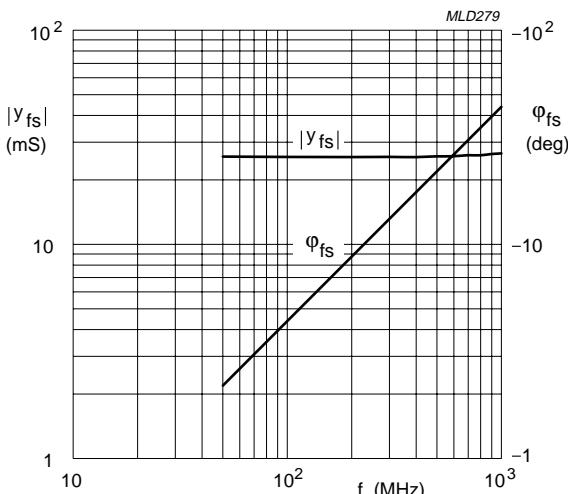
$V_{DS} = 5$ V; $V_{G2} = 4$ V.
 $I_D = 15$ mA; $T_{amb} = 25$ °C.

Fig.16 Input admittance as a function of frequency; typical values.



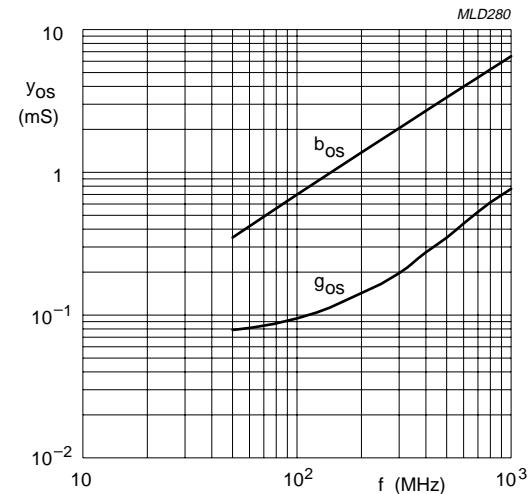
$V_{DS} = 5$ V; $V_{G2} = 4$ V.
 $I_D = 15$ mA; $T_{amb} = 25$ °C.

Fig.17 Reverse transfer admittance and phase as a function of frequency; typical values.



$V_{DS} = 5$ V; $V_{G2} = 4$ V.
 $I_D = 15$ mA; $T_{amb} = 25$ °C.

Fig.18 Forward transfer admittance and phase as a function of frequency; typical values.



$V_{DS} = 5$ V; $V_{G2} = 4$ V.
 $I_D = 15$ mA; $T_{amb} = 25$ °C.

Fig.19 Output admittance as a function of frequency; typical values.

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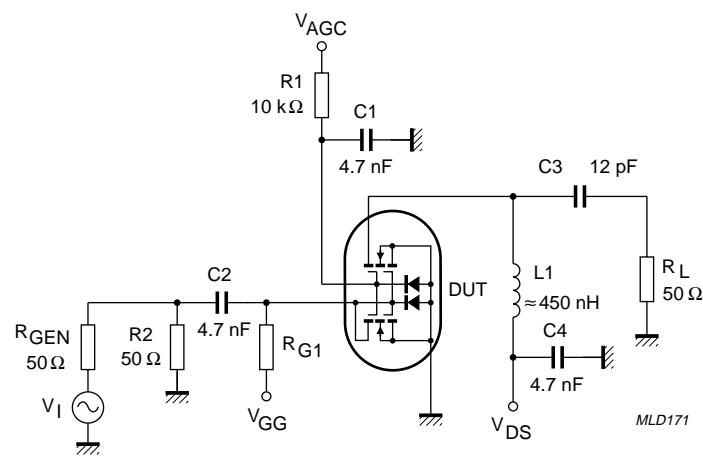


Fig.20 Cross-modulation test set-up.

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Table 1 Scattering parameters: $V_{DS} = 5$ V; $V_{G2-S} = 4$ V; $I_D = 10$ mA

f (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
40	0.989	-3.4	2.420	175.7	0.000	79.9	0.993	-1.6
100	0.985	-8.3	2.414	169.1	0.001	78.3	0.992	-3.9
200	0.976	-16.4	2.368	158.8	0.003	80.3	0.987	-7.8
300	0.958	-24.1	2.301	148.5	0.004	73.7	0.980	-11.4
400	0.942	-32.0	2.251	138.8	0.005	70.7	0.974	-15.2
500	0.918	-39.3	2.170	129.5	0.005	67.2	0.966	-18.7
600	0.899	-46.0	2.080	120.7	0.005	67.8	0.958	-22.2
700	0.876	-52.6	2.001	112.1	0.005	68.6	0.951	-25.5
800	0.852	-58.8	1.924	103.2	0.005	72.9	0.944	-28.9
900	0.823	-64.9	1.829	94.7	0.005	78.7	0.937	-32.1
1000	0.800	-70.9	1.747	86.5	0.005	88.3	0.933	-35.2
1200	0.750	-82.4	1.621	70.7	0.005	120.5	0.928	-41.7
1400	0.719	-92.7	1.535	54.6	0.008	139.8	0.930	-48.4
1600	0.682	-102.5	1.424	39.4	0.010	137.8	0.924	-54.9
1800	0.642	-109.8	1.349	22.5	0.013	156.8	0.928	-62.9
2000	0.602	-116.5	1.283	1.1	0.018	175.1	0.928	-73.1
2200	0.547	-124.9	1.130	-15.1	0.014	172.6	0.887	-81.0
2400	0.596	-128.7	1.018	-49.1	0.040	-163.9	0.837	-95.8
2600	0.682	-132.6	0.979	-79.4	0.077	-164.0	0.778	-109.6
2800	0.771	-142.5	0.804	-116.2	0.120	178.8	0.629	-119.5
3000	0.793	-157.5	0.541	-153.5	0.149	158.3	0.479	-119.9

Table 2 Noise data: $V_{DS} = 5$ V; $V_{G2-S} = 4$ V; $I_D = 10$ mA

f (MHz)	F_{min} (dB)	Γ_{opt}		r_n
		(ratio)	(deg)	
800	2.00	0.686	49.6	50.40

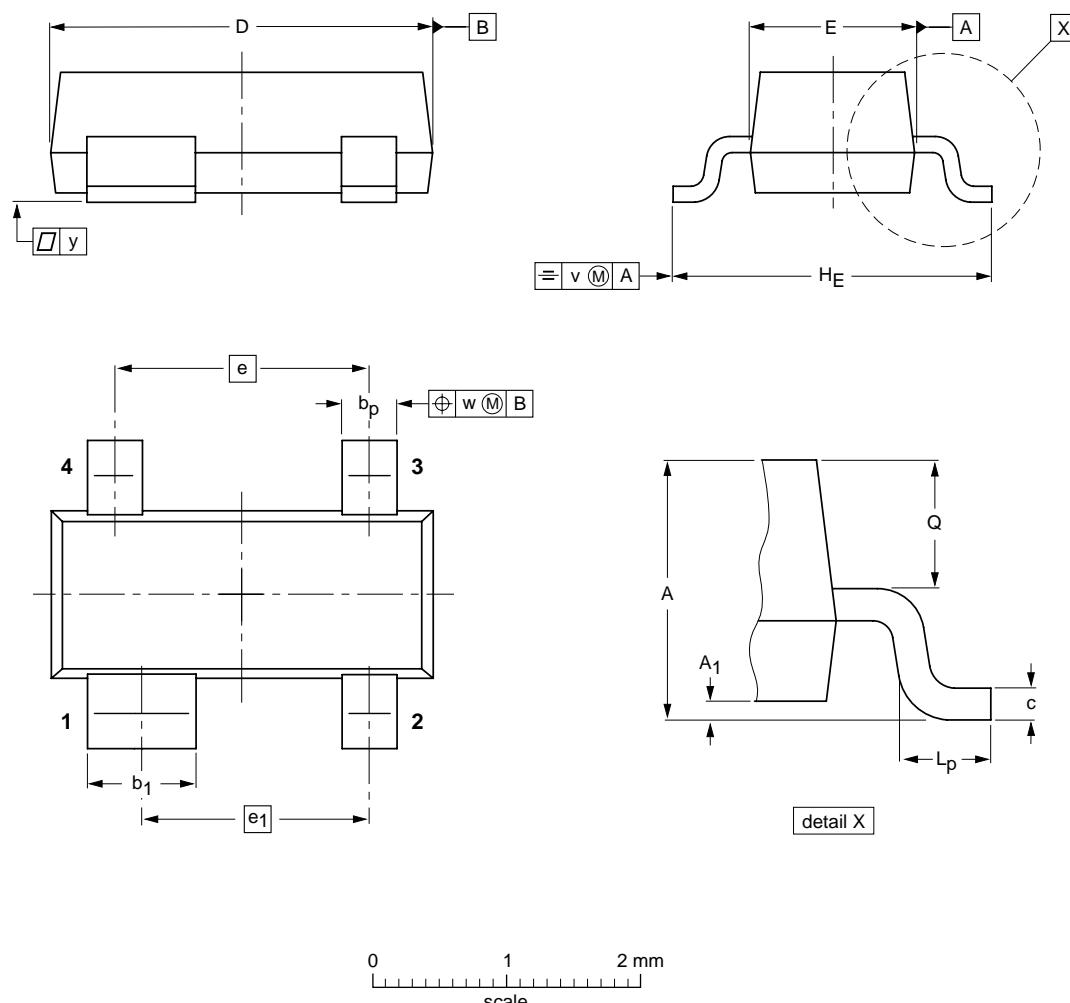
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PACKAGE OUTLINES

Plastic surface mounted package; 4 leads

SOT143B



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

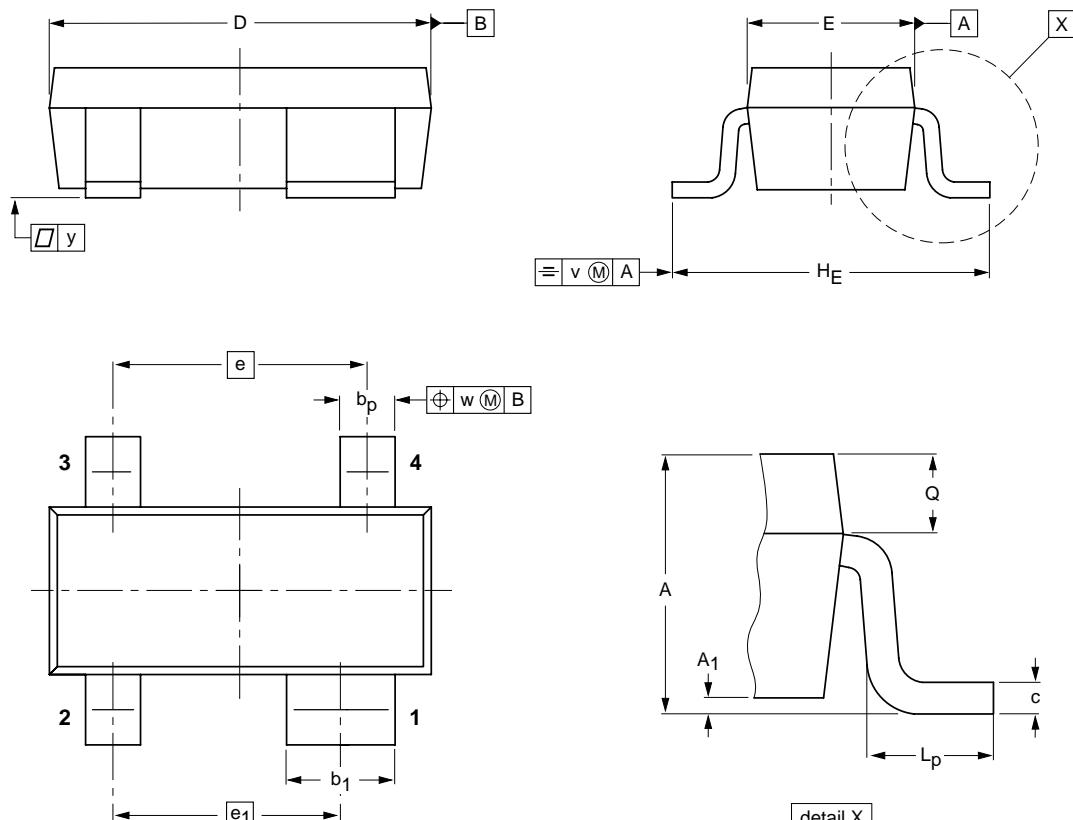
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143B						97-02-28

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Plastic surface mounted package; reverse pinning; 4 leads

SOT143R



0 1 2 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	l_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143R						97-03-10

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DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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NOTES

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NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113, Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor, 51 James Bourchier Blvd., 1407 SOFIA, Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V, Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO, Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex, Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor, 254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025, Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division, Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510, Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3, 20124 MILANO, Tel. +39 02 67 52 2531, Fax. +39 02 67 52 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905, Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO, Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA, Tel. +48 22 612 2831, Fax. +48 22 612 2327

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Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW, Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762, Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale, 2092 JOHANNESBURG, P.O. Box 58088 Newville 2114, Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor, 04547-130 SÃO PAULO, SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA, Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM, Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH, Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1, TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd., 209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260, Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye, ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7, 252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD, Tel. +381 11 62 5344, Fax.+381 11 63 5777

For all other countries apply to: Philips Semiconductors, International Marketing & Sales Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

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Printed in The Netherlands

125004/00/05/PP16

Date of release: 1999 May 17

Document order number: 9397 750 05898

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