

# TIBPAL20L8-5C, TIBPAL20R4-5C, TIBPAL20R6-5C, TIBPAL20R8-5C TIBPAL20L8-7M, TIBPAL20R4-7M, TIBPAL20R6-7M, TIBPAL20R8-7M HIGH-PERFORMANCE *IMPACT-X*<sup>TM</sup> *PAL*<sup>®</sup> CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

## • High-Performance Operation:

$f_{\max}$  (no feedback)

TIBPAL20R' -5C Series . . . 125 MHz Min

TIBPAL20R' -7M Series . . . 100 MHz Min

$f_{\max}$  (internal feedback)

TIBPAL20R' -5C Series . . . 125 MHz Min

TIBPAL20R' -7M Series . . . 100 MHz Min

$f_{\max}$  (external feedback)

TIBPAL20R' -5C Series . . . 117 MHz Min

TIBPAL20R' -7M Series . . . 74 MHz Min

Propagation Delay

TIBPAL20L8-5C Series . . . 5 ns Max

TIBPAL20L8-7M Series . . . 7 ns Max

TIBPAL20R' -5C Series

(CLK-to-Q) . . . 4 ns Max

TIBPAL20R' -7M Series

(CLK-to-Q) . . . 6.5 ns Max

- Functionally Equivalent, but Faster Than, Existing 24-Pin PLDs
- Preload Capability on Output Registers Simplifies Testing
- Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)
- Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs
- Security Fuse Prevents Duplication

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORT S
PAL20L8	14	2	0	6
PAL20R4	12	0	4 (3-state buffers)	4
PAL20R6	12	0	6 (3-state buffers)	2
PAL20R8	12	0	8 (3-state buffers)	0

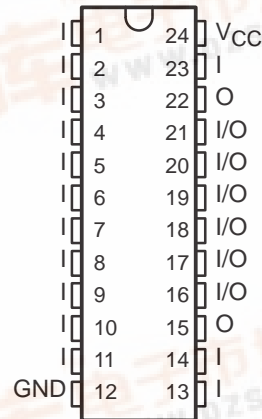
## description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These *IMPACT-X*<sup>TM</sup> circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board.

The TIBPAL20' C series is characterized from 0°C to 75°C. The TIBPAL20' M series is characterized for operation over the full military temperature range of -55°C to 125°C.

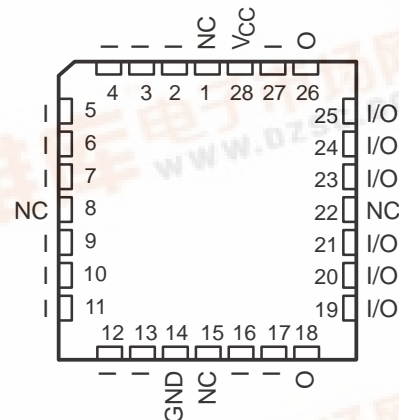
TIBPAL20L8'  
C SUFFIX . . . JT OR NT PACKAGE  
M SUFFIX . . . JT PACKAGE

(TOP VIEW)



TIBPAL20L8'  
C SUFFIX . . . FN PACKAGE  
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



NC — No internal connection  
Pin assignments in operating mode

These devices are covered by U.S. Patent 4,410,987.  
*IMPACT-X* is a trademark of Texas Instruments Incorporated.  
*PAL* is a registered trademark of Advanced Micro Devices Inc.

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

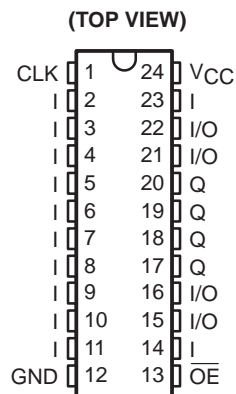
TEXAS  
INSTRUMENTS

Copyright © 1992, Texas Instruments Incorporated

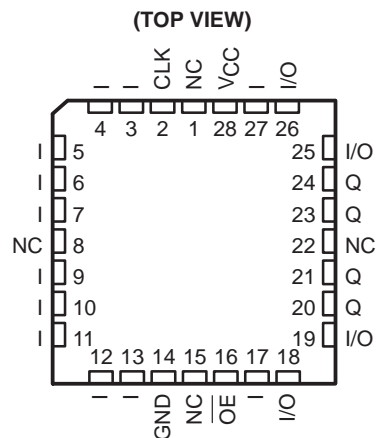
# TIBPAL20R4-5C, TIBPAL20R6-5C, TIBPAL20R8-5C TIBPAL20R4-7M, TIBPAL20R6-7M, TIBPAL20R8-7M HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

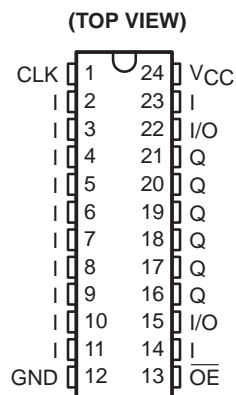
**TIBPAL20R4'**  
C SUFFIX ... JT OR NT PACKAGE  
M SUFFIX ... JT PACKAGE



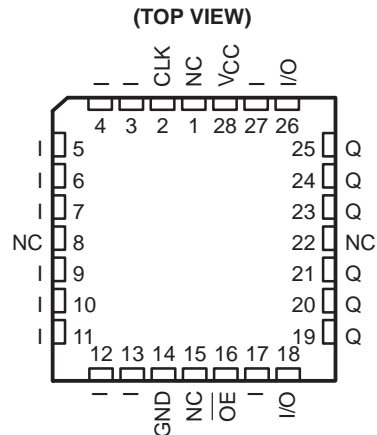
**TIBPAL20R4'**  
C SUFFIX ... FN PACKAGE  
M SUFFIX ... FK PACKAGE



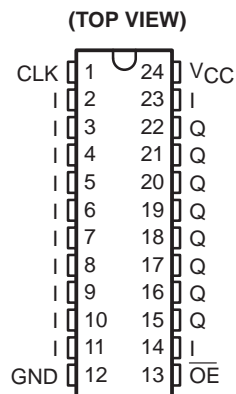
**TIBPAL20R6'**  
C SUFFIX ... JT OR NT PACKAGE  
M SUFFIX ... JT PACKAGE



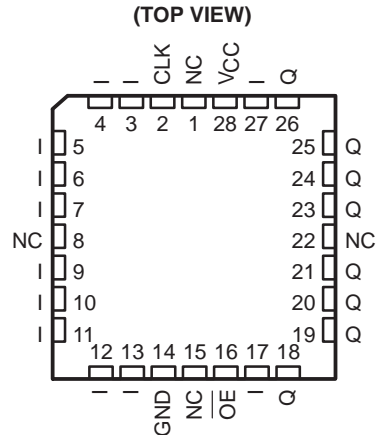
**TIBPAL20R6'**  
C SUFFIX ... FN PACKAGE  
M SUFFIX ... FK PACKAGE



**TIBPAL20R8'**  
C SUFFIX ... JT OR NT PACKAGE  
M SUFFIX ... JT PACKAGE



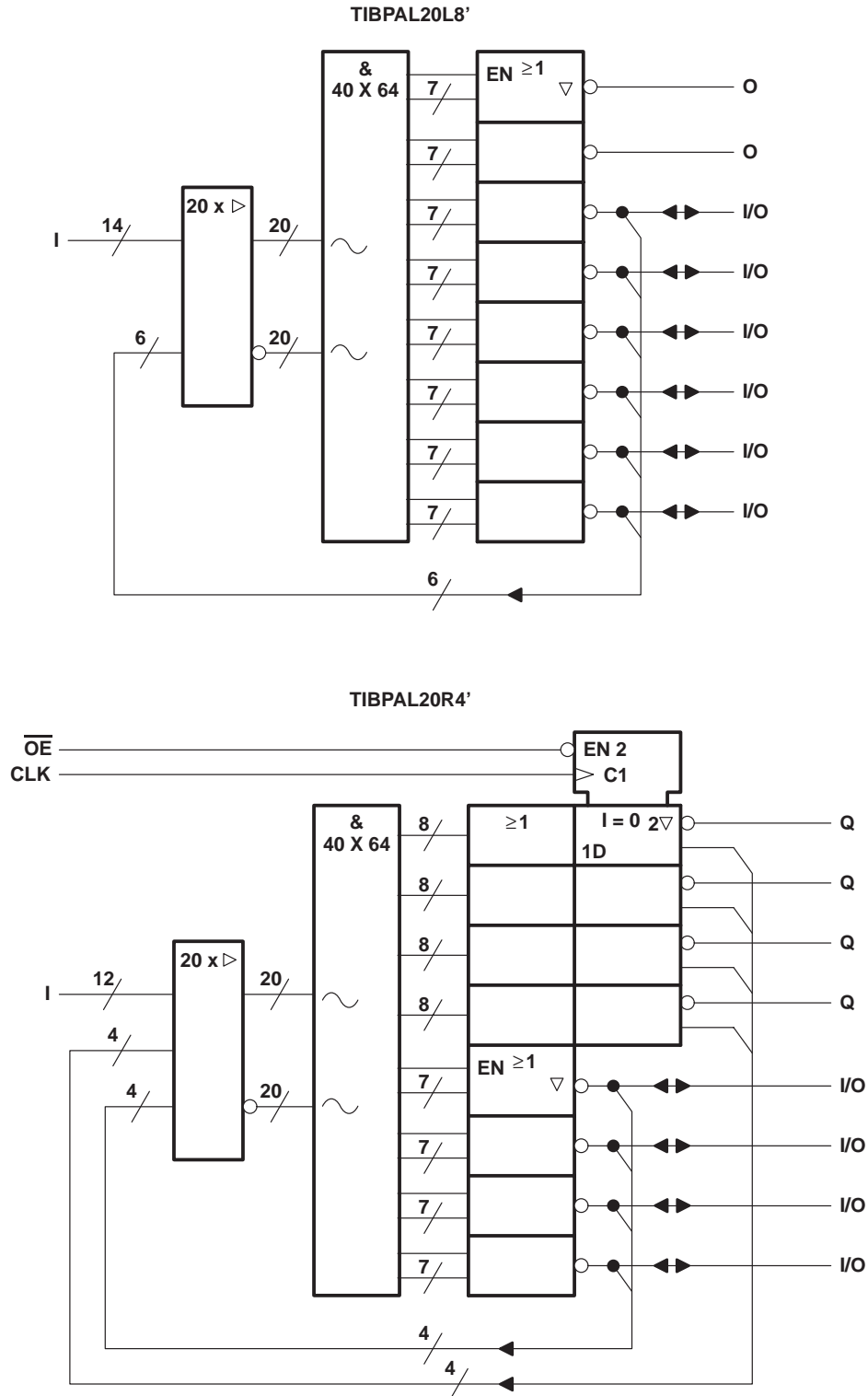
**TIBPAL20R8'**  
C SUFFIX ... FN PACKAGE  
M SUFFIX ... FK PACKAGE



Pin assignments in operating mode

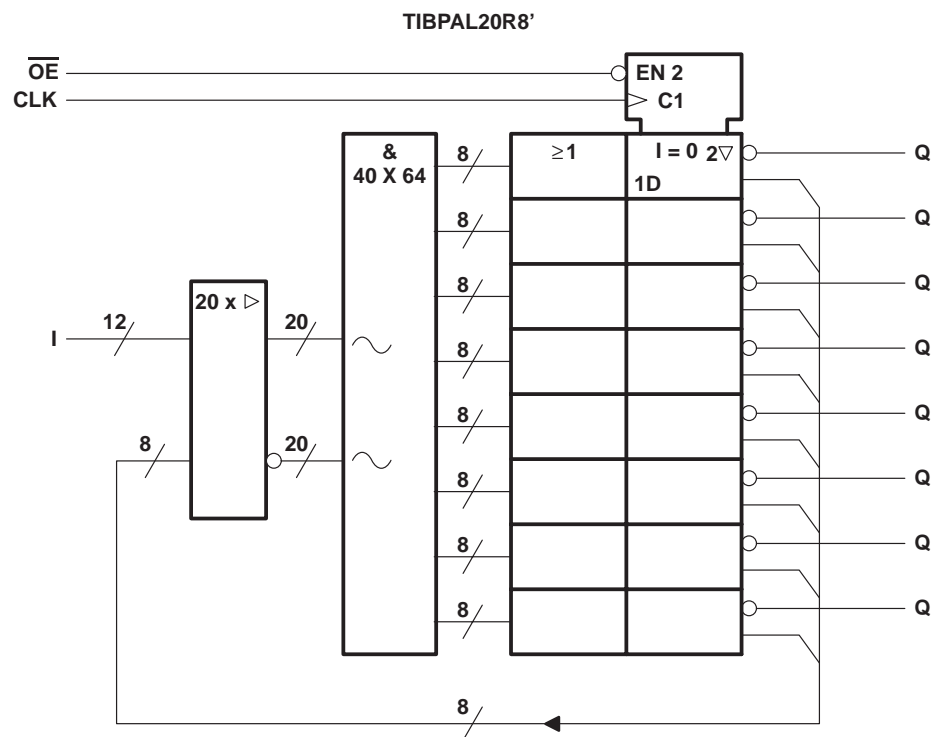
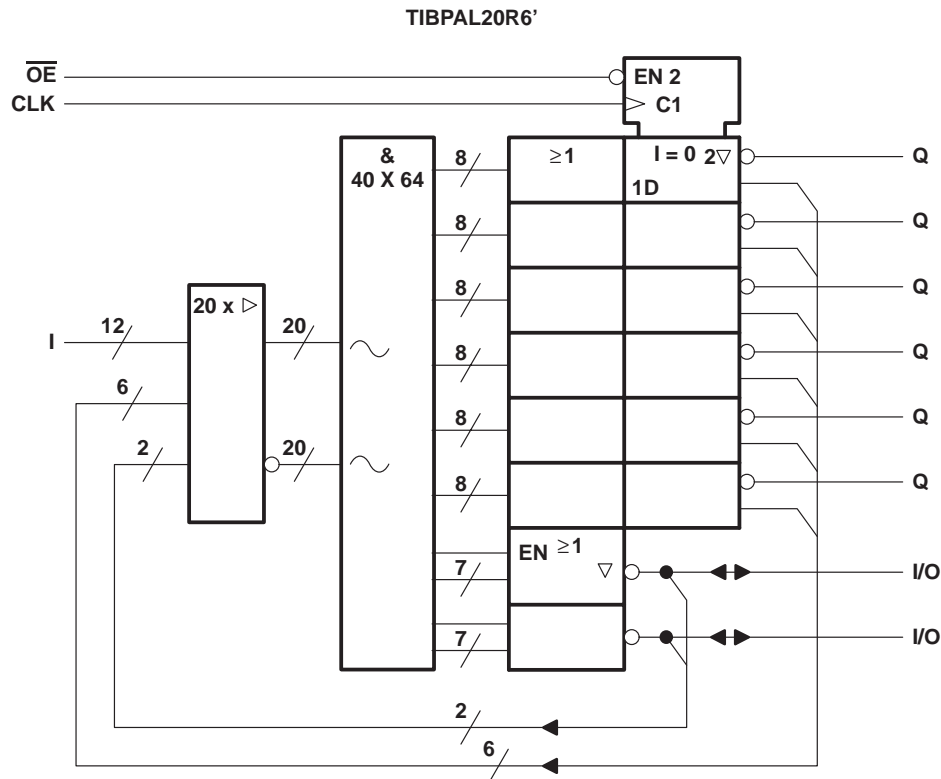
NC — No internal connection

functional block diagrams (positive logic)



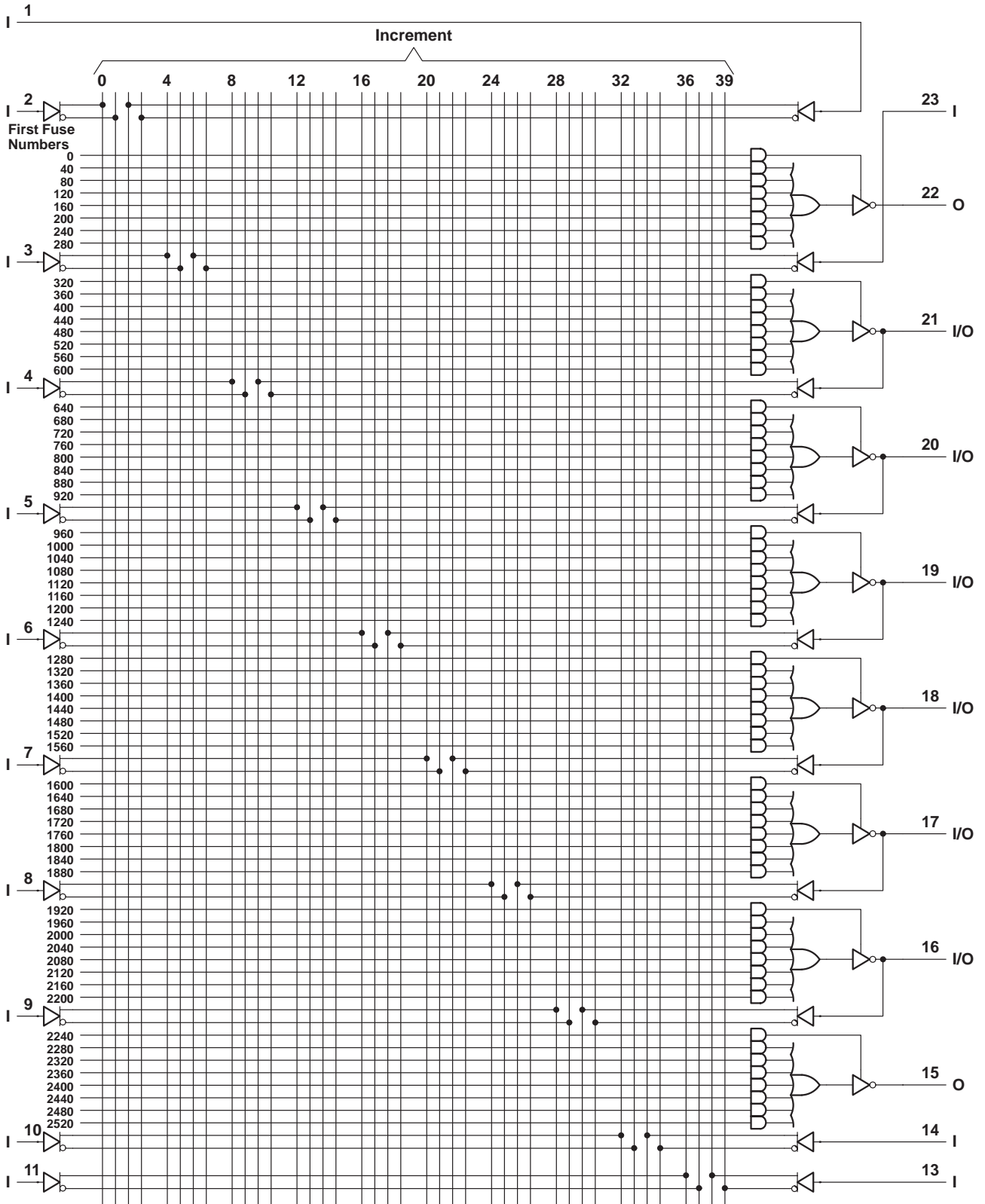
TIBPAL20R6-5C, TIBPAL20R8-5C  
TIBPAL20R6-7M, TIBPAL20R8-7M  
HIGH-PERFORMANCE *IMPACT-X*™ PAL® CIRCUITS  
SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

functional block diagrams (positive logic)



~ denotes fused inputs

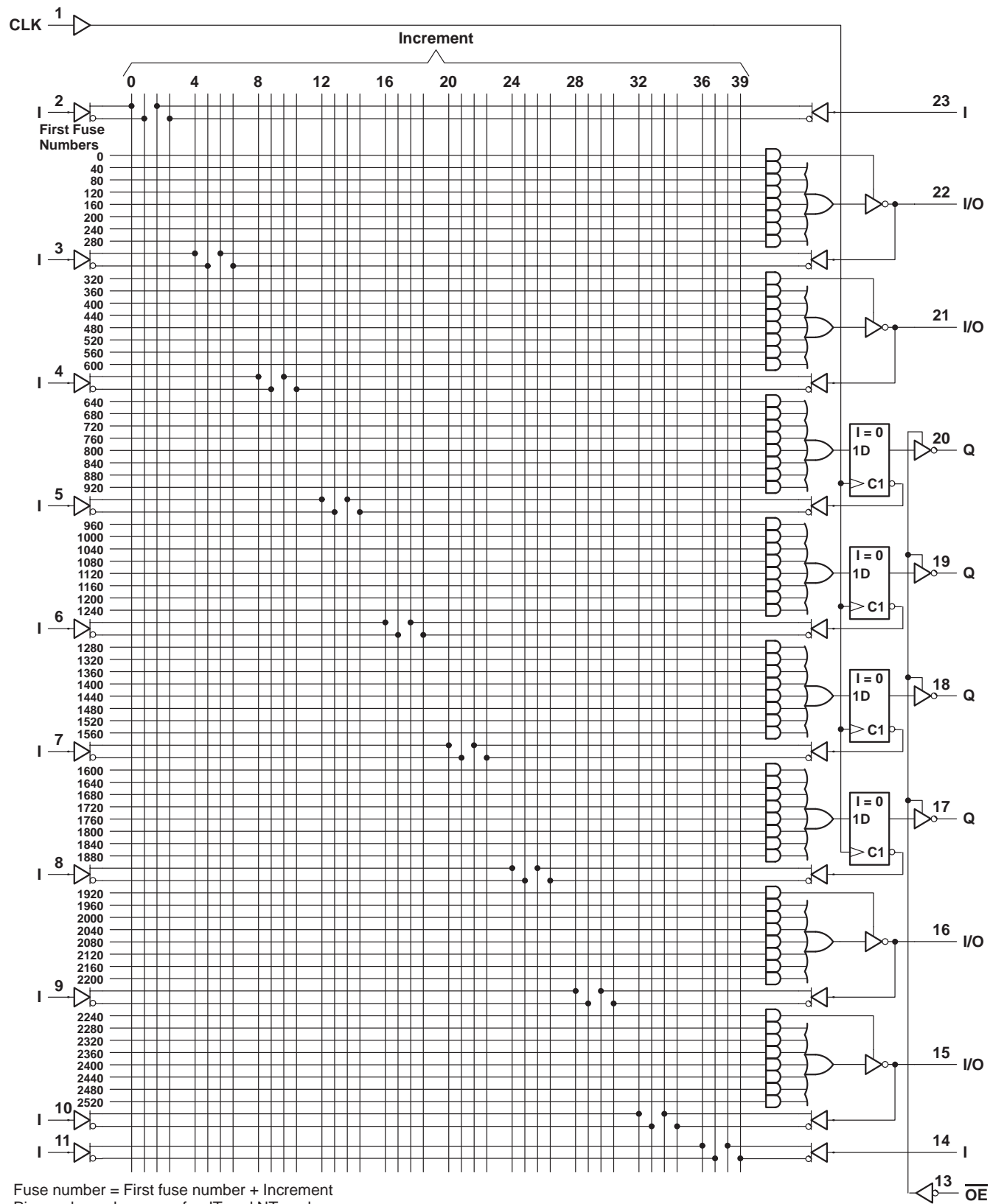
**logic diagram (positive logic)**



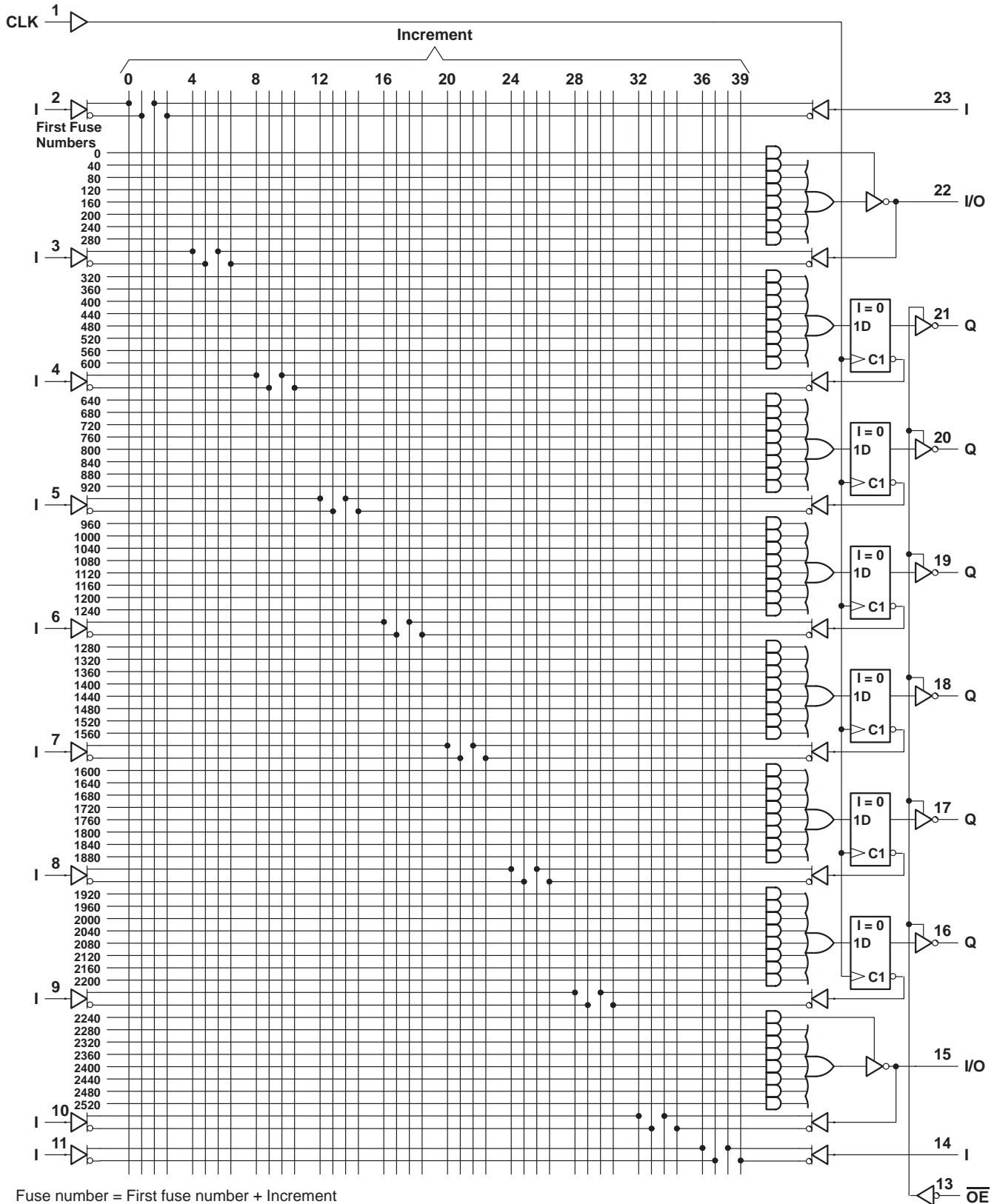
Fuse number = First fuse number + Increment  
Pin numbers shown are for JT and NT packages.

**TIBPAL20R4-5C**  
**TIBPAL20R4-7M**  
**HIGH-PERFORMANCE *IMPACT-X*™ PAL® CIRCUITS**  
 SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

**logic diagram (positive logic)**

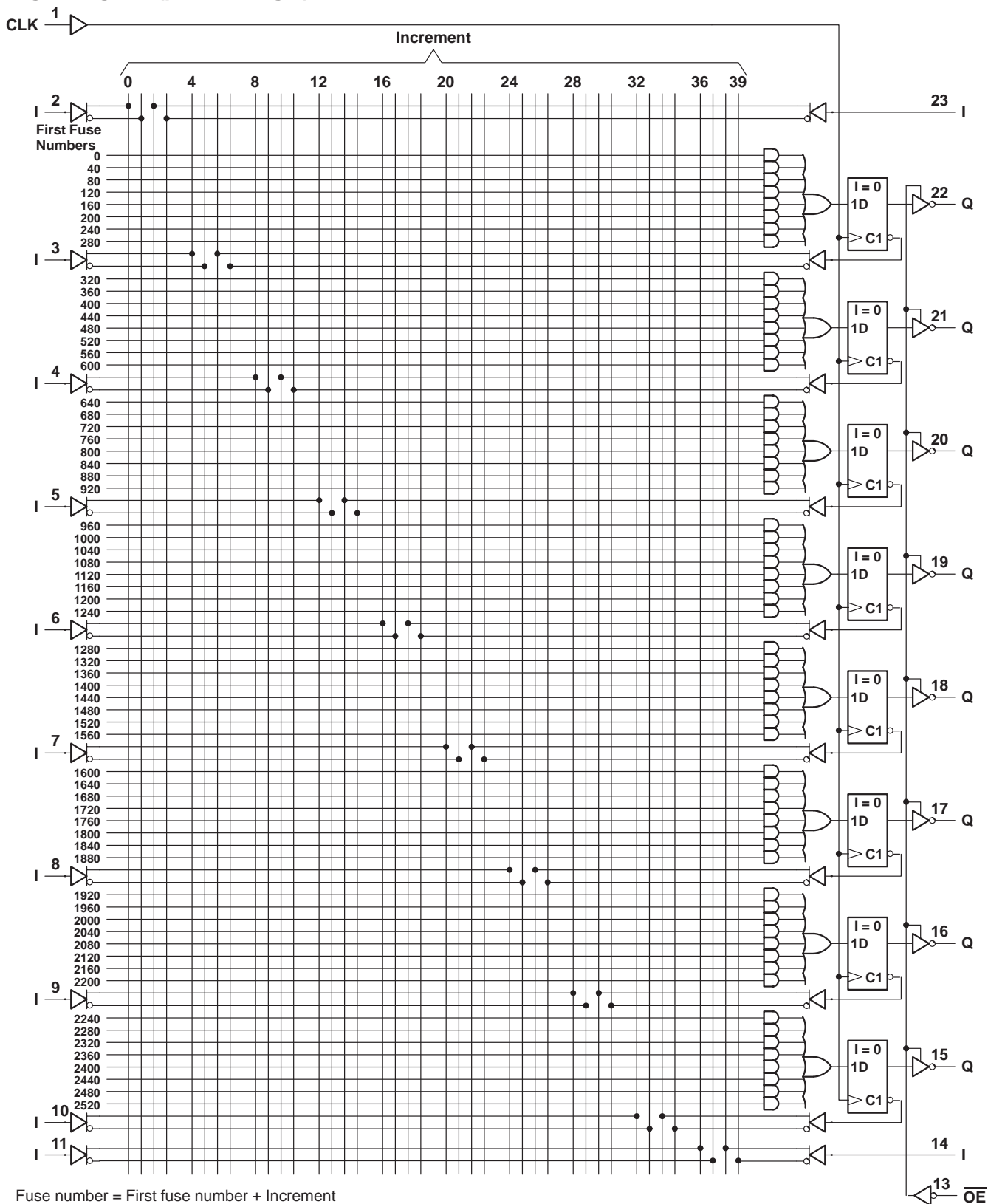


**logic diagram (positive logic)**



**TIBPAL20R8-5C**  
**TIBPAL20R8-7M**  
**HIGH-PERFORMANCE *IMPACT-X*™ PAL® CIRCUITS**  
 SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

**logic diagram (positive logic)**





# TIBPAL20L8-5C HIGH-PERFORMANCE *IMPACT-X*™ PAL® CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature	0°C to 75°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

## recommended operating conditions

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.75	5	5.25	V
$V_{IH}$ High-level input voltage (see Note 2)	2		5.5	V
$V_{IL}$ Low-level input voltage (see Note 2)			0.8	V
$I_{OH}$ High-level output current			–3.2	mA
$I_{OL}$ Low-level output current			24	mA
$T_A$ Operating free-air temperature	0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

## electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	$V_{CC} = 4.75$ V,	$I_I = -18$ mA		–0.8	–1.5	V
$V_{OH}$	$V_{CC} = 4.75$ V,	$I_{OH} = -3.2$ mA	2.4	2.7		V
$V_{OL}$	$V_{CC} = 4.75$ V,	$I_{OL} = 24$ mA		0.3	0.5	V
$I_{OZH}^{\ddagger}$	$V_{CC} = 5.25$ V,	$V_O = 2.7$ V			100	μA
$I_{OZL}^{\ddagger}$	$V_{CC} = 5.25$ V,	$V_O = 0.4$ V			–100	μA
$I_I$	$V_{CC} = 5.25$ V,	$V_I = 5.5$ V			100	μA
$I_{IH}^{\ddagger}$	$V_{CC} = 5.25$ V,	$V_I = 2.7$ V			25	μA
$I_{IL}^{\ddagger}$	$V_{CC} = 5.25$ V,	$V_I = 0.4$ V			–250	μA
$I_{OS}^{\S}$	$V_{CC} = 5.25$ V,	$V_O = 0.5$ V	–30	–70	–130	mA
$I_{CC}$	$V_{CC} = 5.25$ V,	$V_I = 0$ , Outputs open			210	mA
$C_i$	$f = 1$ MHz,	$V_I = 2$ V		8.5		pF
$C_o$	$f = 1$ MHz,	$V_O = 2$ V		10		pF

† All typical values are at  $V_{CC} = 5$  V,  $T_A = 25^\circ\text{C}$ .

‡ I/O leakage is the worst case of  $I_{OZL}$  and  $I_{IL}$  or  $I_{OZH}$  and  $I_{IH}$ , respectively.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.  $V_O$  is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		TEST CONDITIONS	TIBPAL20L8-5CFN		TIBPAL20L8-5CJT TIBPAL20L8-5CNT		UNIT
					MIN	MAX	MIN	MAX	
t <sub>pd</sub>	I, I/O	O, I/O	with up to 4 outputs switching	R1 = 200 Ω, R2 = 200 Ω, See Figure 8	1.5	5	1.5	5	ns
	I, I/O	O, I/O	with more than 4 outputs switching		1.5	5	1.5	5.5	
t <sub>en</sub>	I, I/O	O, I/O			2	7	2	7	ns
t <sub>djs</sub>	I, I/O	O, I/O			2	7	2	7	ns

# TIBPAL20R4-5C, TIBPAL20R6-5C HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

## recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.75	5	5.25	V
$V_{IH}$	High-level input voltage (see Note 2)	2		5.5	V
$V_{IL}$	Low-level input voltage (see Note 2)			0.8	V
$I_{OH}$	High-level output current			–3.2	mA
$I_{OL}$	Low-level output current			24	mA
$f_{clock}$	Clock frequency	0		125	MHz
$t_w$	Pulse duration, clock	High		4	ns
		Low		4	
$t_{su}$	Setup time, input or feedback before clock↑	4.5			ns
$t_h$	Hold time, input or feedback after clock↑	0			ns
$T_A$	Operating free-air temperature	0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

# TIBPAL20R4-5C, TIBPAL20R6-5C HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

## electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 4.75\text{ V}$ ,	$I_I = -18\text{ mA}$		-0.8	-1.5	V
$V_{OH}$		$V_{CC} = 4.75\text{ V}$ ,	$I_{OH} = -3.2\text{ mA}$	2.4	2.7		V
$V_{OL}$		$V_{CC} = 4.75\text{ V}$ ,	$I_{OL} = 24\text{ mA}$		0.3	0.5	V
$I_{OZH}^{\ddagger}$		$V_{CC} = 5.25\text{ V}$ ,	$V_O = 2.7\text{ V}$			100	$\mu\text{A}$
$I_{OZL}^{\ddagger}$		$V_{CC} = 5.25\text{ V}$ ,	$V_O = 0.4\text{ V}$			-100	$\mu\text{A}$
$I_I$		$V_{CC} = 5.25\text{ V}$ ,	$V_I = 5.5\text{ V}$			100	$\mu\text{A}$
$I_{IH}^{\ddagger}$		$V_{CC} = 5.25\text{ V}$ ,	$V_I = 2.7\text{ V}$			25	$\mu\text{A}$
$I_{IL}^{\ddagger}$		$V_{CC} = 5.25\text{ V}$ ,	$V_I = 0.4\text{ V}$			-250	$\mu\text{A}$
$I_{OS}^{\S}$		$V_{CC} = 5.25\text{ V}$ ,	$V_O = 0.5\text{ V}$	-30	-70	-130	mA
$I_{CC}$		$V_{CC} = 5.25\text{ V}$ ,	$V_I = 0$ , Outputs open			210	mA
$C_i$	$I$	$f = 1\text{ MHz}$ ,	$V_I = 2\text{ V}$		8.5		pF
	$\text{CLK}/\overline{\text{OE}}$				7.5		
$C_o$	$I/O$	$f = 1\text{ MHz}$ ,	$V_O = 2\text{ V}$		10		pF
	$Q$				7		

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TIBPAL20R4-5CFN TIBPAL20R6-5CFN			TIBPAL20R4-5CJT TIBPAL20R4-5CNT TIBPAL20R6-5CJT TIBPAL20R6-5CNT			UNIT	
				MIN	TYP†	MAX	MIN	TYP†	MAX		
f <sub>max</sub> <sup>¶</sup>	without feedback		R1 = 200 Ω, R2 = 200 Ω, See Figure 8	125			125			MHz	
	with internal feedback (counter configuration)			125			125				
	with external feedback			117			111				
t <sub>pd</sub>	CLK↑	Q		1.5			4	1.5	4.5	ns	
t <sub>pd</sub>	CLK↑	Internal feedback		3.5			3.5			ns	
t <sub>pd</sub>	I, I/O	I/O		1.5			5	1.5	5	ns	
t <sub>en</sub>	OE↓	Q		1.5			6	1.5	6	ns	
t <sub>dis</sub>	OE↑	Q		1			6.5	1	7	ns	
t <sub>en</sub>	I, I/O	I/O		2			7	2	7	ns	
t <sub>dis</sub>	I, I/O	I/O		2			7	2	7	ns	
t <sub>r</sub>				1.5			1.5			ns	
t <sub>f</sub>				1.5			1.5			ns	
t <sub>sk(o)</sub> <sup>#</sup>	Skew between registered outputs			0.5			0.5			ns	

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ I/O leakage is the worst case of  $I_{OZL}$  and  $I_{IL}$  or  $I_{OZH}$  and  $I_{IH}$ , respectively.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.  $V_O$  is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

¶ See 'f<sub>max</sub> Specification' near the end of this data sheet.

#  $t_{sk(o)}$  is the skew time between registered outputs.

# TIBPAL20R8-5C

## HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

### recommended operating conditions

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	4.75	5	5.25	V
$V_{IH}$	High-level input voltage (see Note 2)	2		5.5	V
$V_{IL}$	Low-level input voltage (see Note 2)			0.8	V
$I_{OH}$	High-level output current			–3.2	mA
$I_{OL}$	Low-level output current			24	mA
$f_{clock}$	Clock frequency	0		125	MHz
$t_w$	Pulse duration, clock	High		4	ns
		Low		4	
$t_{su}$	Setup time, input or feedback before clock↑	4.5			ns
$t_h$	Hold time, input or feedback after clock↑	0			ns
$T_A$	Operating free-air temperature	0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

# TIBPAL20R8-5C HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

## electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS	TIBPAL20R8-5CFN			TIBPAL20R8-5CJT TIBPAL20R8-5CNT			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 4.75\text{ V}$ , $I_I = -18\text{ mA}$	-0.8		-1.5	-0.8		-1.5	V
$V_{OH}$	$V_{CC} = 4.75\text{ V}$ , $I_{OH} = -3.2\text{ mA}$	2.4	2.7		2.4	2.7		V
$V_{OL}$	$V_{CC} = 4.75\text{ V}$ , $I_{OL} = 24\text{ mA}$		0.3	0.5		0.3	0.5	V
$I_{OZH}$	$V_{CC} = 5.25\text{ V}$ , $V_O = 2.7\text{ V}$			100			100	μA
$I_{OZL}$	$V_{CC} = 5.25\text{ V}$ , $V_O = 0.4\text{ V}$			-100			-100	μA
$I_I$	$V_{CC} = 5.25\text{ V}$ , $V_I = 5.5\text{ V}$			100			100	μA
$I_{IH}$	$V_{CC} = 5.25\text{ V}$ , $V_I = 2.7\text{ V}$			25			25	μA
$I_{IL}$	$V_{CC} = 5.25\text{ V}$ , $V_I = 0.4\text{ V}$			-250			-250	μA
$I_{OS}^\ddagger$	$V_{CC} = 5.25\text{ V}$ , $V_O = 0.5\text{ V}$	-30	-70	-130	-30	-70	-130	mA
$I_{CC}$	$V_{CC} = 5.25\text{ V}$ , $V_I = 0$ , Outputs open			210			210	mA
$C_i$	$I$		8.5			6.5		pF
	$\overline{\text{CLK/OE}}$		7.5			5.5		
$C_o$	$f = 1\text{ MHz}$ , $V_O = 2\text{ V}$		10			8		pF

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)		TO (OUTPUT)		TEST CONDITIONS	TIBPAL20R8-5CFN			TIBPAL20R8-5CJT TIBPAL20R8-5CNT			UNIT	
						MIN	TYP†	MAX	MIN	TYP†	MAX		
f <sub>max</sub> <sup>§</sup>	without feedback				R1 = 200 Ω, R2 = 200 Ω, See Figure 8	125			125			MHz	
	with internal feedback (counter configuration)					125			125				
	with external feedback					117			111				
t <sub>pd</sub>	CLK↑	Q	with up to 4 outputs switching			1.5			4	1.5		4	ns
	CLK↑	Q	with more than 4 outputs switching			1.5			4	1.5		4.5	
t <sub>pd</sub> <sup>¶</sup>	CLK↑	Internal feedback				3.5			3.5			ns	
t <sub>en</sub>	OE↓	Q				1.5			6	1.5		6	ns
t <sub>dis</sub>	OE↑	Q				1			6.5	1		7	ns
t <sub>r</sub>						1.5			1.5			ns	
t <sub>f</sub>					1.5			1.5			ns		
t <sub>sk(o)</sub> <sup>#</sup>	Skew between outputs				0.5			0.5			ns		

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.  $V_O$  is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

§ See 'f<sub>max</sub> Specification' near the end of this data sheet.

¶ This parameter is calculated from the measured  $f_{\max}$  with internal feedback in a counter configuration (see Figure 4 for illustration).

#  $t_{sk(o)}$  is the skew time between registered outputs.

# TIBPAL20L8-7M, TIBPAL20R4-7M, TIBPAL20R6-7M, TIBPAL20R8-7M HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	–55°C to 125°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

## recommended operating conditions

	MIN	NOM	MAX	UNIT
$V_{CC}$ Supply voltage	4.5	5	5.5	V
$V_{IH}$ High-level input voltage (see Note 2)	2		5.5	V
$V_{IL}$ Low-level input voltage (see Note 2)			0.8	V
$I_{OH}$ High-level output current			–2	mA
$I_{OL}$ Low-level output current			12	mA
$f_{clock}^{\dagger}$ Clock frequency	0		100	MHz
$t_w^{\dagger}$ Pulse duration, clock	High		5	ns
	Low		5	
$t_{su}^{\dagger}$ Setup time, input or feedback before clock $\uparrow$	7			ns
$t_h^{\dagger}$ Hold time, input or feedback after clock $\uparrow$	0			ns
$T_A$ Operating free-air temperature	–55	25	125	°C

$^{\dagger} f_{clock}$ ,  $t_w$ ,  $t_{su}$ , and  $t_h$  do not apply to TIBPAL16L8'

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

PRODUCT PREVIEW

# TIBPAL20L8-7M, TIBPAL20R4-7M, TIBPAL20R6-7M, TIBPAL20R8-7M HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

## electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$		$V_{CC} = 4.5\text{ V}$ ,	$I_I = -18\text{ mA}$		-0.8	-1.5	V
$V_{OH}$		$V_{CC} = 4.5\text{ V}$ ,	$I_{OH} = -2\text{ mA}$	2.4	2.7		V
$V_{OL}$		$V_{CC} = 4.5\text{ V}$ ,	$I_{OL} = 12\text{ mA}$		0.25	0.5	V
$I_{OZH}$	0, Q outputs	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 2.7\text{ V}$			20	$\mu\text{A}$
	I/O ports					100	
$I_{OZL}$	0, Q outputs	$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0.4\text{ V}$			-20	$\mu\text{A}$
	I/O ports					-250	
$I_I$		$V_{CC} = 5.5\text{ V}$ ,	$V_I = 5.5\text{ V}$			1	mA
$I_{IH}$	I/O ports	$V_{CC} = 5.5\text{ V}$ ,	$V_I = 2.7\text{ V}$			100	$\mu\text{A}$
	All others					25	
$I_{IL}$		$V_{CC} = 5.5\text{ V}$ ,	$V_I = 0.4\text{ V}$			-250	$\mu\text{A}$
$I_{OS}^\ddagger$		$V_{CC} = 5.5\text{ V}$ ,	$V_O = 0.5\text{ V}$	-30	-70	-130	mA
$I_{CC}$		$V_{CC} = 5.5\text{ V}$ ,	$V_I = \text{GND}$ , $\overline{\text{OE}} = V_{IH}$ , Outputs open			220	mA
$C_i$	I	$f = 1\text{ MHz}$ ,	$V_I = 2\text{ V}$			8.5	pF
	CLK/ $\overline{\text{OE}}$					7.5	
$C_o$		$f = 1\text{ MHz}$ ,	$V_O = 2\text{ V}$			10	pF

† All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.  $V_O$  is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	MAX	UNIT
f <sub>max</sub> <sup>§</sup>	without feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 8	100		MHz
	with internal feedback (counter configuration)			100		
	with external feedback			74		
t <sub>pd</sub>	I, I/O	O, I/O		1	7	ns
t <sub>pd</sub>	CLK	Q		1	7	ns
t <sub>en</sub>	OE↓	Q		1	8	ns
t <sub>dis</sub>	OE↑	Q		1	10	ns
t <sub>en</sub>	I, I/O	O, I/O		1	9	ns
t <sub>dis</sub>	I, I/O	O, I/O		1	10	ns

§ See 'f<sub>max</sub> Specification' near the end of this data sheet. f<sub>max</sub> does not apply for TIBPAL20L8'. f<sub>max</sub> with external feedback is not production tested and is calculated from the equation found in the f<sub>max</sub> specifications section.

PRODUCT PREVIEW

**TIBPAL20L8-5C, TIBPAL20R4-5C, TIBPAL20R6-5C, TIBPAL20R8-5C  
TIBPAL20L8-7M, TIBPAL20R4-7M, TIBPAL20R6-7M, TIBPAL20R8-7M  
HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS**

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

## programming information

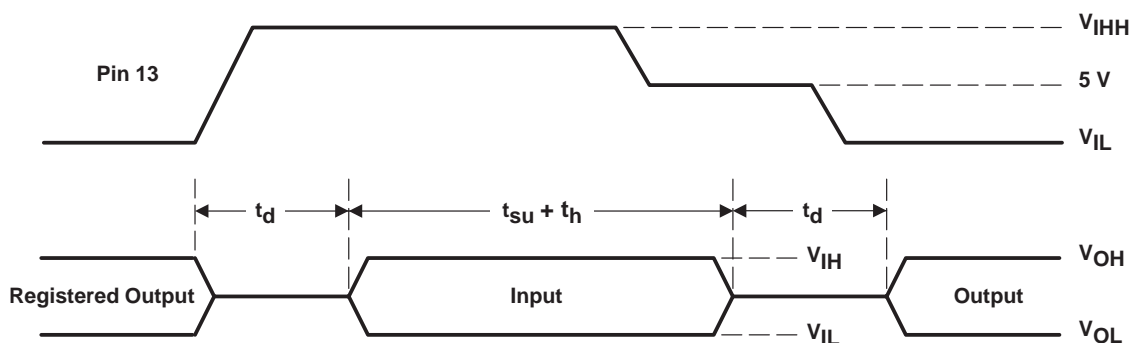
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

## asynchronous preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

- Step 1. With  $V_{CC}$  at 5 volts and Pin 1 at  $V_{IL}$ , raise Pin 13 to  $V_{IHH}$ .
- Step 2. Apply either  $V_{IL}$  or  $V_{IH}$  to the output corresponding to the register to be preloaded.
- Step 3. Lower Pin 13 to 5 V.
- Step 4. Remove output voltage, then lower Pin 13 to  $V_{IL}$ . Preload can be verified by observing the voltage level at the output pin.



**Figure 1. Asynchronous Preload Waveforms**

NOTE 3:  $t_d = t_{su} = t_h = 100$  ns to 1000 ns,  $V_{IHH} = 10.25$  V to 10.75 V

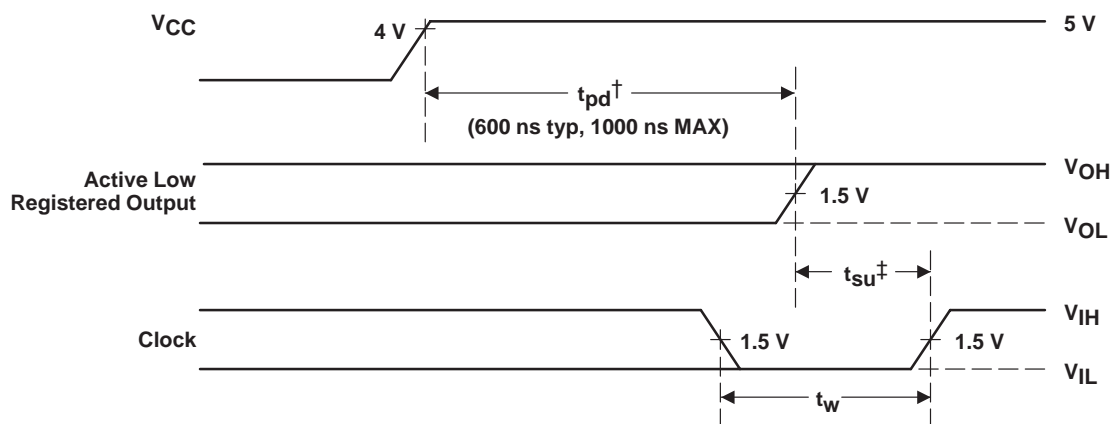


TIBPAL20L8-5C, TIBPAL20R4-5C, TIBPAL20R6-5C, TIBPAL20R8-5C  
TIBPAL20L8-7M, TIBPAL20R4-7M, TIBPAL20R6-7M, TIBPAL20R8-7M  
HIGH-PERFORMANCE *IMPACT-X*<sup>™</sup> PAL<sup>®</sup> CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

**power-up reset, see Figure 2**

Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of  $V_{CC}$  be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



<sup>†</sup> This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.

<sup>‡</sup> This is the setup time for input or feedback.

**Figure 2. Power-Up Reset Waveforms**

## $f_{\max}$ SPECIFICATIONS

### $f_{\max}$ without feedback, see Figure 3

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time ( $t_{su} + t_h$ ). However, the minimum  $f_{\max}$  is determined by the minimum clock period ( $t_{w\text{ high}} + t_{w\text{ low}}$ ).

Thus,  $f_{\max}$  without feedback =  $\frac{1}{(t_{w\text{ high}} + t_{w\text{ low}})}$  or  $\frac{1}{(t_{su} + t_h)}$ .

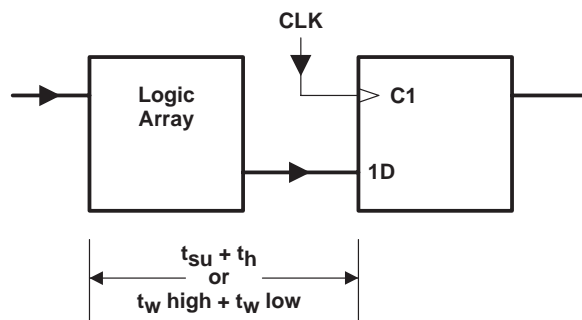


Figure 3.  $f_{\max}$  Without Feedback

### $f_{\max}$ with internal feedback, see Figure 4

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

Thus,  $f_{\max}$  with internal feedback =  $\frac{1}{(t_{su} + t_{pd\text{ CLK-to-FB}})}$ .

Where  $t_{pd\text{ CLK-to-FB}}$  is the deduced value of the delay from CLK to the input of the logic array.

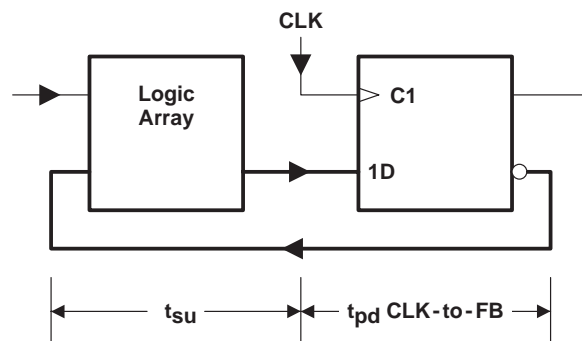


Figure 4.  $f_{\max}$  With Internal Feedback

## $f_{\max}$ SPECIFICATIONS

### $f_{\max}$ with external feedback, see Figure 5

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals ( $t_{su} + t_{pd} \text{ CLK-to-Q}$ ).

Thus,  $f_{\max}$  with external feedback =  $\frac{1}{(t_{su} + t_{pd} \text{ CLK-to-Q})}$ .

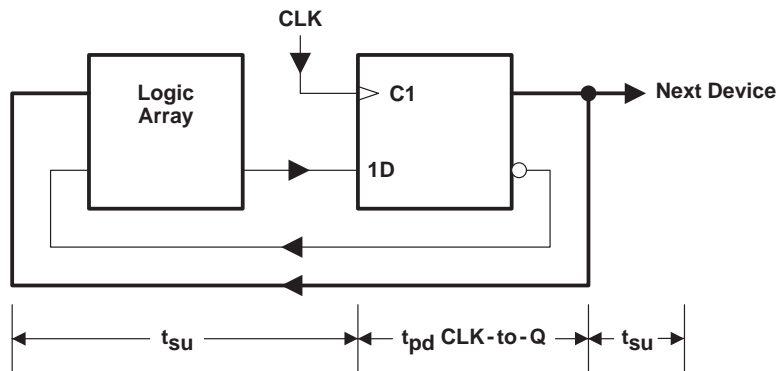


Figure 5.  $f_{\max}$  With External Feedback

# TIBPAL20R8-5C HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

## THERMAL INFORMATION

### thermal management of the TIBPAL20R8-5C

Thermal management of the TIBPAL20R8-5CNT and TIBPAL20R8-5CFN is necessary when operating at certain conditions of frequency, output loading, and outputs switching simultaneously. The device and system application will determine the appropriate level of management.

Determining the level of thermal management is based on factors such as power dissipation ( $P_D$ ), ambient temperature ( $T_A$ ), and transverse airflow (FPM). Figures 6 (a) and 6 (b) show the relationship between ambient temperature and transverse airflow at given power dissipation levels. The required transverse airflow can be determined at a particular ambient temperature and device power dissipation level in order to ensure the device specifications.

Figure 7 illustrates how power dissipation varies as a function of frequency and the number of outputs switching simultaneously. It should be noted that all outputs are fully loaded ( $C_L = 50$  pF). Since the condition of eight fully loaded outputs represents the worst-case condition, each application must be evaluated accordingly.

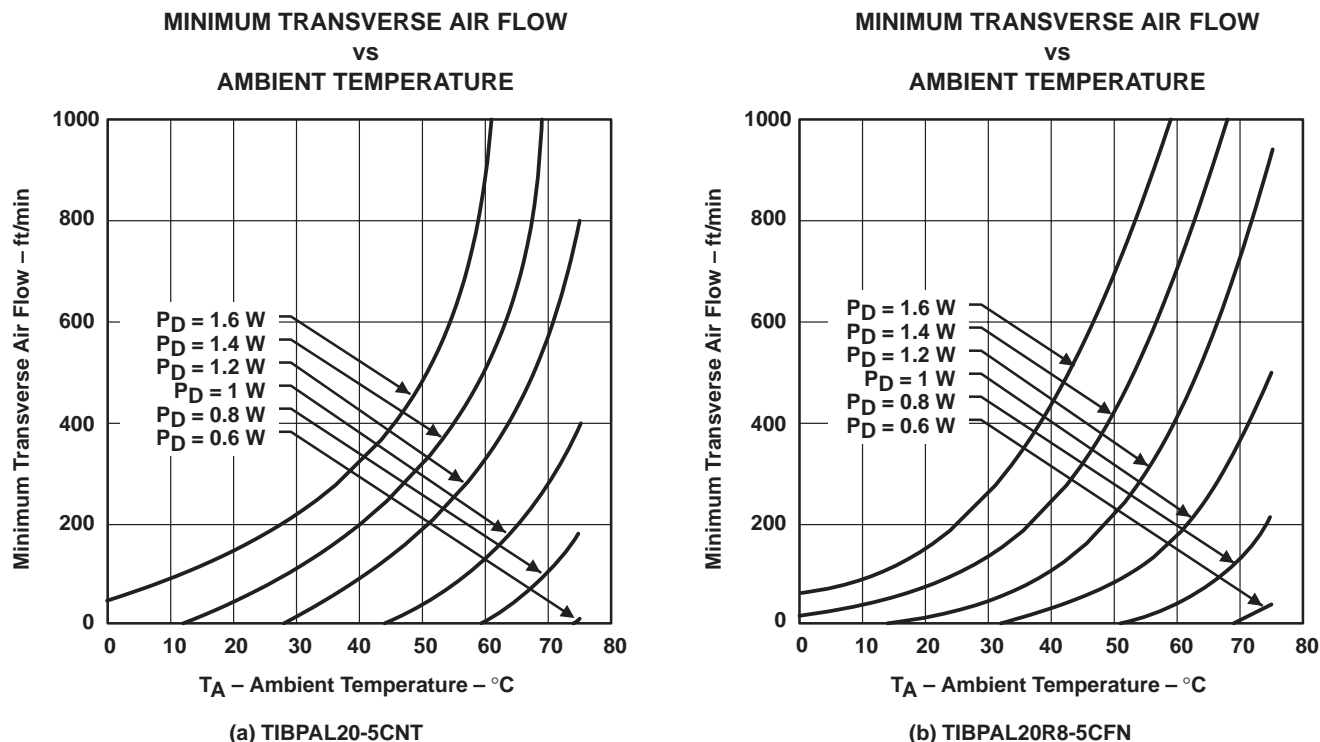


Figure 6

## THERMAL INFORMATION

### POWER DISSIPATION vs FREQUENCY

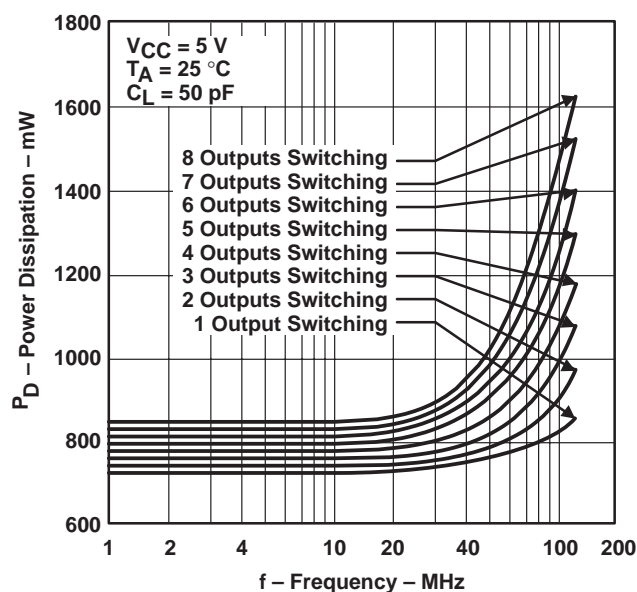
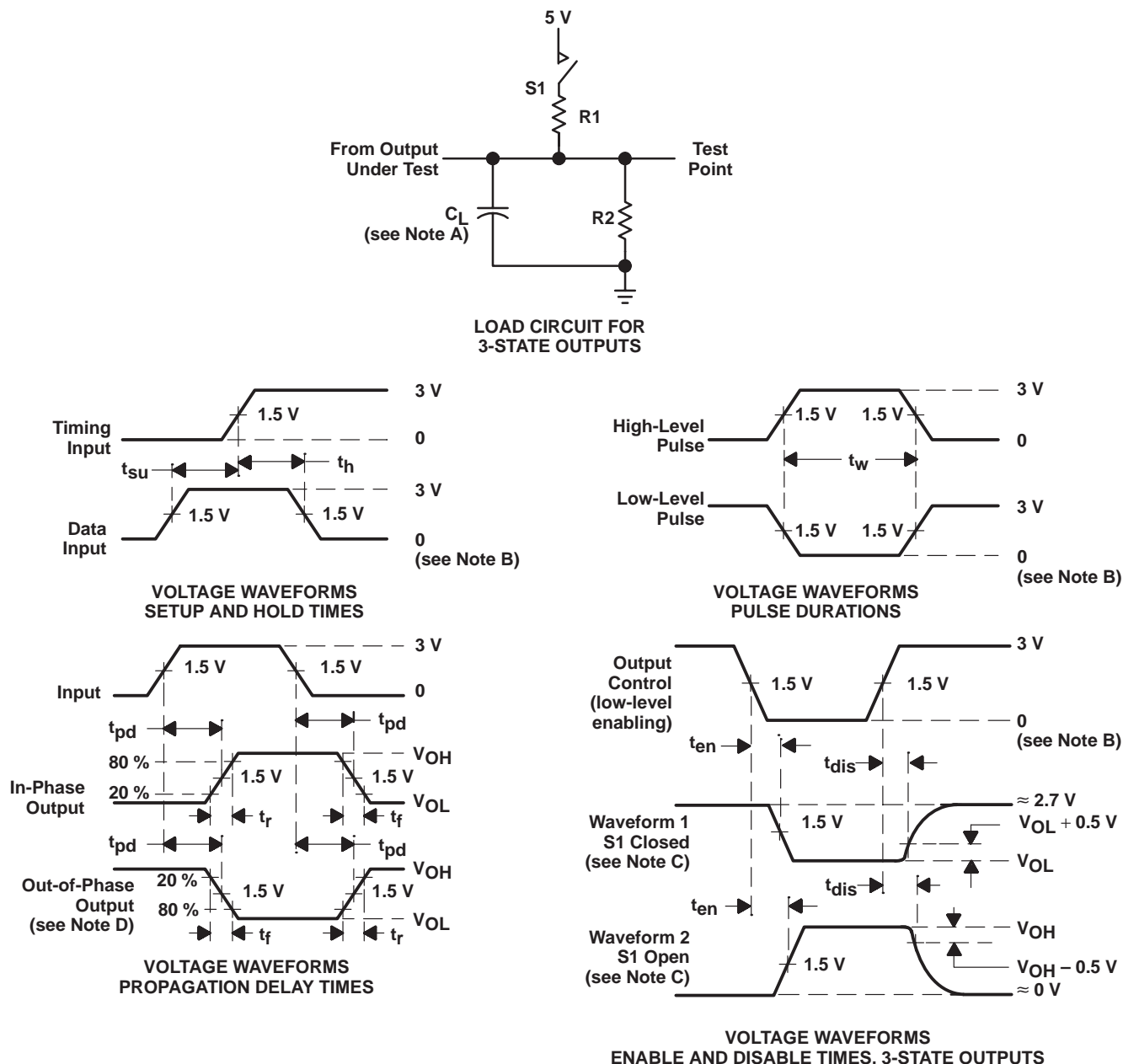


Figure 7

TIBPAL20L8-5C, TIBPAL20R4-5C, TIBPAL20R6-5C, TIBPAL20R8-5C  
TIBPAL20L8-7M, TIBPAL20R4-7M, TIBPAL20R6-7M, TIBPAL20R8-7M  
HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance and is 50 pF for  $t_{pd}$  and  $t_{en}$ , 5 pF for  $t_{dis}$ .  
B. All input pulses have the following characteristics: For C suffix,  $PRR \leq 1$  MHz,  $t_r = t_f = 2$  ns, duty cycle = 50%; For M suffix,  $PRR \leq 10$  MHz,  $t_r = t_f \leq 2$  ns, duty cycle = 50%.  
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.  
E. Equivalent loads may be used for testing.

Figure 8. Load Circuit and Voltage Waveforms

# TIBPAL20R4-5C, TIBPAL20R6-5C, TIBPAL20R8-5C HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

## metastable characteristics of TIBPAL20R4-5C, TIBPAL20R6-5C, and TIBPAL20R8-5C

At some point a system designer is faced with the problem of synchronizing two digital signals operating at two different frequencies. This problem is typically overcome by synchronizing one of the signals to the local clock through use of a flip-flop. However, this solution presents an awkward dilemma since the setup and hold time specifications associated with the flip-flop are sure to be violated. The metastable characteristics of the flip-flop can influence overall system reliability.

Whenever the setup and hold times of a flip-flop are violated, its output response becomes uncertain and is said to be in the metastable state if the output hangs up in the region between  $V_{IL}$  and  $V_{IH}$ . This metastable condition lasts until the flip-flop falls into one of its two stable states, which takes longer than the specified maximum propagation delay time (CLK to Q max).

From a system engineering standpoint, a designer cannot use the specified data sheet maximum for propagation delay time when using the flip-flop as a data synchronizer – how long to wait after the specified data sheet maximum must be known before using the data in order to guarantee reliable system operation.

The circuit shown in Figure 9 can be used to evaluate MTBF (Mean Time Between Failure) and  $\Delta t$  for a selected flip-flop. Whenever the Q output of the DUT is between 0.8 V and 2 V, the comparators are in opposite states. When the Q output of the DUT is higher than 2 V or lower than 0.8 V, the comparators are at the same logic level. The outputs of the two comparators are sampled a selected time ( $\Delta t$ ) after SCLK. The exclusive OR gate detects the occurrence of a failure and increments the failure counter.

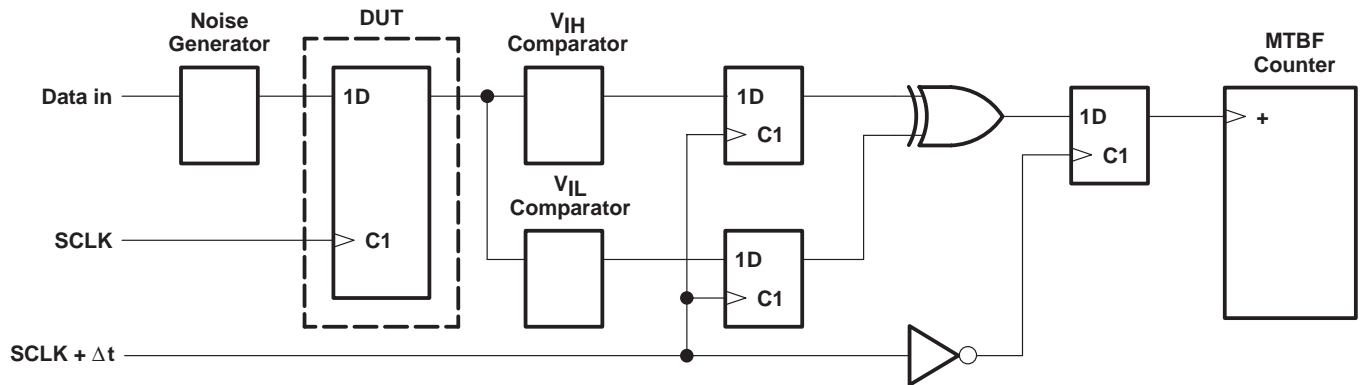


Figure 9. Metastable Evaluation Test Circuit

In order to maximize the possibility of forcing the DUT into a metastable state, the input data signal is applied so that it always violates the setup and hold time. This condition is illustrated in the timing diagram in Figure 10. Any other relationship of SCLK to data will provide less chance for the device to enter into the metastable state.

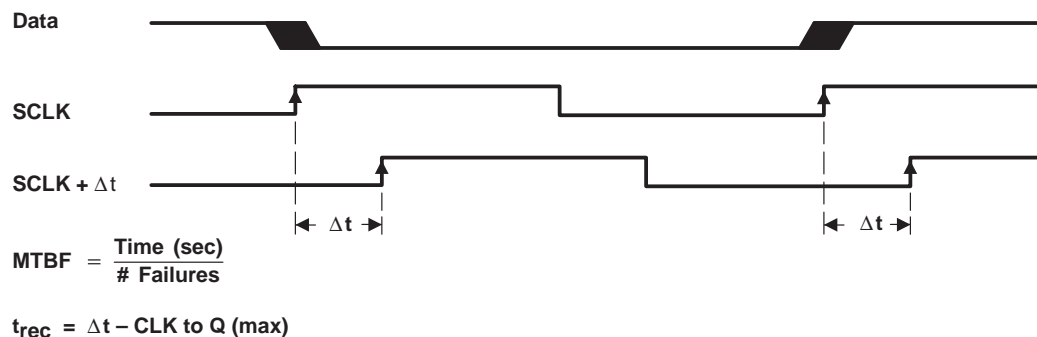
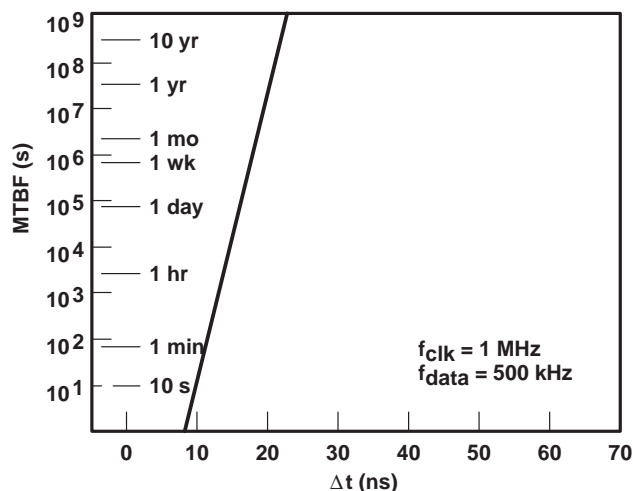


Figure 10. Timing Diagram

# TIBPAL20R4-5C, TIBPAL20R6-5C, TIBPAL20R8-5C HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

By using the described test circuit, MTBF can be determined for several different values of  $\Delta t$  (see Figure 9). Plotting this information on semilog scale demonstrates the metastable characteristics of the selected flip-flop. Figure 11 shows the results for the TIBPAL20'-5C operating at 1 MHz.



**Figure 11. Metastable Characteristics**

From the data taken in the above experiment, an equation can be derived for the metastable characteristics at other clock frequencies.

The metastable equation:  $\frac{1}{\text{MTBF}} = f_{\text{SCLK}} \times f_{\text{data}} \times C1 \times e^{(-C2 \times \Delta t)}$

The constants C1 and C2 describe the metastable characteristics of the device. From the experimental data, these constants can be solved for:  $C1 = 4.37 \times 10^{-3}$  and  $C2 = 2.01$

Therefore

$$\frac{1}{\text{MTBF}} = f_{\text{SCLK}} \times f_{\text{data}} \times 4.37 \times 10^{-3} \times e^{(-2.01 \times \Delta t)}$$

## definition of variables

**DUT (Device Under Test):** The DUT is a 5-ns registered PLD programmed with the equation  $Q : = D$ .

**MTBF (Mean Time Between Failures):** The average time (s) between metastable occurrences that cause a violation of the device specifications.

**$f_{\text{SCLK}}$  (system clock frequency):** Actual clock frequency for the DUT.

**$f_{\text{data}}$  (data frequency):** Actual data frequency for a specified input to the DUT.

**C1:** Calculated constant that defines the magnitude of the curve.

**C2:** Calculated constant that defines the slope of the curve.

**$t_{\text{rec}}$  (metastability recovery time):** Minimum time required to guarantee recovery from metastability, at a given MTBF failure rate.  $t_{\text{rec}} = \Delta t - t_{\text{pd}}$  (CLK to Q, max)

**$\Delta t$ :** The time difference (ns) from when the synchronizing flip-flop is clocked to when its output is sampled.

The test described above has shown the metastable characteristics of the TIBPAL20R4/R6/R8-5C series. For additional information on metastable characteristics of Texas Instruments logic circuits, please refer to TI Applications publication SDAA004, "Metastable Characteristics, Design Considerations for ALS, AS, and LS Circuits."



TIBPAL20L8-5C, TIBPAL20R4-5C, TIBPAL20R6-5C, TIBPAL20R8-5C  
TIBPAL20L8-7M, TIBPAL20R4-7M, TIBPAL20R6-7M, TIBPAL20R8-7M  
HIGH-PERFORMANCE *IMPACT-X*<sup>™</sup> PAL<sup>®</sup> CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

TYPICAL CHARACTERISTICS

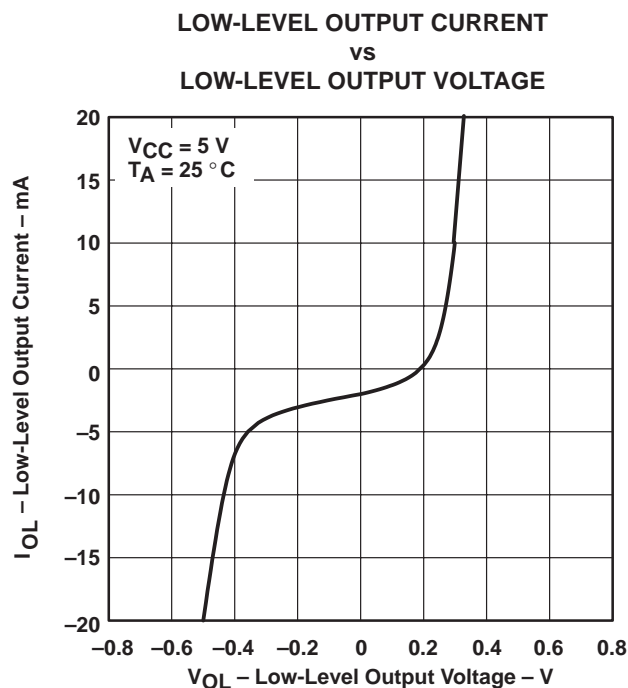


Figure 12

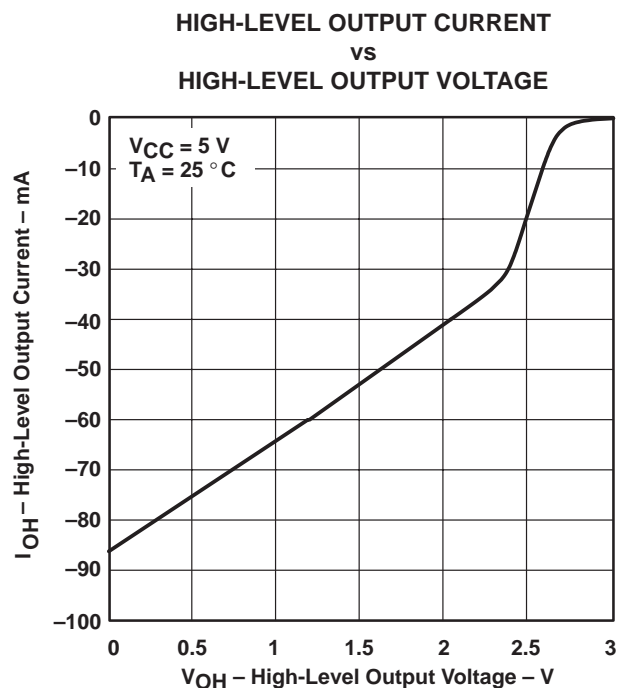


Figure 13

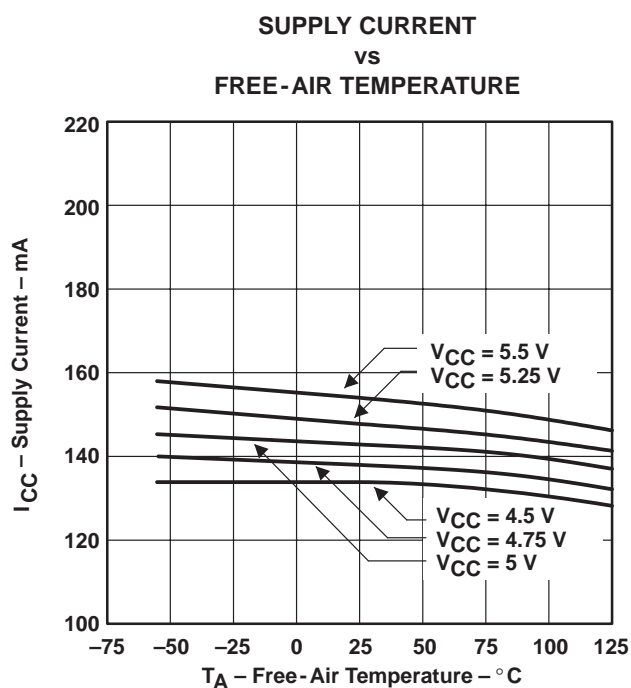


Figure 14

TIBPAL20L8-5C, TIBPAL20R4-5C, TIBPAL20R6-5C, TIBPAL20R8-5C  
TIBPAL20L8-7M, TIBPAL20R4-7M, TIBPAL20R6-7M, TIBPAL20R8-7M  
HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

# TYPICAL CHARACTERISTICS

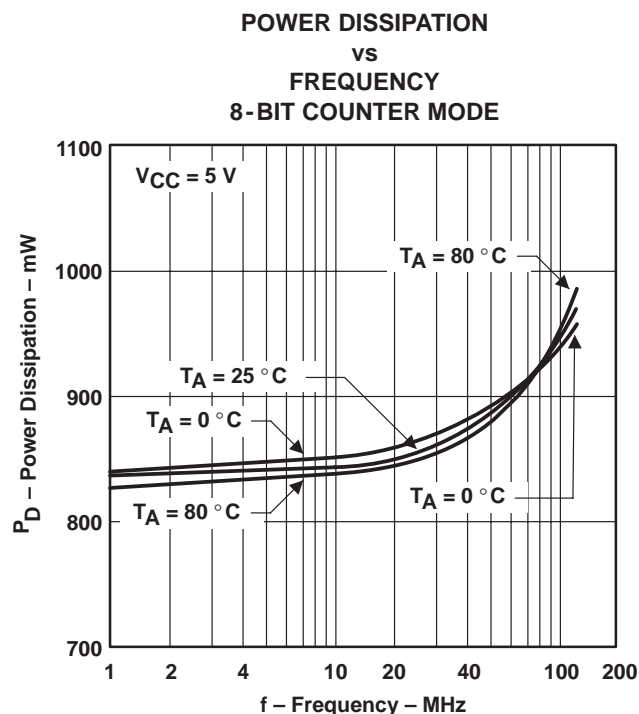


Figure 15

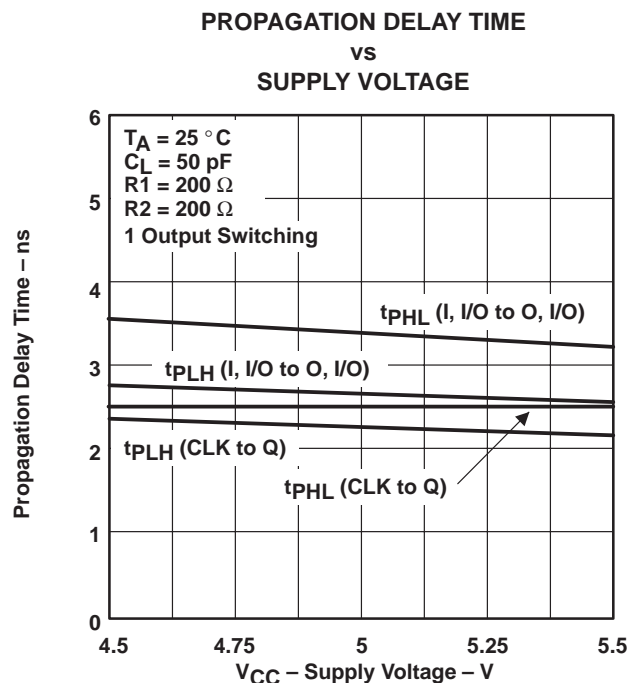


Figure 16

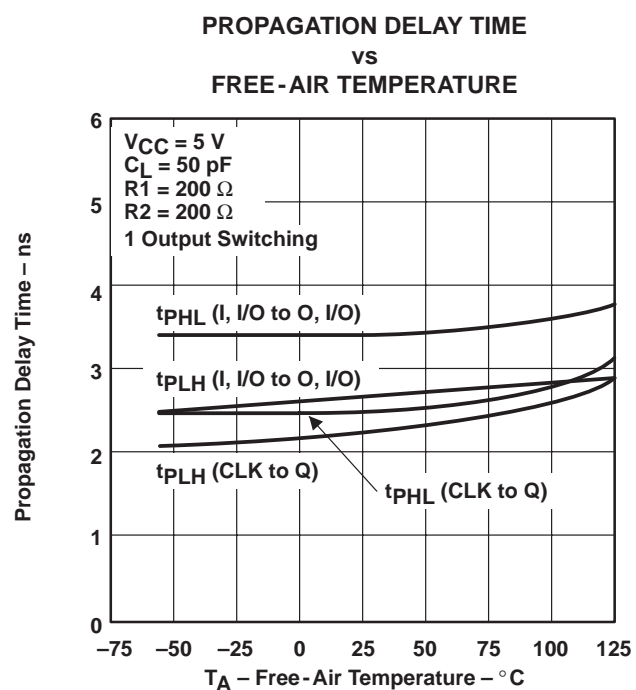


Figure 17

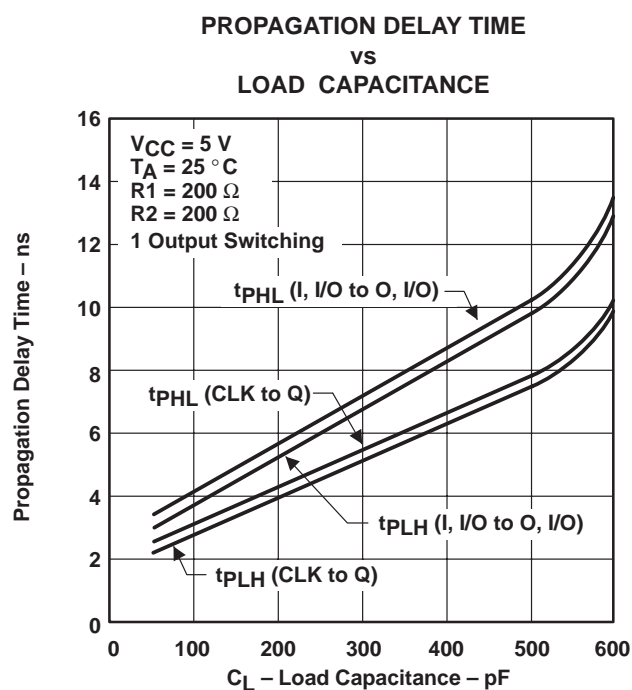


Figure 18

## TYPICAL CHARACTERISTICS

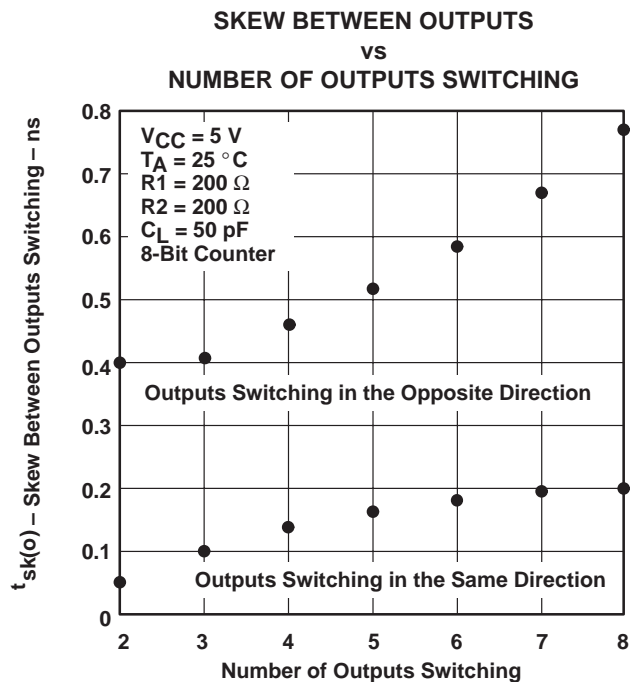


Figure 19

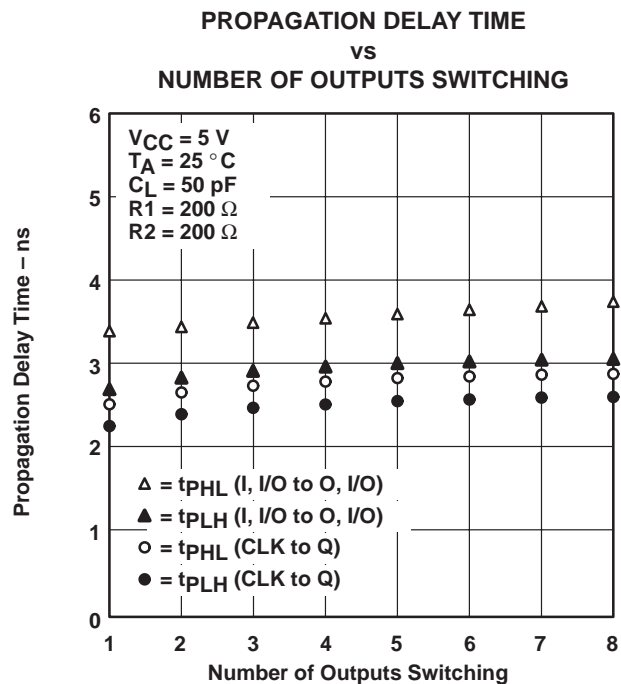


Figure 20

# TI North American Sales Offices

**ALABAMA:** Huntsville: (205) 837-7530  
**ARIZONA:** Phoenix: (602) 995-1007  
**CALIFORNIA:** Irvine: (714) 660-1200  
San Diego: (619) 278-9600  
Santa Clara: (408) 980-9000  
Woodland Hills: (818) 704-8100  
**COLORADO:** Aurora: (303) 368-8000  
**CONNECTICUT:** Wallingford: (203) 269-0074  
**FLORIDA:** Altamonte Springs: (407) 260-2116  
Fort Lauderdale: (305) 973-8502  
Tampa: (813) 885-7588  
**GEORGIA:** Norcross: (404) 662-7967  
**ILLINOIS:** Arlington Heights: (708) 640-3000  
**INDIANA:** Carmel: (317) 573-6400  
Fort Wayne: (219) 489-4697  
**KANSAS:** Overland Park: (913) 451-4511  
**MARYLAND:** Columbia: (410) 964-2003  
**MASSACHUSETTS:** Waltham: (617) 895-9100  
**MICHIGAN:** Farmington Hills: (313) 553-1581  
**MINNESOTA:** Eden Prairie: (612) 828-9300  
**MISSOURI:** St. Louis: (314) 821-8400  
**NEW JERSEY:** Iselin: (908) 750-1050  
**NEW MEXICO:** Albuquerque: (505) 345-2555  
**NEW YORK:** East Syracuse: (315) 463-9291  
Fishkill: (914) 897-2900  
Melville: (516) 454-6600  
Pittsford: (716) 385-6770  
**NORTH CAROLINA:** Charlotte: (704) 527-0930  
Raleigh: (919) 876-2725  
**OHIO:** Beachwood: (216) 765-7258  
Beavercreek: (513) 427-6200  
**OREGON:** Beaverton: (503) 643-6758  
**PENNSYLVANIA:** Blue Bell: (215) 825-9500  
**PUERTO RICO:** Hato Rey: (809) 753-8700  
**TEXAS:** Austin: (512) 250-6769  
Dallas: (214) 917-1264  
Houston: (713) 778-6592  
Midland: (915) 561-7137  
**UTAH:** Salt Lake City: (801) 466-8972  
**WISCONSIN:** Waukesha: (414) 798-1001  
**CANADA:** Nepean: (613) 726-1970  
Richmond Hill: (416) 884-9181  
St. Laurent: (514) 335-8392

# TI Regional Technology Centers

**CALIFORNIA:** Irvine: (714) 660-8140  
Santa Clara: (408) 748-2222  
**GEORGIA:** Norcross: (404) 662-7945  
**ILLINOIS:** Arlington Heights: (708) 640-2909  
**INDIANA:** Indianapolis: (317) 573-6400  
**MASSACHUSETTS:** Waltham: (617) 895-9196  
**MEXICO:** Mexico City: 491-70834  
**MINNESOTA:** Minneapolis: (612) 828-9300  
**TEXAS:** Dallas: (214) 917-3881  
**CANADA:** Nepean: (613) 726-1970

## Customer Response Center

**TOLL FREE:** (800) 336-5236  
**OUTSIDE USA:** (214) 995-6611  
(8:00 a.m. – 5:00 p.m. CST)

# TI Authorized North American Distributors

Alliance Electronics, Inc. (military product only)  
Almac/Arrow  
Anthem Electronics  
Arrow/Schweber  
Future Electronics (Canada)  
GRS Electronics Co., Inc.  
Hall-Mark Electronics  
Marshall Industries  
Newark Electronics  
Rochester Electronics, Inc.  
(obsolete product only (508) 462-9332)  
Wyle Laboratories  
Zeus Components

# TI Distributors

**ALABAMA:** Arrow/Schweber (205) 837-6955; Hall-Mark (205) 837-8700; Marshall (205) 881-9235.  
**ARIZONA:** Anthem (602) 966-6600; Arrow/Schweber (602) 437-0750; Hall-Mark (602) 431-0030; Marshall (602) 496-0290; Wyle (602) 437-2088.  
**CALIFORNIA:** Los Angeles/Orange County: Anthem (818) 775-1333, (714) 768-4444; Arrow/Schweber (818) 380-9686, (714) 838-5422; Hall-Mark (818) 773-4500, (714) 727-6000; Marshall (818) 878-7000, (714) 458-5301; Wyle (818) 880-9000, (714) 863-9953; Zeus (714) 921-9000, (818) 889-3838;  
**Sacramento:** Anthem (916) 624-9744; Hall-Mark (916) 624-9781; Marshall (916) 635-9700; Wyle (916) 638-5282;  
**San Diego:** Anthem (619) 453-9005; Arrow/Schweber (619) 565-4800; Hall-Mark (619) 268-1201; Marshall (619) 578-9600; Wyle (619) 565-9171; Zeus (619) 277-9681.  
**San Francisco Bay Area:** Anthem (408) 453-1200; Arrow/Schweber (408) 441-9700, (510) 490-9477; Hall-Mark (408) 432-4000; Marshall (408) 942-4600; Wyle (408) 727-2500; Zeus (408) 629-4789.  
**COLORADO:** Anthem (303) 790-4500; Arrow/Schweber (303) 799-0258; Hall-Mark (303) 790-1662; Marshall (303) 451-8383; Wyle (303) 457-9953.  
**CONNECTICUT:** Anthem (203) 575-1575; Arrow/Schweber (203) 265-7741; Hall-Mark (203) 271-2844; Marshall (203) 265-3822.  
**FLORIDA:** Fort Lauderdale: Arrow/Schweber (305) 429-8200; Hall-Mark (305) 971-9280; Marshall (305) 977-4880.  
**Orlando:** Arrow/Schweber (407) 333-9300; Hall-Mark (407) 830-5855; Marshall (407) 767-8585; Zeus (407) 788-9100.  
**Tampa:** Hall-Mark (813) 541-7440; Marshall (813) 573-1399.  
**GEORGIA:** Arrow/Schweber (404) 497-1300; Hall-Mark (404) 623-4400; Marshall (404) 923-5750.  
**ILLINOIS:** Anthem (708) 884-0200; Arrow/Schweber (708) 250-0500; Hall-Mark (312) 860-3800; Marshall (708) 490-0155; Newark (312) 784-5100.  
**INDIANA:** Arrow/Schweber (317) 299-2071; Hall-Mark (317) 872-8875; Marshall (317) 297-0483.  
**IOWA:** Arrow/Schweber (319) 395-7230.  
**KANSAS:** Arrow/Schweber (913) 541-9542; Hall-Mark (913) 888-4747; Marshall (913) 492-3121.  
**MARYLAND:** Anthem (301) 995-6640; Arrow/Schweber (301) 596-7800; Hall-Mark (301) 988-9800; Marshall (301) 622-1118; Zeus (301) 997-1118.  
**MASSACHUSETTS:** Anthem (508) 657-5170; Arrow/Schweber (508) 658-0900; Hall-Mark (508) 667-0902; Marshall (508) 658-0810; Wyle (617) 272-7300; Zeus (617) 246-8200.

**MICHIGAN:** Detroit: Arrow/Schweber (313) 462-2290; Hall-Mark (313) 416-5800; Marshall (313) 525-5850; Newark (313) 967-0600.  
**MINNESOTA:** Anthem (612) 944-5454; Arrow/Schweber (612) 941-5280; Hall-Mark (612) 881-2600; Marshall (612) 559-2211.  
**MISSOURI:** Arrow/Schweber (314) 567-6888; Hall-Mark (314) 291-5350; Marshall (314) 291-4650.  
**NEW JERSEY:** Anthem (201) 227-7960; Arrow/Schweber (201) 227-7880, (609) 596-8000; Hall-Mark (201) 515-3000, (609) 235-1900; Marshall (201) 882-0320, (609) 234-9100.  
**NEW MEXICO:** Alliance (505) 292-3360.  
**NEW YORK: Long Island:** Anthem (516) 864-6600; Arrow/Schweber (516) 231-1000; Hall-Mark (516) 737-0600; Marshall (516) 273-2424; Zeus (914) 937-7400.  
**Rochester:** Arrow/Schweber (716) 427-0300; Hall-Mark (716) 425-3300; Marshall (716) 235-7620.  
**Syracuse:** Marshall (607) 785-2345.  
**NORTH CAROLINA:** Arrow/Schweber (919) 876-3132; Hall-Mark (919) 872-0712; Marshall (919) 878-9882.  
**OHIO: Cleveland:** Arrow/Schweber (216) 248-3990; Hall-Mark (216) 349-4632; Marshall (216) 248-1788.  
**Columbus:** Hall-Mark (614) 888-3313.  
**Dayton:** Arrow/Schweber (513) 435-5563; Marshall (513) 898-4480; Zeus (513) 293-6162.  
**OKLAHOMA:** Arrow/Schweber (918) 252-7537; Hall-Mark (918) 254-6110.  
**OREGON:** Almac/Arrow (503) 629-8090; Anthem (503) 643-1114; Marshall (503) 644-5050; Wyle (503) 643-7900.  
**PENNSYLVANIA:** Anthem (215) 443-5150; Arrow/Schweber (215) 928-1800; GRS (215) 922-7037; (609) 964-8560; Marshall (412) 788-0441.  
**TEXAS: Austin:** Arrow/Schweber (512) 835-4180; Hall-Mark (512) 258-8848; Marshall (512) 837-1991; Wyle (512) 345-8853;  
**Dallas:** Anthem (214) 238-7100; Arrow/Schweber (214) 380-6464; Hall-Mark (214) 553-4300; Marshall (214) 233-5200; Wyle (214) 235-9953; Zeus (214) 783-7010;  
**Houston:** Arrow/Schweber (713) 530-4700; Hall-Mark (713) 781-6100; Marshall (713) 467-1666; Wyle (713) 879-9953.  
**UTAH:** Anthem (801) 973-8555; Arrow/Schweber (801) 973-6913; Marshall (801) 973-2288; Wyle (801) 974-9953.  
**WASHINGTON:** Almac/Arrow (206) 643-9992; Anthem (206) 483-1700; Marshall (206) 486-5747; Wyle (206) 881-1150.  
**WISCONSIN:** Arrow/Schweber (414) 792-0150; Hall-Mark (414) 797-7844; Marshall (414) 797-8400.  
**CANADA: Calgary:** Future (403) 235-5325;  
**Edmonton:** Future (403) 438-2858;  
**Montreal:** Arrow/Schweber (514) 421-7411; Future (514) 694-7710; Marshall (514) 694-8142  
**Ottawa:** Arrow/Schweber (613) 226-6903; Future (613) 820-8313.  
**Quebec:** Future (418) 897-6666.  
**Toronto:** Arrow/Schweber (416) 670-7769; Future (416) 612-9200; Marshall (416) 458-8046.  
**Vancouver:** Arrow/Schweber (604) 421-2333; Future (604) 294-1166.

## TI Die Processors

Chip Supply	(407) 298-7100
Elmo Semiconductor	(818) 768-7400
Minco Technology Labs	(512) 834-2022



D0892

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
5962-87671193A	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Level-NC-NC-NC
5962-8767119KA	ACTIVE	CFP	W	24	1	TBD	Call TI	Level-NC-NC-NC
5962-8767119LA	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
TIBPAL20L8-5CFN	ACTIVE	PLCC	FN	28	37	TBD	Call TI	Level-1-220-UNLIM
TIBPAL20L8-5CNT	ACTIVE	PDIP	NT	24	15	TBD	Call TI	Level-NC-NC-NC
TIBPAL20R4-5CFN	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI
TIBPAL20R4-5CNT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
TIBPAL20R6-5CFN	ACTIVE	PLCC	FN	28	37	TBD	Call TI	Level-1-220-UNLIM
TIBPAL20R6-5CNT	ACTIVE	PDIP	NT	24	15	TBD	Call TI	Level-NC-NC-NC
TIBPAL20R8-5CFN	OBSOLETE	PLCC	FN	28		TBD	Call TI	Call TI
TIBPAL20R8-5CNT	OBSOLETE	PDIP	NT	24		TBD	Call TI	Call TI
TIBPAL20R8-7MFKB	ACTIVE	LCCC	FK	28	1	TBD	Call TI	Level-NC-NC-NC
TIBPAL20R8-7MJTB	ACTIVE	CDIP	JT	24	1	TBD	Call TI	Level-NC-NC-NC
TIBPAL20R8-7MWB	ACTIVE	CFP	W	24	1	TBD	Call TI	Level-NC-NC-NC

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

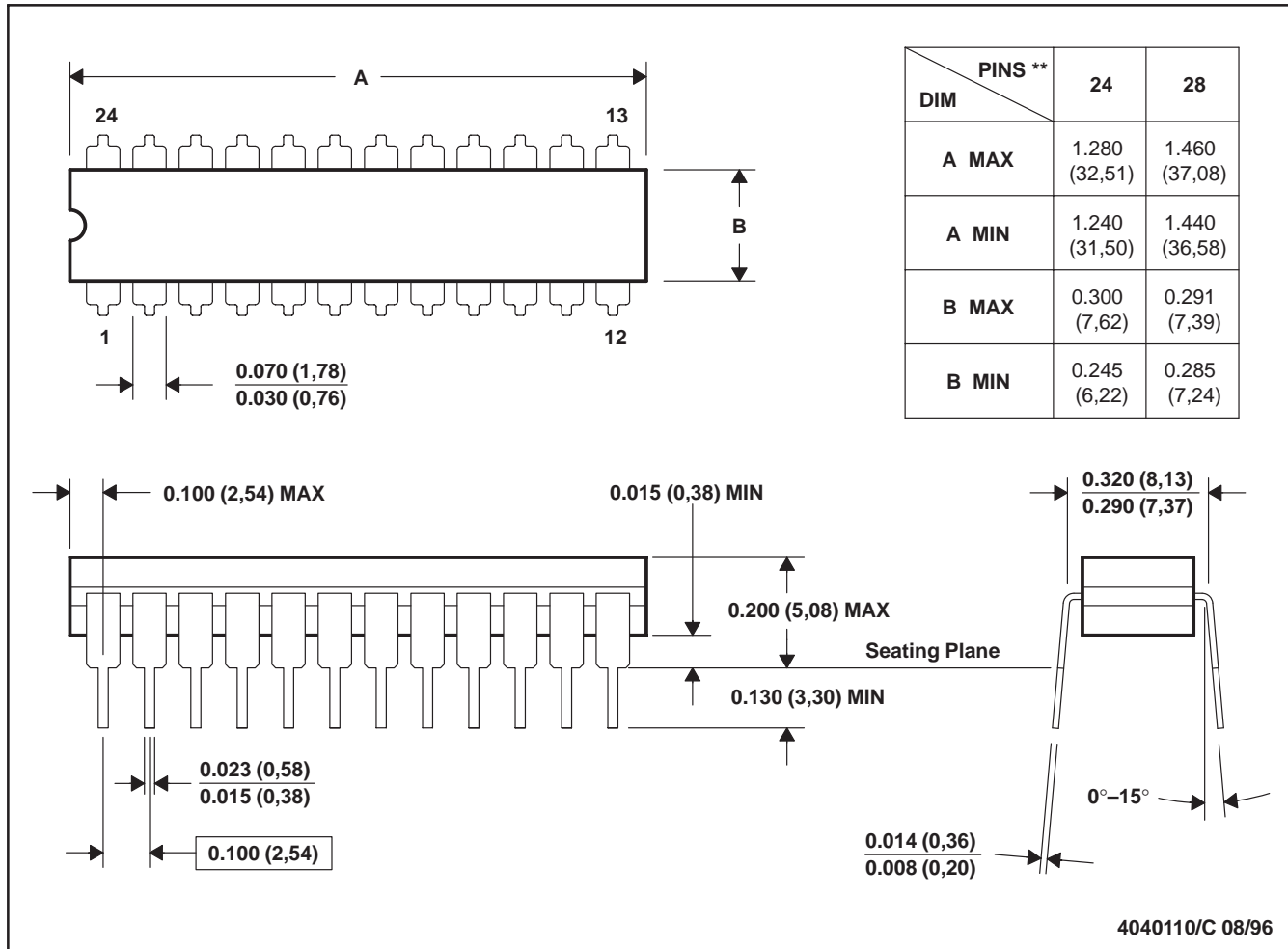
# MECHANICAL DATA

MCER004A – JANUARY 1995 – REVISED JANUARY 1997

JT (R-GDIP-T\*\*)

CERAMIC DUAL-IN-LINE

24 LEADS SHOWN



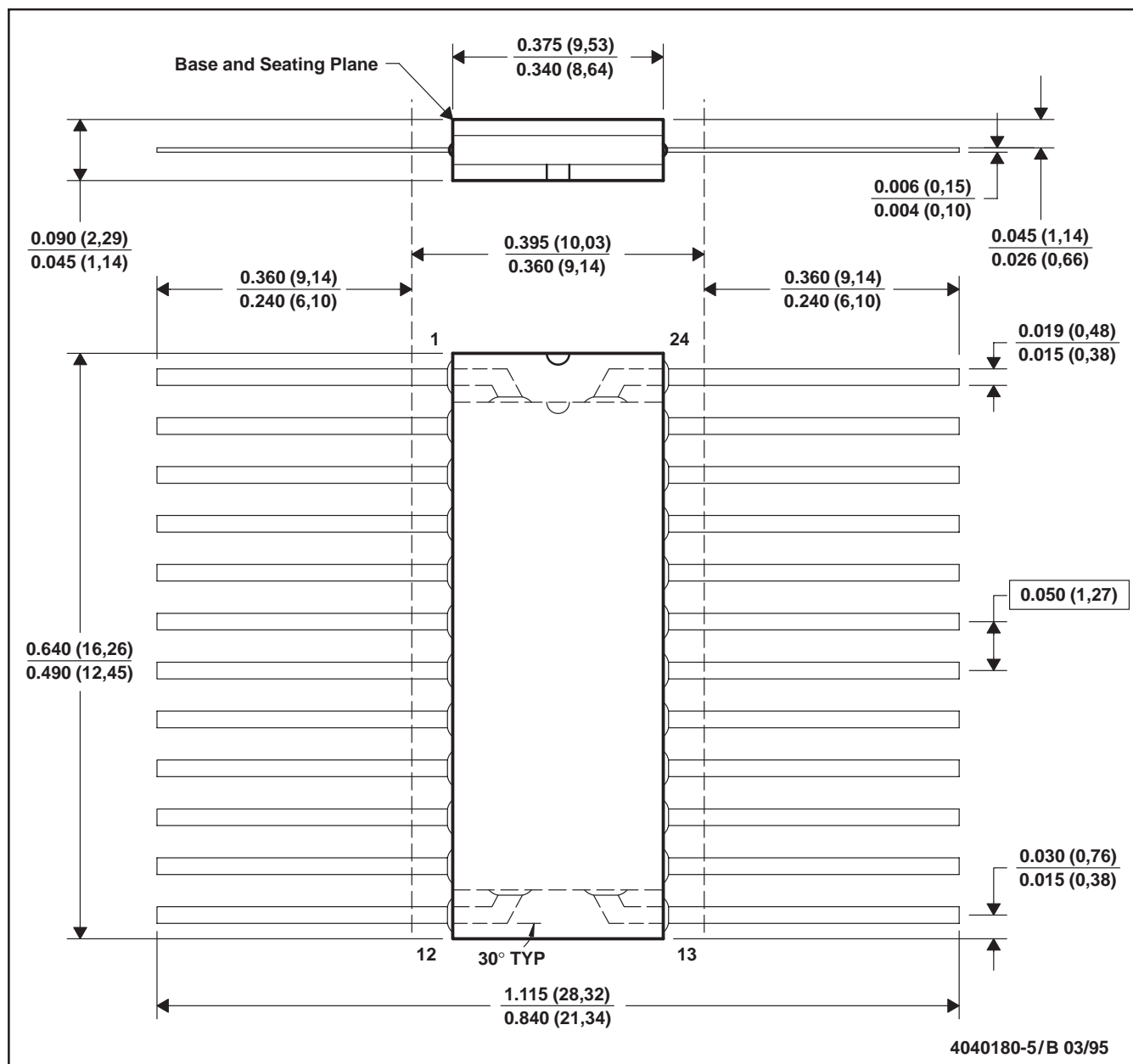
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification.
  - E. Falls within MIL STD 1835 GDIP3-T24, GDIP4-T28, and JEDEC MO-058 AA, MO-058 AB

# MECHANICAL DATA

MCFP007 – OCTOBER 1994

W (R-GDFP-F24)

CERAMIC DUAL FLATPACK



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a ceramic lid using glass frit.
  - Falls within MIL-STD-1835 GDFP2-F24 and JEDEC MO-070AD
  - Index point is provided on cap for terminal identification only.

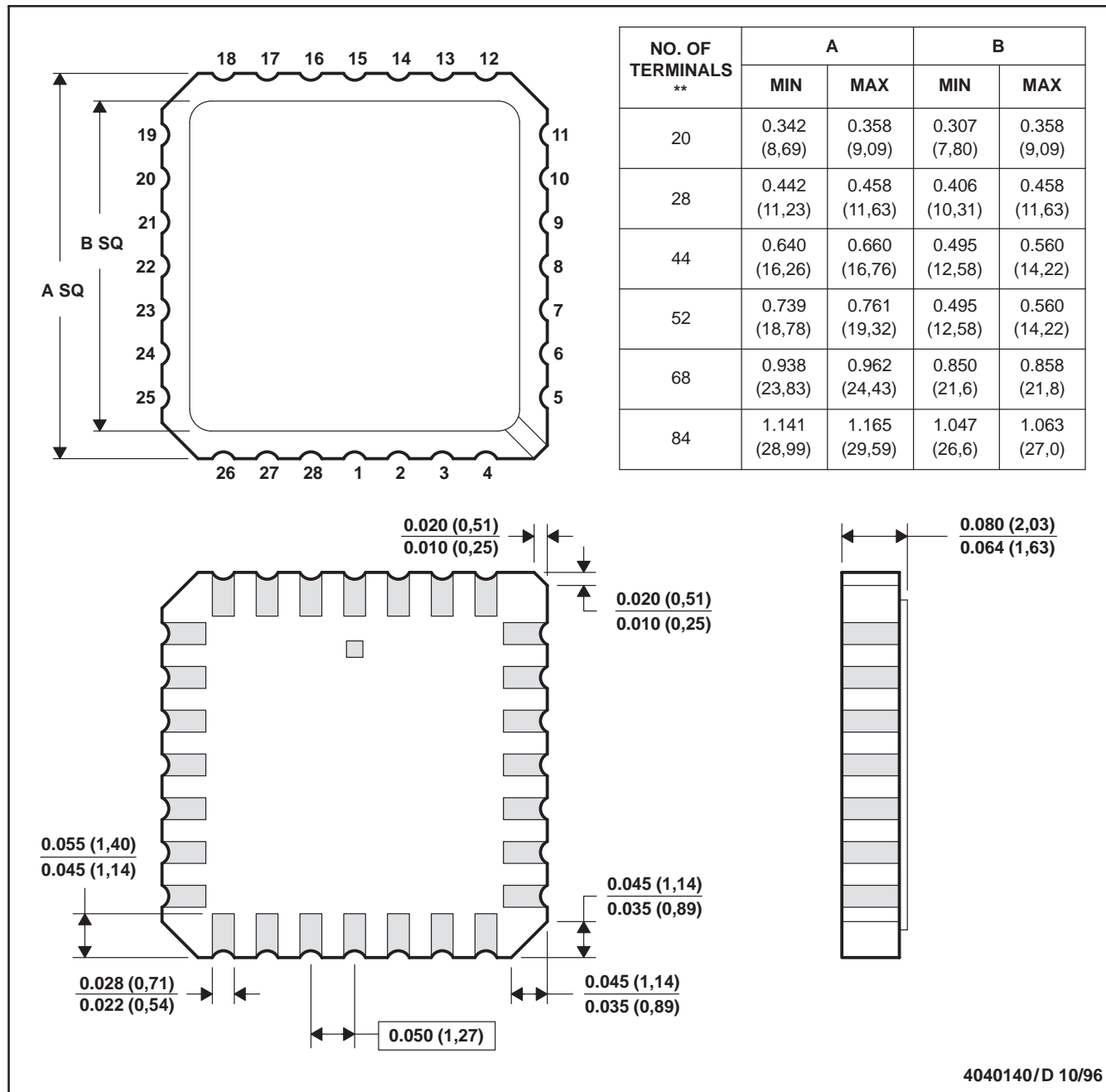
# MECHANICAL DATA

MLCC006B – OCTOBER 1996

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004



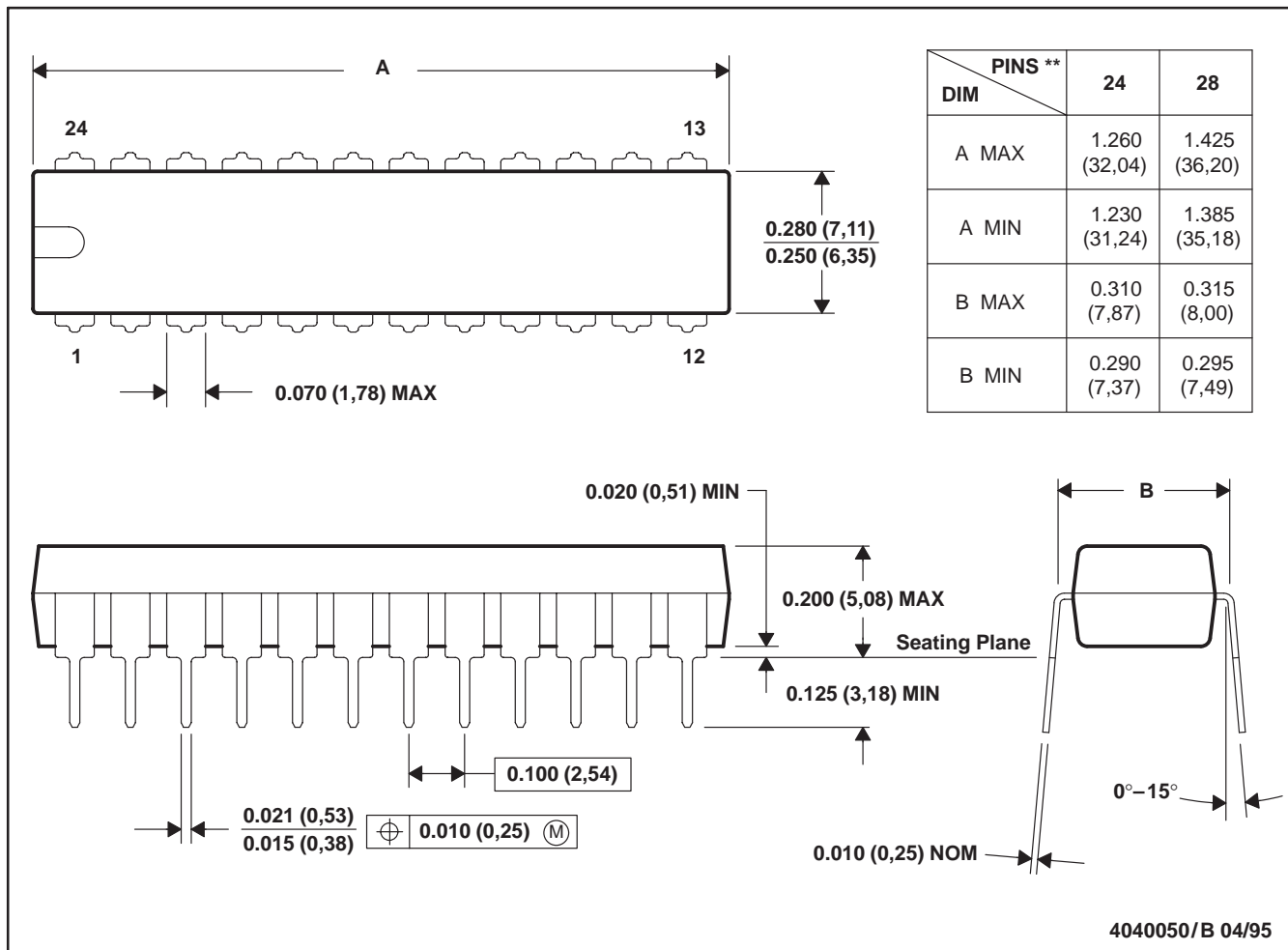
# MECHANICAL DATA

MPDI004 – OCTOBER 1994

NT (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

24 PINS SHOWN



NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

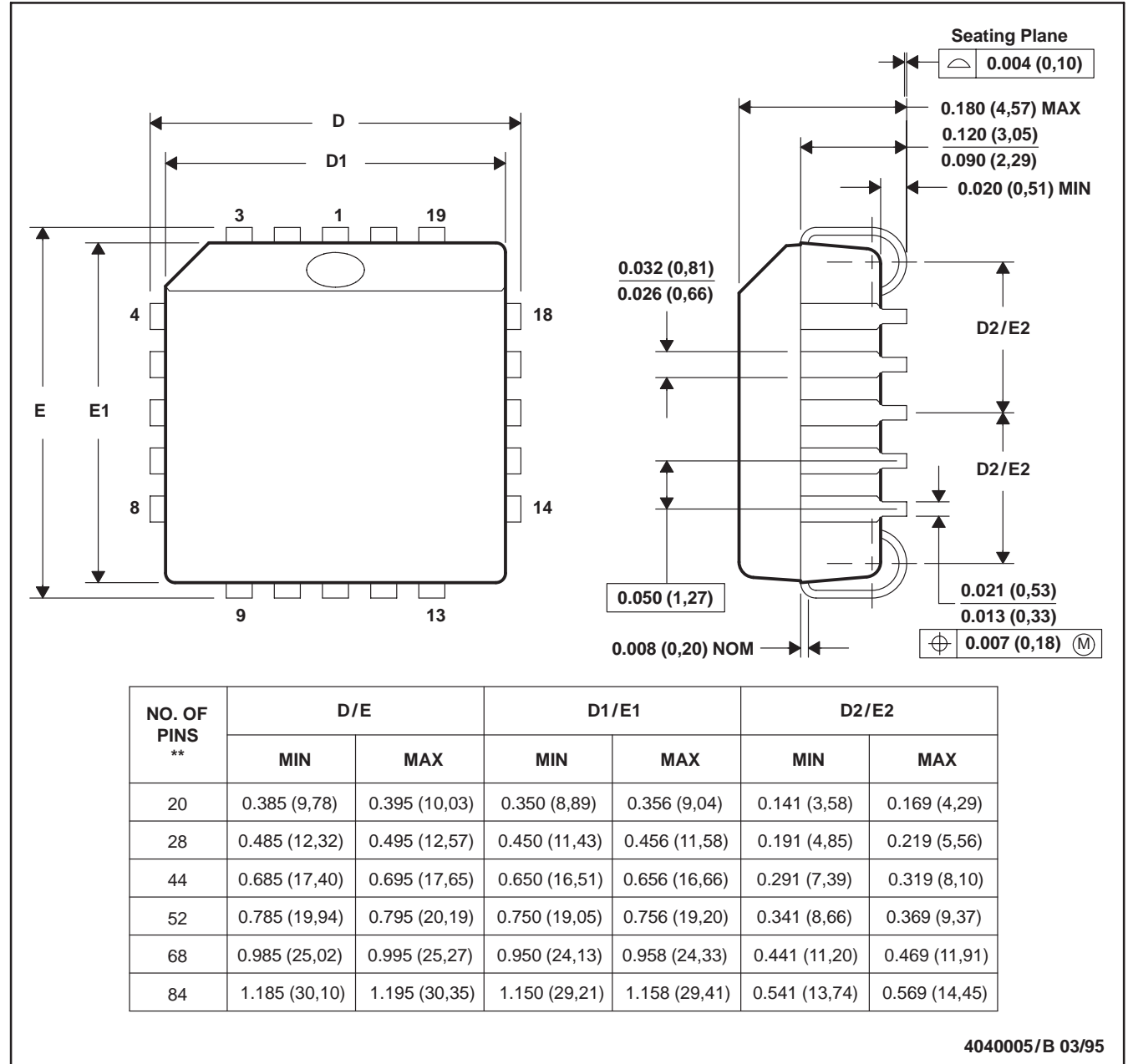
# MECHANICAL DATA

MPLC004A – OCTOBER 1994

FN (S-PQCC-J\*\*)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-018

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

### Products

Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>

### Applications

Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265