BS817

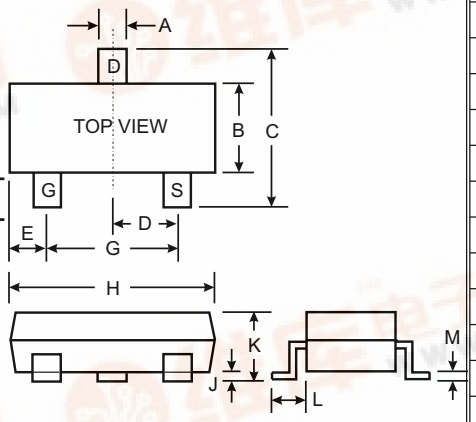
P-CHANNEL ENHANCEMENT MODE DMOS TRANSISTOR

Features

- High Breakdown Voltage
- High Input Impedance
- Fast Switching Speed
- Specially Suited for Telephone Subsets
- Ideal for Automated Surface Mount Assembly

Mechanical Data

- Case: SOT-23, Plastic
- Terminals: Solderable per MIL-STD-202, Method 208
- Terminal Connections (see Diagram)
- Marking: S17
- Weight: 0.008 grams (approx.)



SOT-23		
Dim	**Min**	**Max**
A	0.37	0.51
B	1.19	1.40
C	2.10	2.50
D	0.89	1.05
E	0.45	0.61
G	1.78	2.05
H	2.65	3.05
J	0.013	0.15
K	0.89	1.10
L	0.45	0.61
M	0.076	0.178
All Dimensions in mm		

Maximum Ratings @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	$-V_{DSS}$	200	V
Drain-Gate Voltage	$-V_{DGS}$	200	V
Gate-Source Voltage (pulsed) (Note 2)	V_{GS}	±20	V
Drain Current (continuous)	$-I_D$	100	mA
Power Dissipation @ $T_{C = 50°C}$ (Note 1)	Pd	310	mW
Operating and Storage Temperature Range	T_j, T_{STG}	-55 to +150	°C

Inverse Diode @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Max Forward Current (continuous)	I_F	0.3	A
Forward Voltage Drop (typical) @ V_{GS} = 0, I_F = 0.3A, T_j = 25°C	V_F	0.85	V

Notes: 1. Device mounted on Ceramic Substrate 0.7mm x 2.5cm² area.
2. Pulse Test: Pulse width = 80µs, duty cycle = 1%.

Electrical Characteristics @ T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Drain-Source Breakdown Voltage	$-V_{(BR)DSS}$	200	230	—	V	$-I_D$ = 100μA, V_{GS} = 0
Gate-Body Leakage Current	$-I_{GSS}$	—	—	10	nA	$-V_{GS}$ = 15V, V_{DS} = 0
Drain-Source Cutoff Current	$-I_{DSS}$ $-I_{DSX}$	—	—	30 1.0	nA μA	$-V_{DS}$ = 130V, V_{GS} = 0 $-V_{DS}$ = 70V, $-V_{GS}$ = 0.2V
Gate-Source Threshold Voltage	$-V_{GS(th)}$	—	2.8	3.5	V	$-V_{GS}$ = V_{DS}, $-I_D$ = 1.0mA
Drain-Source ON Resistance	$r_{DS(ON)}$	—	30	50	Ω	$-V_{GS}$ = 2.8V, $-I_D$ = 20mA
Thermal Resistance, Junction to Substrate Backside	$R_{\theta JSB}$	—	—	320	K/W	Note 1
Thermal Resistance, Junction to Ambient Air	$R_{\theta JA}$	—	—	400	K/W	Note 1
Input Capacitance Output Capacitance Feedback Capacitance	C_{iss} C_{oss} C_{rss}	—	58 8.0 1.5	—	pF	$-V_{DS}$ = 20V, V_{GS} = 0, f = 1.0MHz
Switching Times Turn-On Time Turn-Off Time	 t_{ON} t_{OFF}	—	 5.0 15	—	ns	$-V_{GS}$ = 10V, $-V_{DS}$ = 10V, R_D = 100Ω

Notes: 1. Device mounted on ceramic substrate 0.7mm x 2.5 cm² area.
2. Pulse test: Pulse width = 80μs, duty cycle = 1%.

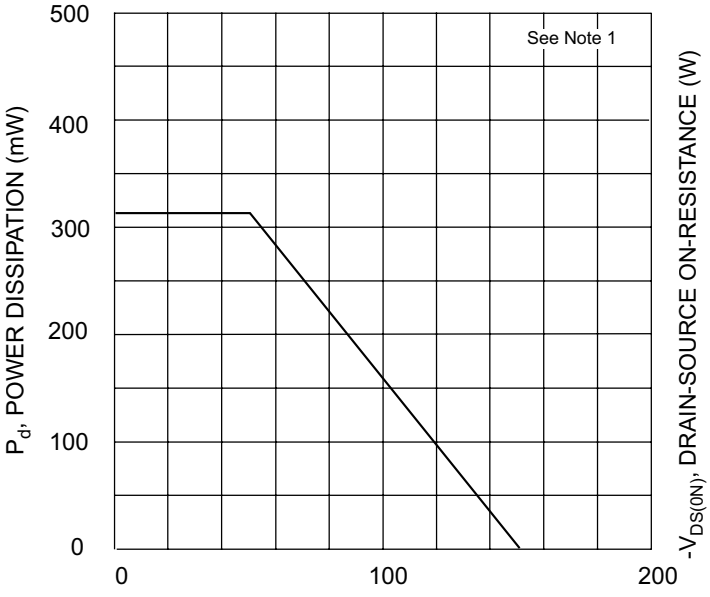


Fig. 1, Power Derating Curve

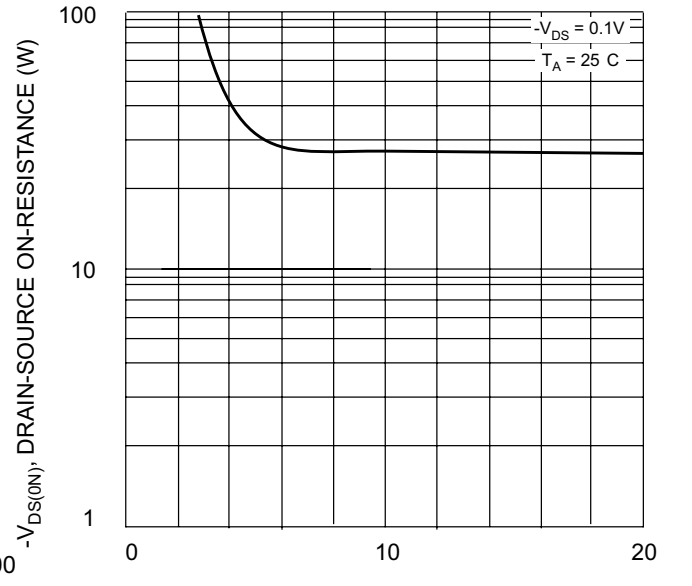


Fig. 2, Drain-Source Resistance vs Gate-Source Voltage