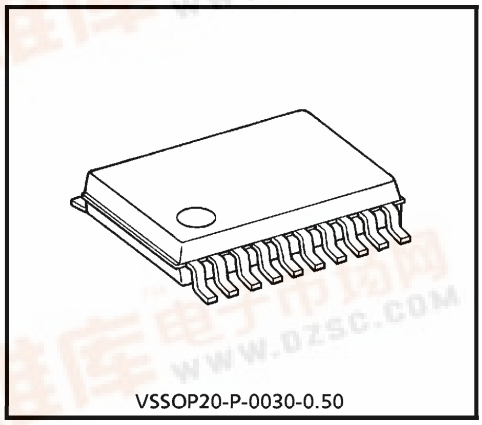
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC7MB3245FK

OCTAL BUS SWITCH

The TC7MB3245FK provides eight bits of high-speed TTL-compatible bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device is organized as one 8-bit switch. When output enable ($\overline{OE}$) is low, the switch is on and port A is connected to port B. When $\overline{OE}$ is high, the switch is open and a high-impedance state exists between the two ports. All inputs are equipped with protection circuits against static discharge.



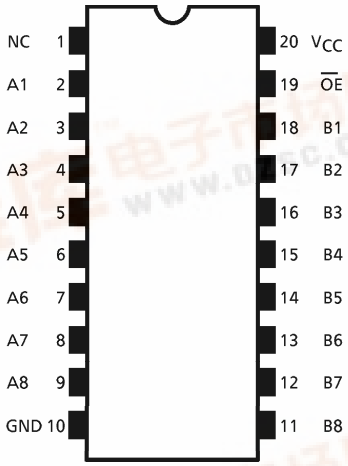
VSSOP20-P-0030-0.50

Weight : 0.03 g (typ.)

FEATURES

- Operating Voltage : V_{CC} = 4.5~5.5 V
- High Speed : t_{pd} = 0.25 ns (max)
- Low On Resistance : R_{ON} = 5 Ω (typ.)
- ESD Performance : Human Body Model > ± 2000 V
  Machine Model > ± 200 V
- Compatible With TTL Outputs (Control Inputs)
- Package : VSSOP (US20)
- Pin Compatible with the 74xx245 type.
  Functionally Equivalent to (FST / CBT) 3245.

PIN ASSIGNMENT

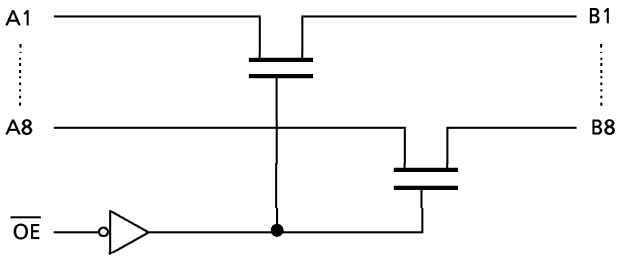


(TOP VIEW)

TRUTH TABLE

INPUTS $\overline{OE}$	FUNCTION
L	Aport = Bport
H	Disconnect

SYSTEM DIAGRAM



MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Power Supply Range	V_{CC}	−0.5~7.0	V
DC Input Voltage	V_{IN}	−0.5~7.0	V
DC Switch Voltage	V_S	−0.5~7.0	V
Input Diode Current	I_{IK}	−50	mA
Continuous Channel Current	I_S	128	mA
Power Dissipation	P_D	180	mW
DC V_{CC} / Ground Current	I_{CC} / I_{GND}	±100	mA
Storage Temperature	T_{stg}	−65~150	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~5.5	V
Switch Voltage	V_S	0~5.5	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	dt / dv	0~10	ns / V

ELECTRICAL CHARACTERISTICS

DC Characteristics (Ta = −40~85°C)

PARAMETER		SYMBOL	TEST CONDITION		V_{CC} (V)	Min	Typ. (Note 1)	Max	UNIT
Input Voltage	"H" Level	V_{IH}			4.5~5.5	2.0	—	—	V
	"L" Level	V_{IL}			4.5~5.5	—	—	0.8	
Input Leakage Current		I_{IN}	V_{IN} = 0~5.5 V		5.5	—	—	±1.0	μA
Off-STATE Leakage Current		I_{SZ}	A, B = 0~5.5 V, $\overline{OE}$ = V_{CC}		0~5.5	—	—	±1.0	μA
ON Resistance (Note 2)		R_{ON}	V_{IS} = 0 V	I_{IS} = 64 mA	4.5	—	5	7	Ω
				I_{IS} = 30 mA	4.5	—	5	7	
			V_{IS} = 2.4 V, I_{IS} = 15 mA		4.5	—	10	15	
Quiescent Supply Current		I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0		5.5	—	—	10	μA
Increase In I_{CC} Per Input		ΔI_{CC}	V_{IN} = 3.4 V (One Input)		5.5	—	—	2.5	mA

(Note 1) : Typical values are at V_{CC} = 5.0 V and Ta = +25°C.

(Note 2) : Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC Characteristics (Ta = −40~85°C)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Min	Max	UNIT
Propagation Delay Time (Bus to Bus)	t_{pLH} t_{pHL}	(Fig.1, 2)	(Note 3)	4.5	—	0.25	ns
Output Enable Time	t_{pZL} t_{pZH}	(Fig1, 3)		4.5	—	5.9	ns
Output Disable Time	t_{pLZ} t_{pHZ}	(Fig1, 3)		4.5	—	5.9	ns

(Note 3) : This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage the source (zero output impedance).

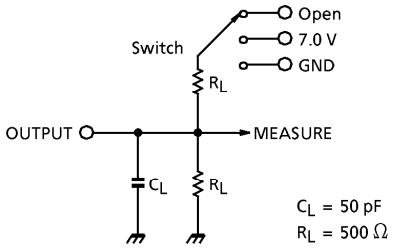
Capacitive Characteristics (Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Typ.	UNIT
Control Pin Input Capacitance	C_{IN}		(Note 4)	5.0	3	pF
Switch Terminal Capacitance	$C_{I/O}$	$\overline{OE}$ = V_{CC}	(Note 4)	5.0	10	pF

(Note 4) : Parameter guaranteed by design

TEST CIRCUIT

Fig.1



PARAMETER	SWITCH
t_{pLH}, t_{pHL}	Open
t_{pLZ}, t_{pZL}	7.0 V
t_{pHZ}, t_{pZH}	Open

AC WAVEFORM

Fig.2 t_{pLH}, t_{pHL}

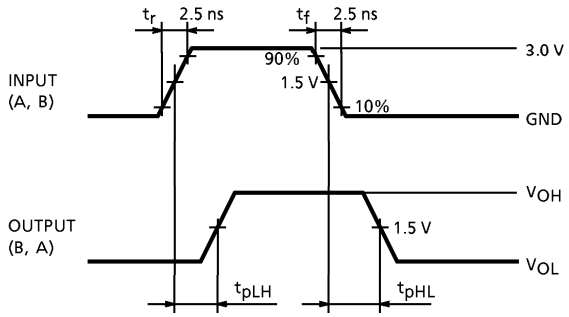
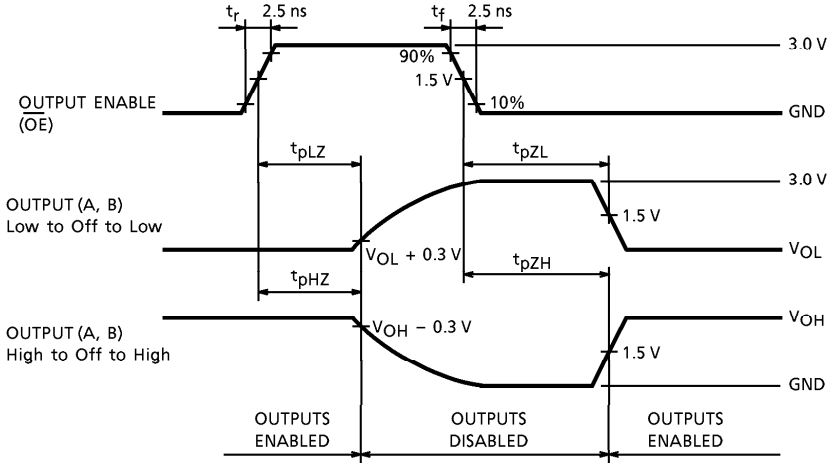
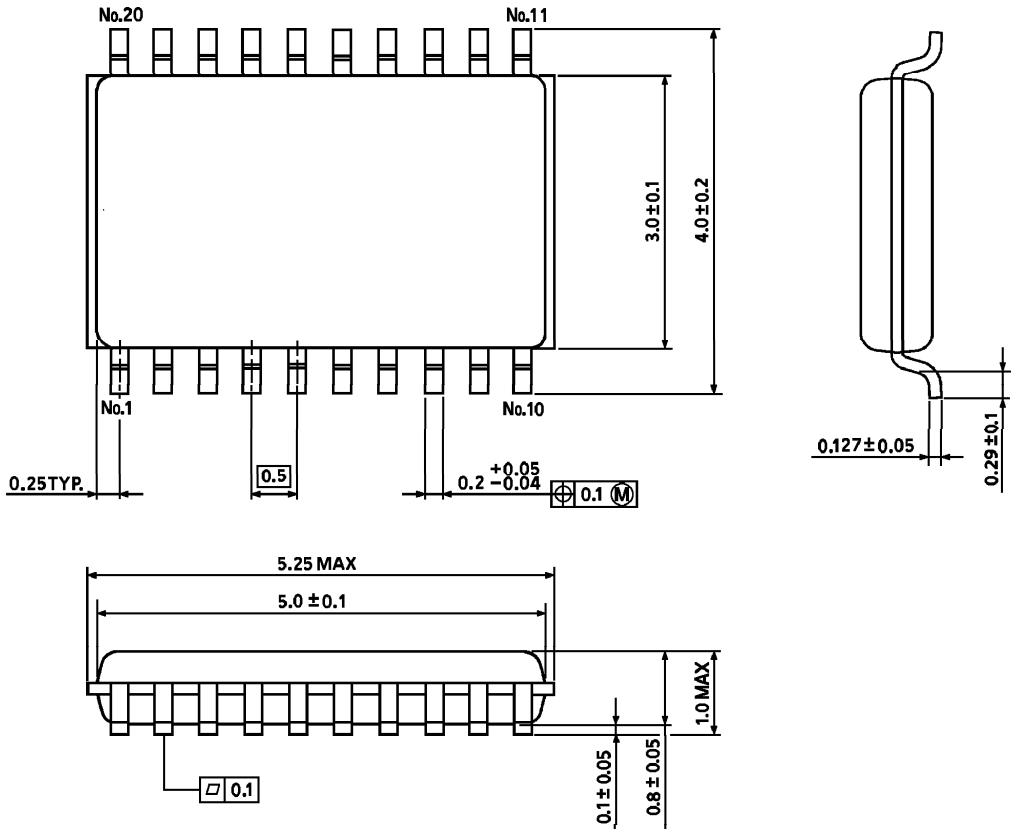


Fig.3 t_{pLZ}, t_{pHZ}, t_{pZL}, t_{pZH}



PACKAGE DIMENSIONS

VSSOP20-P-0030-0.50 Unit : mm



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