



Data sheet acquired from Harris Semiconductor  
SCHS098D – Revised October 2003

# CD40107B Types

## CMOS Dual 2-Input NAND Buffer/Driver

### High-Voltage Type (20-Volt Rating)

The CD40107B is a dual 2-input NAND buffer/driver containing two independent 2-input NAND buffers with open-drain single n-channel transistor outputs. This device features a wired-OR capability and high output sink current capability (136 mA typ. at  $V_{DD} = 10\text{ V}$ ,  $V_{DS} = 1\text{ V}$ ). The CD40107B is supplied in 8-lead hermetic dual-in-line ceramic packages (F3A suffix), 8-lead dual-in-line plastic packages (E suffix), 8-lead small-outline packages (M, M96, MT, and PSR suffixes), and 8-lead thin shrink small-outline packages (PW and PWR suffixes).

### Features:

- 32 times standard B-Series output current drive sinking capability – 136 mA typ. @  $V_{DD} = 10\text{ V}$ ,  $V_{DS} = 1\text{ V}$
- 100% tested for quiescent current at 20 V
- Maximum input current of  $1\text{ }\mu\text{A}$  at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin, full package temperature range,  $R_L$  to  $V_{DD} = 10\text{ k}\Omega$ :  
1 V at  $V_{DD} = 5\text{ V}$   
2 V at  $V_{DD} = 10\text{ V}$   
2.5 V at  $V_{DD} = 15\text{ V}$
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

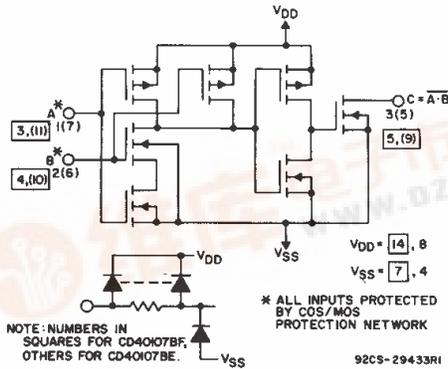
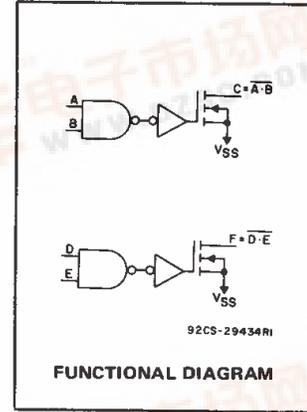


Fig.1 – Schematic diagram of CD40107B (one of 2 gates)

### TRUTH TABLE

A	B	C
0	0	1*
1	0	1*
0	1	1*
1	1	0

\*Requires external pull-up resistor ( $R_L$ ) to  $V_{DD}$ .  
#Without pull-up resistor. (3-state).

### Applications

- Driving relays, lamps, LEDs
- Line driver
- Level shifter (up or down)

### MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, ( $V_{DD}$ )	-0.5V to +20V
Voltages referenced to $V_{SS}$ Terminal)	
INPUT VOLTAGE RANGE, ALL INPUTS	-0.5V to $V_{DD} + 0.5\text{ V}$
DC INPUT CURRENT, ANY ONE INPUT	$\pm 10\text{ }\mu\text{A}$
POWER DISSIPATION PER PACKAGE ( $P_D$ ):	
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$	500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$	Derate Linearity at $12\text{ mW}/^\circ\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR	
FOR $T_A =$ FULL PACKAGE-TEMPERATURE RANGE (All Package Types)	100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):	
At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79\text{ mm}$ ) from case for 10s max	$+265^\circ\text{C}$

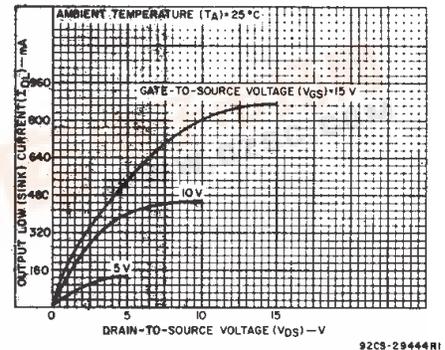


Fig.2 – Typical output low (sink) current characteristics.

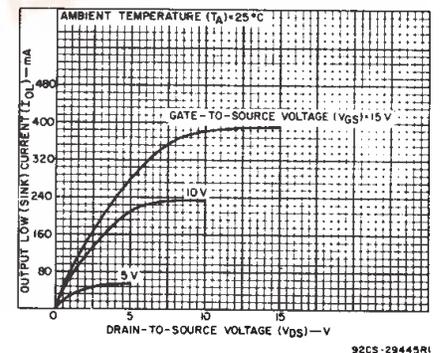


Fig.3 – Minimum output low (sink) current characteristics.

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For $T_A =$ Full Package-Temperature Range)	3	18	V

## CD40107B Types

**DYNAMIC ELECTRICAL CHARACTERISTICS** at  $T_A = 25^\circ\text{C}$ ,  $C_L = 50\text{ pF}$ , Input  $t_r, t_f = 20\text{ ns}$

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS
		VDD Volts	Typ.	Max.	
Propagation Delay: High-to-Low, $t_{PHL}$	$R_L^* = 120\ \Omega$	5	100	200	ns
		10	45	90	
		15	30	60	
Low-to-High, $t_{PLH}$	$R_L^* = 120\ \Omega$	5	100	200	ns
		10	60	120	
		15	50	100	
Transition Time: High-to-Low, $t_{THL}$	$R_L^* = 120\ \Omega$	5	50	100	ns
		10	20	40	
		15	10	20	
Low-to-High, $t_{TLH}$	$R_L^* = 120\ \Omega$	5	50	100	ns
		10	35	70	
		15	25	50	
Average Input Capacitance, $C_{IN}$	Any Input		5	7.5	pF
Average Output Capacitance, $C_{OUT}$	Any Output		30	—	pF

\*  $R_L$  is external pull-up resistor to  $V_{DD}$ .

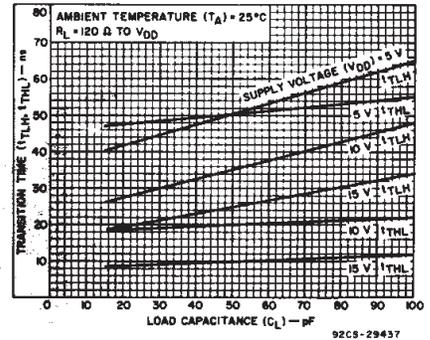


Fig. 4 — Typical transition time as a function of load capacitance.

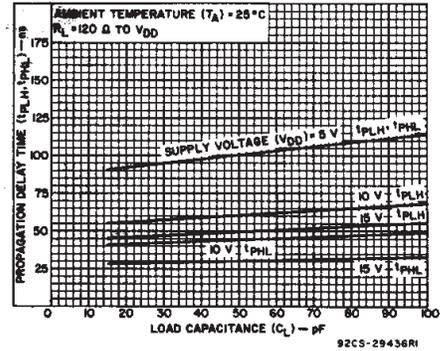


Fig. 5 — Typical propagation delay time as a function of load capacitance.

### STATIC ELECTRICAL CHARACTERISTICS

CHARACTER- ISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES ( $^\circ\text{C}$ )							UNITS
	$V_O$ (V)	$V_{IN}$ (V)	$V_{DD}$ (V)	-55			+25			Max.	
				Min.	Typ.	Max.	Min.	Typ.	Max.		
Quiescent Device Current $I_{DD}$ Max.	—	0.5	5	1	1	30	30	—	0.02	1	$\mu\text{A}$
	—	0.10	10	2	2	60	60	—	0.02	2	
	—	0.15	15	4	4	120	120	—	0.02	4	
	—	0.20	20	20	20	600	600	—	0.04	20	
Output Low (Sink) Current $I_{OL}$ Min.	0.4	0.5	5	21	20	14	12	16	32	—	$\text{mA}$
	1	0.5	5	44	42	30	25	34	68	—	
	0.5	0.10	10	49	46	32	28	37	74	—	
	1	0.10	10	89	85	60	51	68	136	—	
	0.5	0.15	15	66	63	44	38	50	100	—	
Output High (Source) Current $I_{OH}$ Min.	No Internal Pull-Up Device										
Input Low Voltage $V_{IL}$ Max.*	4.5	—	5	1.5			—	—	1.5	$\text{V}$	
	9	—	10	3			—	—	3		
	13.5	—	15	4			—	—	4		
Input High Voltage $V_{IH}$ Min.*	0.5, 4.5	—	5	3.5			3.5	—	—	$\text{V}$	
	1.9	—	10	7			7	—	—		
	1.5, 13.5	—	15	11			11	—	—		
Input Current $I_{IN}$ Max.	—	0.18	18	$\pm 0.1$	$\pm 0.1$	$\pm 1$	$\pm 1$	—	$\pm 10^{-5}$	$\pm 0.1$	$\mu\text{A}$
Output Leakage Current $I_{OZ}$ Max.	18	0.18	18	2	2	20	20	—	$10^{-4}$	2	$\mu\text{A}$

\* Measured with external pull-up resistor,  $R_L = 10\text{ k}\Omega$  to  $V_{DD}$ .

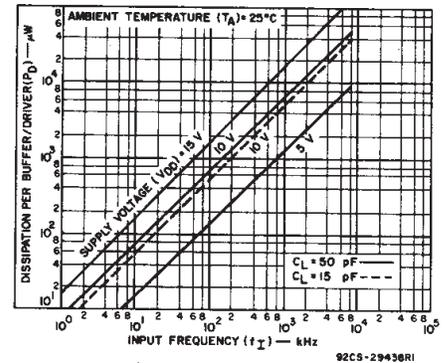


Fig. 6 — Typical power dissipation as a function of input frequency.

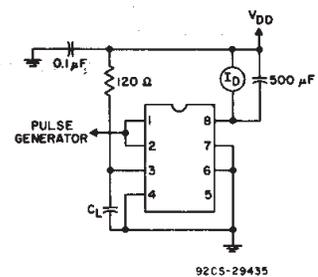
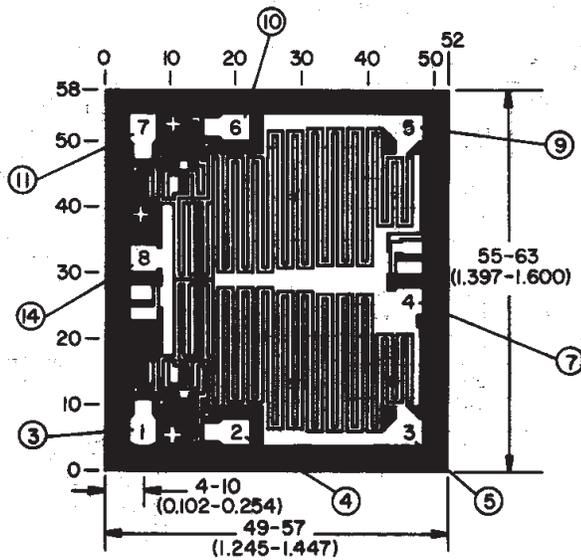


Fig. 7 — Power-dissipation test circuit for CD40107BE.

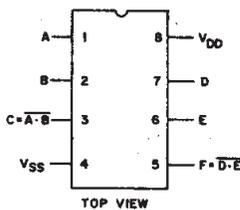
## CD40107B Types



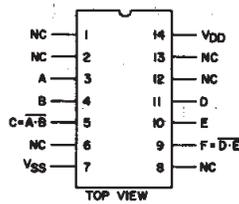
NOTE: NOS. IN PADS FOR CD40107BE  
NOS. OUTSIDE CHIP FOR CD40107BF

*Dimensions and Pad Layout for CD40107BH.*

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).



CD40107BE



CD40107BF

### TERMINAL ASSIGNMENTS

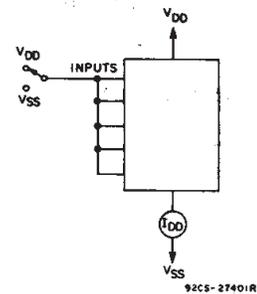


Fig. 8 - Quiescent-device current test circuit.

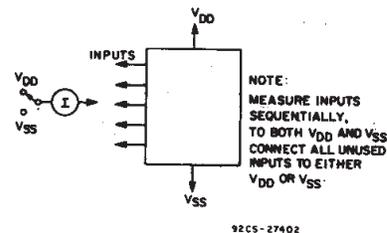


Fig. 9 - Input-current test circuit.

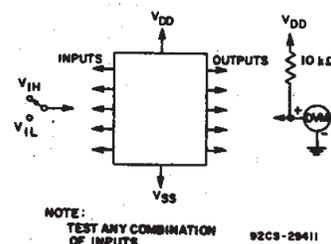


Fig. 10 - Input-voltage test circuit.

### Special Considerations for CD40107B

1. **Limiting Capacitive Currents for  $C_L > 500$  pF,  $V_{DD} > 15$  V.**  
For  $V_{DD} > 15$  V, and load capacitance ( $C_L$ ) from output to ground  $> 500$  pF, an external  $25 \Omega$  series limiting resistor should be inserted between the output terminal and  $C_L$ . No external resistor is necessary if  $C_L < 500$  pF or  $V_{DD} < 15$  V.
2. **Driving Inductive Loads**  
When using the CD40107B to drive inductive loads, the load should be shunted with a diode to prevent high voltages from developing across the CD40107B output.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD40107BE	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CD40107BF	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD40107BF3A	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
CD40107BM	ACTIVE	SOIC	D	8	75	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD40107BM96	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD40107BMT	ACTIVE	SOIC	D	8	250	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD40107BPSR	ACTIVE	SO	PS	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CD40107BPW	ACTIVE	TSSOP	PW	8	150	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CD40107BPWR	ACTIVE	TSSOP	PW	8	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**None:** Not yet available Lead (Pb-Free).

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

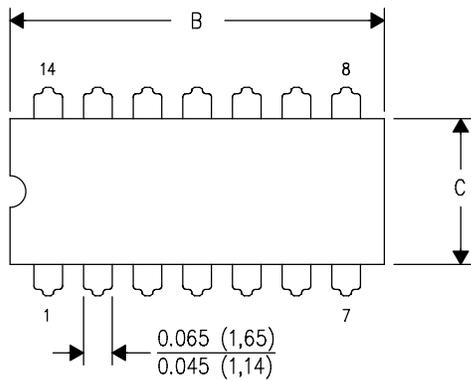
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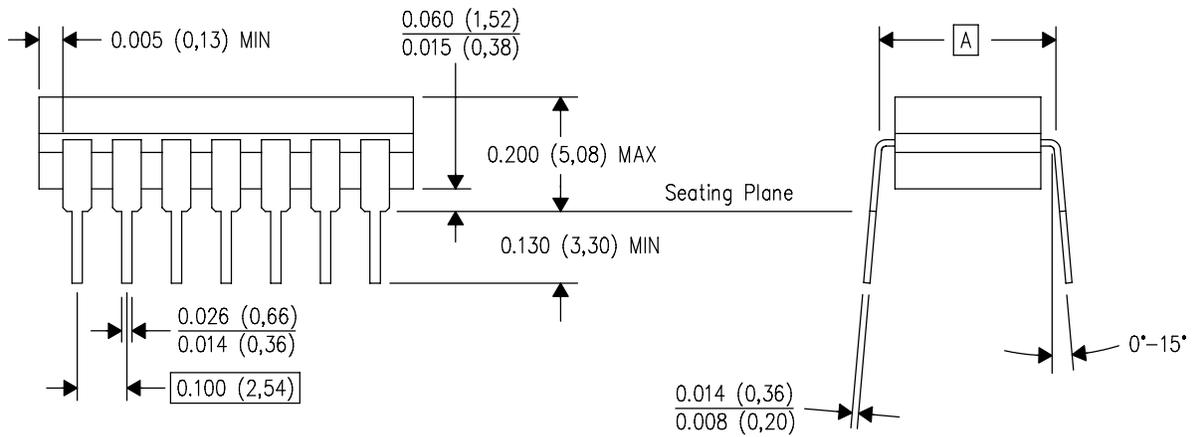
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

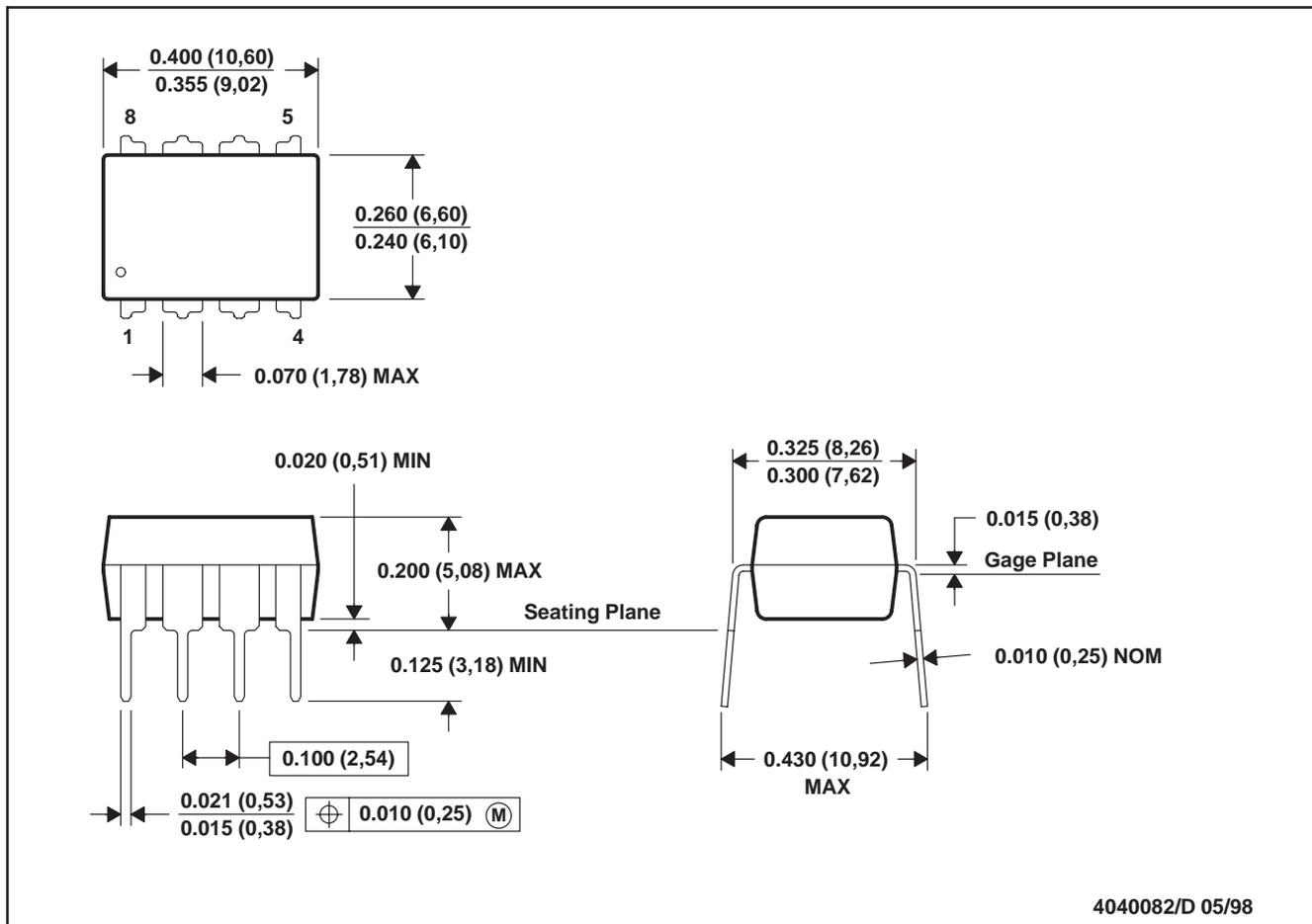
- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

# MECHANICAL DATA

MPDI001A – JANUARY 1995 – REVISED JUNE 1999

## P (R-PDIP-T8)

## PLASTIC DUAL-IN-LINE

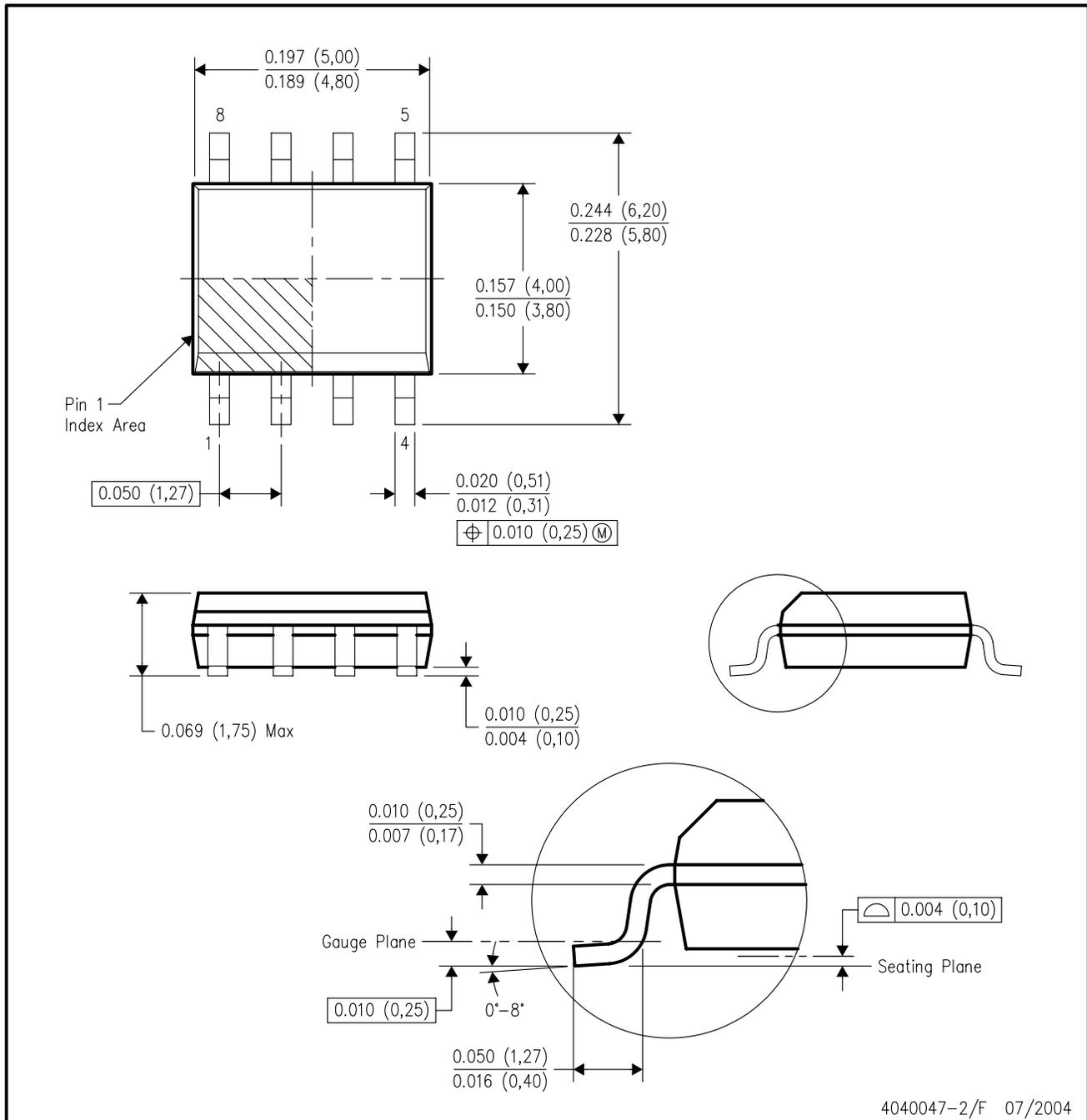


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

# MECHANICAL DATA

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE

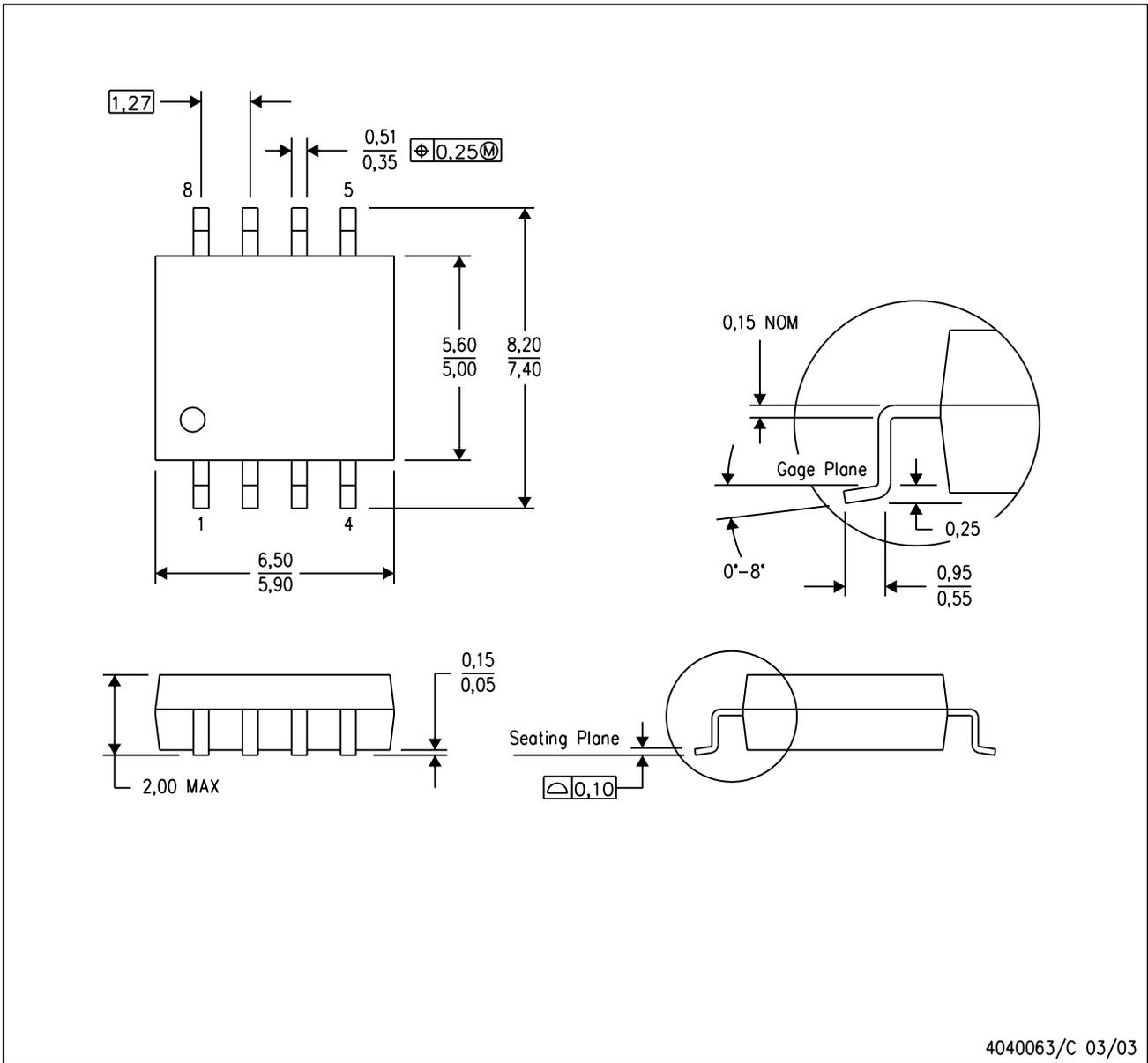


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-012 variation AA.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

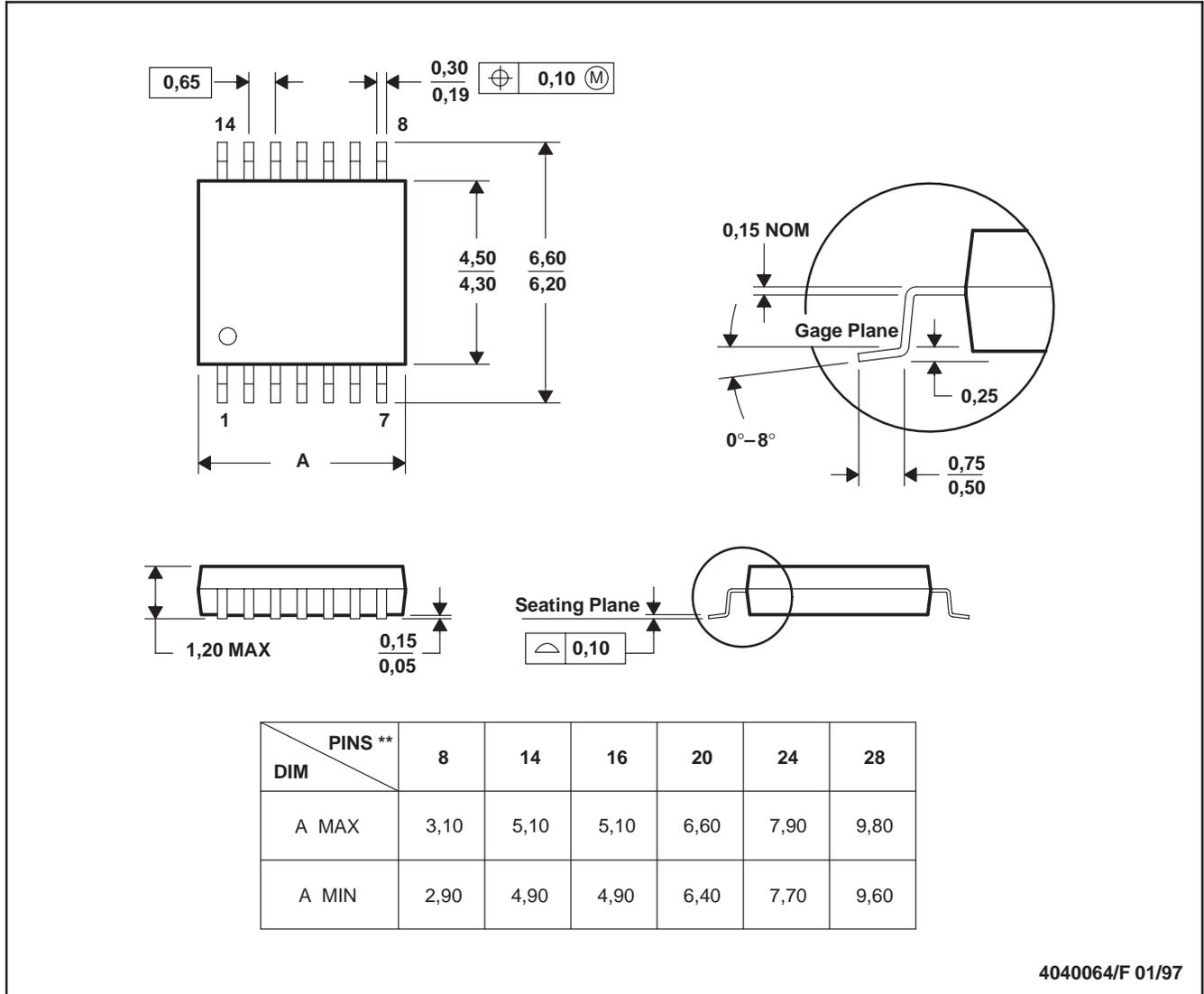
# MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

**PW (R-PDSO-G\*\*)**

**PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - Falls within JEDEC MO-153

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