



CD54AC541F3A, CD54ACT541F3A

Octal Buffer/Line Driver
Three-State, Non-Inverting

July 1998

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Exceeds 2kV ESD Protection MIL-STD-883, Method 3015
- Meets JEDEC Standard No. 20
- SCR - Latch-Up-Resistant CMOS Process and Circuit Design
- Speed of Bipolar FAST/AS with Significantly Reduced Power Consumption
- Functionally and Pin-Compatible with Industry 54 Bipolar Types in the FAST, AS and S Series
- Balanced Propagation Delays
- Military Operating Temperature Range
 - Ceramic (CERDIP) 54 Series: -55 to 125°C
- $\pm 24\text{mA}$ Output Drive Current, Drives 75 Ω Lines without Need for Terminations
- Fan Out (Over Temperature)
 - ACL Loads 2400
 - FAST Loads..... 15
 - AS Loads..... 48
- Operating Voltage
 - AC Types 1.5V to 5.5V
 - ACT Types..... 4.5V to 5.5V

Description

The CD54AC541F3A and CD54ACT541F3A are octal buffer/line drivers that utilize the Harris Advanced CMOS Logic technology. The CD54AC541F3A and CD54ACT541F3A are non-inverting three-state buffers having two active-LOW output enables.

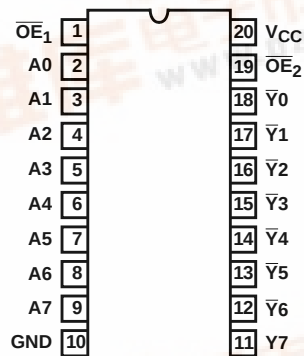
Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD54AC541F3A	-55 to 125	20 Ld CERDIP	F20.3
CD54ACT541F3A	-55 to 125	20 Ld CERDIP	F20.3

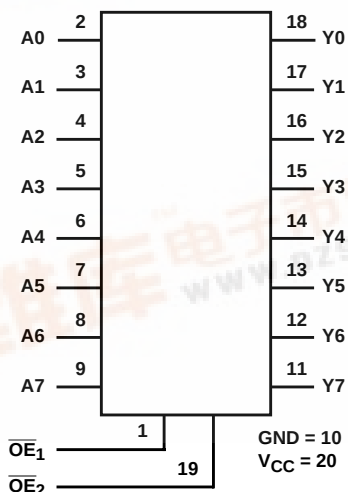
NOTE:

1. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Pinout



Functional Diagram



CD54AC541F3A, CD54ACT541F3A

Absolute Maximum Ratings

DC Supply Voltage, V_{CC} -0.5V to 6V
 DC Input Diode Current, I_{IK}
 For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ $\pm 20mA$
 DC Output Diode Current, I_{OK}
 For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ $\pm 50mA$
 DC Output Source or Sink Current per Output Pin, I_O
 For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ $\pm 50mA$
 DC V_{CC} or Ground Current, I_{CC} or I_{GND} (Note 2) $\pm 100mA$

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} ($^{\circ}C/W$) θ_{JC} ($^{\circ}C/W$)
 CERDIP Package 85 24
 Maximum Junction Temperature (Hermetic Package or Die) . . . $175^{\circ}C$
 Maximum Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
 Maximum Lead Temperature (Soldering 10s) $300^{\circ}C$

Operating Conditions

Temperature Range, T_A $-55^{\circ}C$ to $125^{\circ}C$
 Supply Voltage Range, V_{CC} (Note 3)
 AC Types 1.5V to 5.5V
 ACT Types 4.5V to 5.5V
 DC Input or Output Voltage, V_I , V_O 0V to V_{CC}
 Input Rise and Fall Slew Rate, dt/dv
 AC Types
 1.5V to 3V 50ns (Max)
 3.6V to 5.5V 20ns (Max)
 4.5V to 5.5V 10ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

2. For up to 4 outputs per device, add $\pm 25mA$ for each additional output.
3. Unless otherwise specified, all voltages are referenced to ground.
4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	MAX	MIN	MAX	
AC TYPES									
High Level Input Voltage	V _{IH}	-	-	1.5	1.2	-	1.2	-	V
				3	2.1	-	2.1	-	V
				4.5	3.15 (Note 5)	-	3.15 (Note 5)	-	V
				5.5	3.85	-	3.85	-	V
Low Level Input Voltage	V _{IL}	-	-	1.5	-	0.3	-	0.3	V
				3	-	0.9	-	0.9	V
				4.5	-	1.35 (Note 5)	-	1.35 (Note 5)	V
				5.5	-	1.65	-	1.65	V
High Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-0.05	1.5	1.4	-	1.4	-	V
			-0.05	3	2.9	-	2.9	-	V
			-0.05	4.5	4.4	-	4.4	-	V
			-4	3	2.58	-	2.4	-	V
			-24	4.5	3.94 (Note 5)	-	3.7 (Note 5)	-	V
			-50 (Note 6, 7)	5.5	-	-	3.85	-	V

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DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	MAX	MIN	MAX	
Low Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	0.05	1.5	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.5	V
			24	4.5	-	0.36 (Note 5)	-	0.5 (Note 5)	V
			50 (Note 6, 7)	5.5	-	-	-	1.65	V
Input Leakage Current	I _I	V _{CC} or GND	-	5.5	-	±0.1 (Note 5)	-	±1 (Note 5)	μA
Three-State Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND	-	5.5	-	±0.5 (Note 5)	-	±10 (Note 5)	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	8 (Note 5)	-	160 (Note 5)	μA
ACT TYPES									
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2 (Note 5)	-	2 (Note 5)	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	0.8 (Note 5)	-	0.8 (Note 5)	V
High Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-0.05	4.5	4.4	-	4.4	-	V
			-24	4.5	3.94 (Note 5)	-	3.7 (Note 5)	-	V
			-50 (Note 6, 7)	5.5	-	-	3.85	-	V
Low Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	0.05	4.5	-	0.1	-	0.1	V
			24	4.5	-	0.36 (Note 5)	-	0.5 (Note 5)	V
			50 (Note 6, 7)	5.5	-	-	-	1.65	V
Input Leakage Current	I _I	V _{CC} or GND	-	5.5	-	±0.1 (Note 5)	-	±1 (Note 5)	μA
Three-State or Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND	-	5.5	-	±0.5 (Note 5)	-	±10 (Note 5)	μA
Quiescent Device Current	I _{CC}	V _{CC} or GND	0	5.5	-	8 (Note 5)	-	160 (Note 5)	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI _{CC}	V _{CC} -2.1	-	4.5 to 5.5	-	2.4	-	3	mA

NOTES:

5. Tested 100%.
6. Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
7. Test verifies a minimum transmission-line-drive capability of 75Ω for 54AC/ACT Series.

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ACT Input Load Table

INPUT	UNIT LOAD
Data	0.5
$\overline{OE}1, \overline{OE}2$	1.3

NOTE: Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

Switching Specifications Input $t_r, t_f = 3\text{ns}$, $C_L = 50\text{pF}$ (Worst Case)

PARAMETER	SYMBOL	V _{CC} (V)	-55°C TO 125°C			UNITS
			MIN	TYP	MAX	
AC TYPES						
Propagation Delay, Data to Output	t _{PLH} , t _{PHL}	1.5	-	-	98	ns
		3.3 (Note 9)	3.3	-	10.9	ns
		5 (Note 10)	2.3	-	7.8 (Note 8)	ns
Propagation Delay, Enable, Disable to Output	t _{PZL} , t _{PZH}	1.5	-	-	150	
		3.3	5.4	-	18	
		5	3.6	-	12 (Note 8)	
	t _{PLZ} , t _{PHZ}	1.5	-	-	150	
		3.3	4.5	-	15	
		5	3.6	-	12 (Note 8)	
Minimum (Valley) V _{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OHV} See Figure 1	5	-	4 at 25°C	-	V
Maximum (Peak) V _{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OLP} See Figure 1	5	-	1 at 25°C	-	V
Three-State Output Capacitance	C _O	-	-	-	15	pF
Input Capacitance	C _I	-	-	-	10	pF
Power Dissipation Capacitance	C _{PD} (Note 11)	-	-	60	-	pF
ACT TYPES						
Propagation Delay, Data to Output	t _{PLH} , t _{PHL}	5 (Note 10)	2.5	-	8.3 (Note 8)	ns
Propagation Delay, Enable, Disable to Output	t _{PLZ} , t _{PZL} , t _{PZH} , t _{PHZ}	5	4	-	13.4 (Note 8)	ns
Minimum (Valley) V _{OH} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OHV} See Figure 1	5	-	4 at 25°C	-	V
Maximum (Peak) V _{OL} During Switching of Other Outputs (Output Under Test Not Switching)	V _{OLP} See Figure 1	5	-	1 at 25°C	-	V
Three-State Output Capacitance	C _O	-	-	-	15	pF
Input Capacitance	C _I	-	-	-	10	pF
Power Dissipation Capacitance	C _{PD} (Note 11)	-	-	60	-	pF

NOTES:

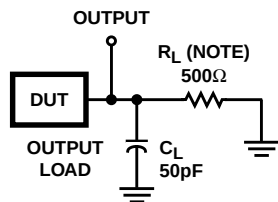
8. Limits tested 100%.
9. 3.3V Min is at 3.6V, Max is at 3V.
10. 5V Min is at 5.5V, Max is at 4.5V
11. C_{PD} is used to determine the dynamic power consumption per gate.
 AC: $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$
 ACT: $P_D = V_{CC}^2 f_i (C_{PD} + C_L) + V_{CC} \Delta I_{CC}$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

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Burn-In Test Circuit Connections (Use DC II for F3A Burn-In and AC for Life Test)

DC	DC BURN-IN I			DC BURN-IN II		
	OPEN	GROUND	V _{CC} (6V)	OPEN	GROUND	V _{CC} (6V)
CD54AC/ACT541	11-18	1-10, 19	20	11-18	10	1-9, 19, 20
AC	OPEN	GROUND	1/2 V _{CC} (3V)	V _{CC} (6V)	OSCILLATOR	
					50kHz	25kHz
CD54AC/ACT541	-	10	11-18	20	1, 19	2-9

NOTE: Each pin except V_{CC} and Gnd will have a resistor of 2k Ω -47k Ω .



NOTE: For AC Series Only: When V_{CC} = 1.5V, R_L = 1k Ω .

	CD54AC	CD54ACT
Input Level	V _{CC}	3V
Input Switching Voltage, V _S	0.5 V _{CC}	1.5V
Output Switching Voltage, V _S	0.5 V _{CC}	0.5 V _{CC}

FIGURE 1. PROPAGATION DELAY TIMES

All Harris Semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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