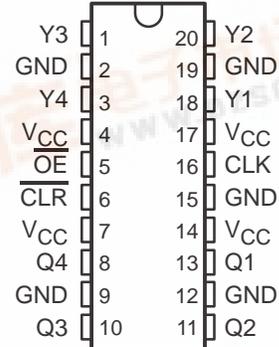


**CLOCK DRIVER
WITH 3-STATE OUTPUTS**

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- **Low Output Skew, Low Pulse Skew for Clock-Distribution and Clock-Generation Applications**
- **TTL-Compatible Inputs and Outputs**
- **Distributes One Clock Input to Eight Outputs**
 - Four Same-Frequency Outputs
 - Four Half-Frequency Outputs
- **Distributed V_{CC} and Ground Pins Reduce Switching Noise**
- **High-Drive Outputs (–48-mA I_{OH}, 48-mA I_{OL})**
- **State-of-the-Art EPIC-II B™ BiCMOS Design Significantly Reduces Power Dissipation**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages**

DB OR DW PACKAGE
(TOP VIEW)



description

The CDC339 is a high-performance, low-skew clock driver. It is specifically designed for applications requiring synchronized output signals at both the primary clock frequency and one-half the primary clock frequency. The four Y outputs switch in phase and at the same frequency as the clock (CLK) input. The four Q outputs switch at one-half the frequency of CLK.

When the output-enable (\overline{OE}) input is low and the clear (\overline{CLR}) input is high, the Y outputs follow CLK and the Q outputs toggle on low-to-high transitions of CLK. Taking \overline{CLR} low asynchronously resets the Q outputs to the low level. When \overline{OE} is high, the outputs are in the high-impedance state.

The CDC339 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

| INPUTS | | | OUTPUTS | |
|-----------------|------------------|-----|---------|--------------------|
| \overline{OE} | \overline{CLR} | CLK | Y1–Y4 | Q1–Q4 |
| H | X | X | Z | Z |
| L | L | L | L | L |
| L | L | H | H | L |
| L | H | L | L | Q ₀ † |
| L | H | ↑ | H | $\overline{Q_0}$ † |

† The level of the Q outputs before the indicated steady-state input conditions were established.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

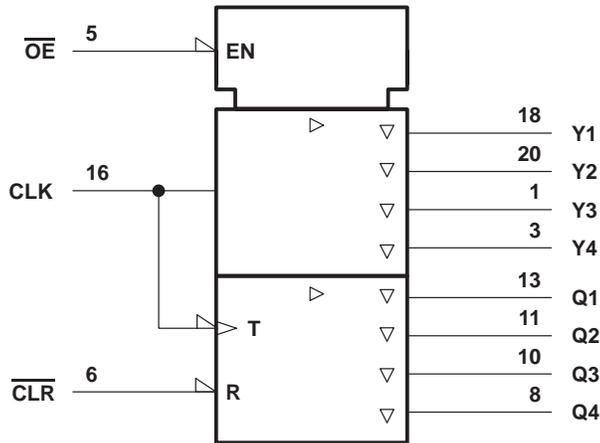
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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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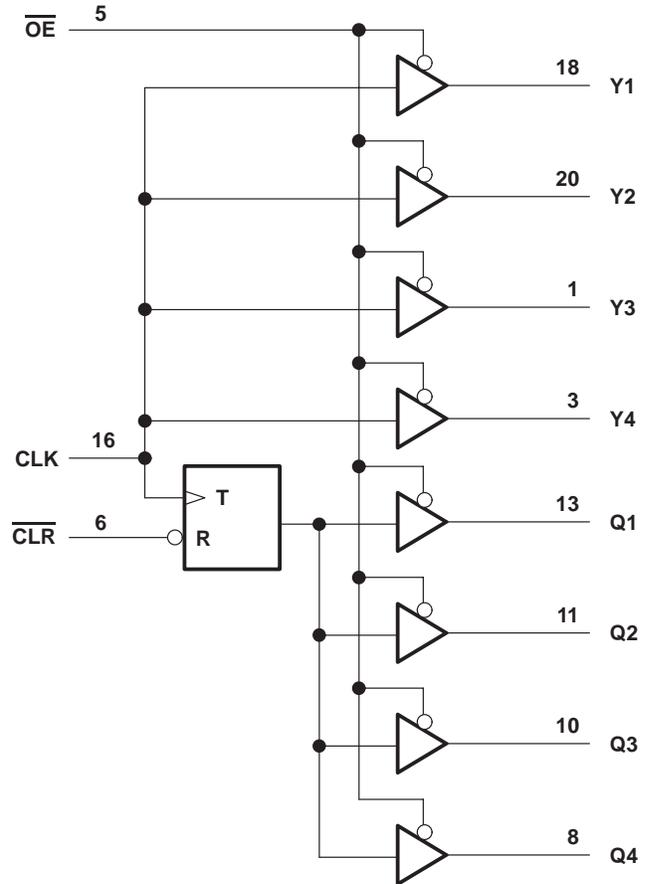
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logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

| | |
|---|--|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the disabled or power-off state, V_O | -0.5 V to 5.5 V |
| Current into any output in the low state, I_O | 96 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | -18 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2): DB package | 0.6 W |
| DW package | 1.6 W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.

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recommended operating conditions (see Note 3)

| | | MIN | MAX | UNIT |
|-------------|--------------------------------|------|----------|------|
| V_{CC} | Supply voltage | 4.75 | 5.25 | V |
| V_{IH} | High-level input voltage | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | V |
| V_I | Input voltage | 0 | V_{CC} | V |
| I_{OH} | High-level output current | | -48 | mA |
| I_{OL} | Low-level output current | | 48 | mA |
| f_{clock} | Input clock frequency | | 80 | MHz |
| T_A | Operating free-air temperature | -40 | 85 | °C |

NOTE 3: Unused pins (input or I/O) must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|--------------------|---|--|------------------|------|------|------|
| V_{IK} | $V_{CC} = 4.75\text{ V}$, | $I_I = -18\text{ mA}$ | | | -1.2 | V |
| V_{OH} | $V_{CC} = 4.75\text{ V}$, | $I_{OH} = -48\text{ mA}$ | 2 | | | V |
| V_{OL} | $V_{CC} = 4.75\text{ V}$, | $I_{OL} = 48\text{ mA}$ | | | 0.5 | V |
| I_{IH} | $V_{CC} = 5.25\text{ V}$, | $V_I = 2.7\text{ V}$ | | | 50 | μA |
| I_{IL} | $V_{CC} = 5.25\text{ V}$, | $V_I = 0.5\text{ V}$ | | | -50 | μA |
| I_{OZ} | $V_{CC} = 5.25\text{ V}$, | $V_O = 2.7\text{ V}$ or 0.5 V | | | ±50 | μA |
| I_{O}^{\ddagger} | $V_{CC} = 5.25\text{ V}$, | $V_O = 2.5\text{ V}$ | -50 | | -180 | mA |
| I_{CC} | $V_{CC} = 5.25\text{ V}$, $V_I = V_{CC}$ or GND | $I_O = 0$, | Outputs high | | 70 | mA |
| | | | Outputs low | | 85 | |
| | | | Outputs disabled | | 70 | |
| C_i | $V_I = 2.5\text{ V}$ or 0.5 V | | | 3 | | pF |
| C_o | $V_O = 2.5\text{ V}$ or 0.5 V | | | 8 | | pF |

† All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

‡ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

| | | MIN | MAX | UNIT |
|-------------|------------------|--|-----|------|
| f_{clock} | Clock frequency | | 80 | MHz |
| t_w | Pulse duration | $\overline{\text{CLR}}$ low | | 4 |
| | | CLK low | | 4 |
| | | CLK high | | 4 |
| t_{su} | Setup time | $\overline{\text{CLR}}$ inactive before $\text{CLK}\uparrow$ | | 2 |
| | Clock duty cycle | 40% | 60% | |

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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

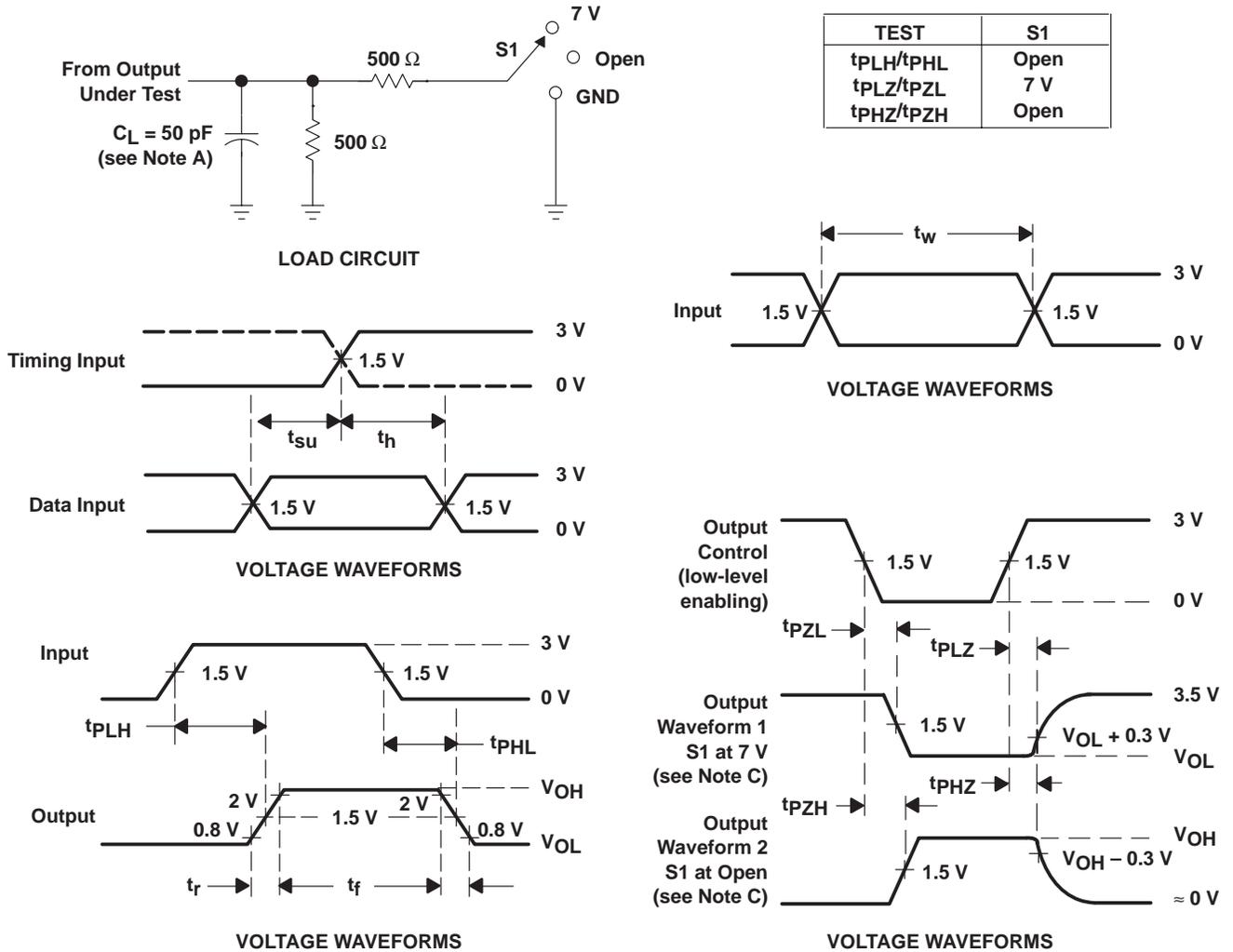
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP† | MAX | UNIT |
|--------------------|-------------------------|-------------|-----|------|------|------|
| f _{max} | | | 80 | | | MHz |
| t _{PLH} | CLK | Any Y or Q | 3 | | 9 | ns |
| t _{PHL} | | | 3 | | 9 | |
| t _{PHL} | $\overline{\text{CLR}}$ | Any Q | 4 | | 9 | ns |
| t _{PZH} | $\overline{\text{OE}}$ | Any Y or Q | 2 | | 7 | ns |
| t _{PZL} | | | 3 | | 7 | |
| t _{PHZ} | $\overline{\text{OE}}$ | Any Y or Q | 2 | | 7 | ns |
| t _{PLZ} | | | 2 | | 7 | |
| t _{sk(o)} | CLK↑ | Y↑ | | | 0.75 | ns |
| | | Q↑ | | | 0.9 | |
| | | Y↑ and Q↑ | | | 0.9 | |
| t _r | | | | 0.9 | | ns |
| t _f | | | | 0.7 | | ns |

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

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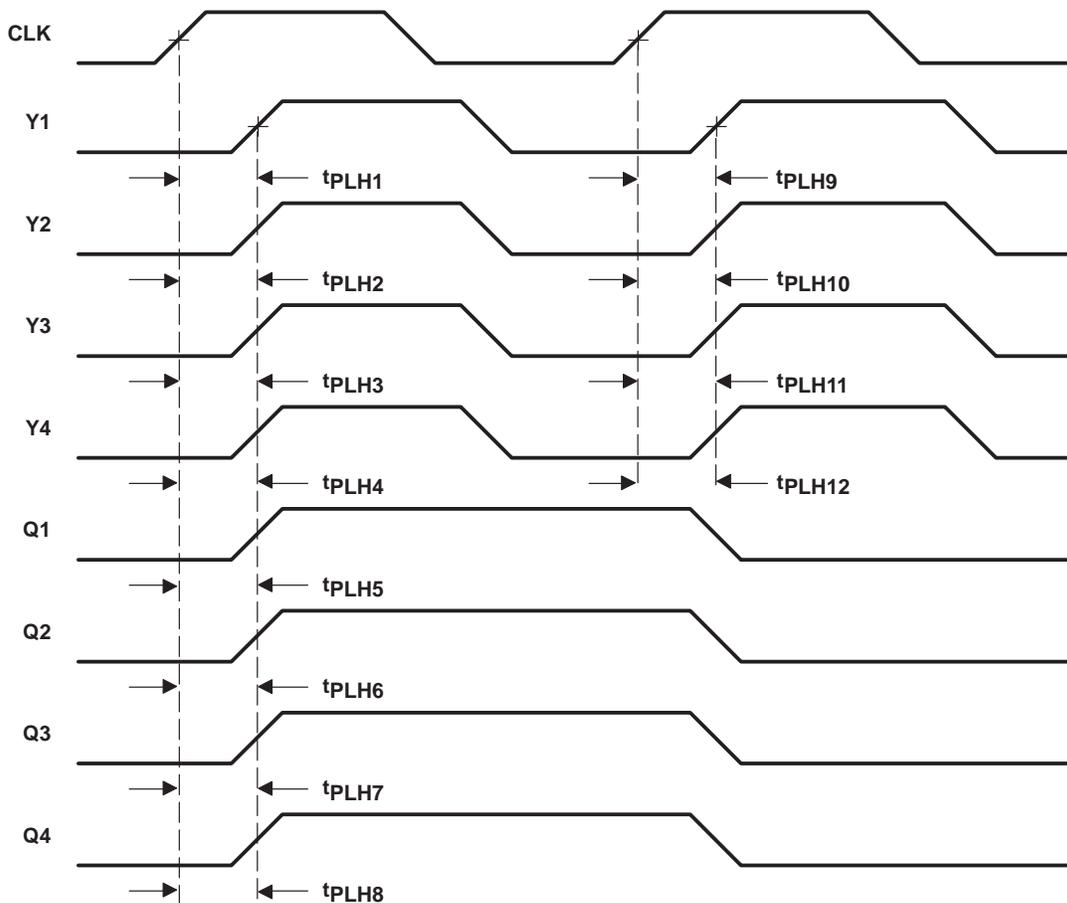
PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 D. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Output skew, $t_{sk(o)}$, from $CLK\uparrow$ to $Y\uparrow$, is calculated as the greater of the difference between the fastest and slowest of t_{PLHn} ($n = 1, 2, 3, 4$) or t_{PLHn} ($n = 9, 10, 11, 12$).
- B. Output skew, $t_{sk(o)}$, from $CLK\uparrow$ to $Q\uparrow$, is calculated as the greater of the difference between the fastest and slowest of t_{PLHn} ($n = 5, 6, 7, 8$).
- C. Output skew, $t_{sk(o)}$, from $CLK\uparrow$ to $Y\uparrow$ and $Q\uparrow$, is calculated as the greater of the difference between the fastest and slowest of t_{PLHn} ($n = 1, 2, \dots, 8$).

Figure 2. Skew Waveforms and Calculations

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