DIRECT RAMBUS™ CLOCK GENERATOR

- **400-MHz Differential Clock Source for Direct Rambus™ Memory Systems for an 800-MHz Data Transfer Rate**
- **Synchronizes the Clock Domains of the Rambus Channel With an External System or Processor Clock**
- **Three Power Operating Modes to Minimize Power for Mobile and Other Power-Sensitive Applications**
- **Operates From a Single 3.3-V Supply and 120 mW at 300 MHz (Typ)**
- **Packaged in a Shrink Small-Outline Package (DBQ)**
- **Supports Frequency Multipliers: 4, 6, 8, 16/3**
- **No External Components Required for PLL**
- **Supports Independent Channel Clocking**
- **Spread Spectrum Clocking Tracking Capability to Reduce EMI**
- **Designed for Use With TI's 133-MHz Clock Synthesizers CDC924 and CDC921**

- **Cycle-Cycle Jitter Is Less Than 50 ps at 400 MHz**
- **Certified by Gigatest Labs to Exceed the Rambus DRCG Validation Requirement**
- **Supports Industrial Temperature Range of −40°C to 85°C**

DBQ PACKAGE
(TOP VIEW)

$V_{DD}IR$	1	24	S0
REFCLK	2	23	S1
$V_{DD}P$	3	22	$V_{DD}O$
GNDP	4	21	GNDO
GNDI	5	20	CLK
PCLKM	6	19	NC
SYNCLKN	7	18	CLKB
GNDC	8	17	GNDO
$V_{DD}C$	9	16	$V_{DD}O$
$V_{DD}IPD$	10	15	MULT0
STOPB	11	14	MULT1
PWRDNB	12	13	S2
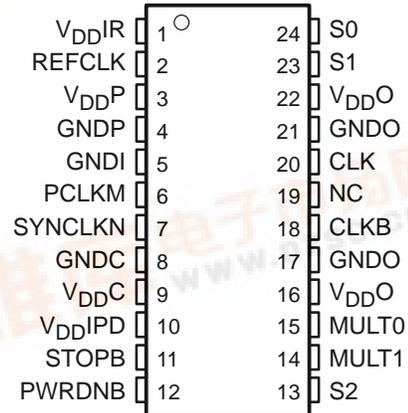
NC – No internal connection

description

The Direct Rambus clock generator (DRCG) provides the necessary clock signals to support a Direct Rambus memory subsystem. It includes signals to synchronize the Direct Rambus channel clock to an external system or processor clock. It is designed to support Direct Rambus memory on a desktop, workstation, server, and mobile PC motherboards. DRCG also provides an off-the-shelf solution for a broad range of Direct Rambus memory applications.

The DRCG provides clock multiplication and phase alignment for a Direct Rambus memory subsystem to enable synchronous communication between the Rambus channel and ASIC clock domains. In a Direct Rambus memory subsystem, a system clock source provides the REFCLK and PCLK clock references to the DRCG and memory controller, respectively. The DRCG multiplies REFCLK and drives a high-speed BUSCLK to RDRAMs and the memory controller. Gear ratio logic in the memory controller divides the PCLK and BUSCLK frequencies by ratios M and N such that PCLKM = SYNCLKN, where SYNCLK = BUSCLK/4. The DRCG detects the phase difference between PCLKM and SYNCLKN and adjusts the phase of BUSCLK such that the skew between PCLKM and SYNCLKN is minimized. This allows data to be transferred across the SYNCLK/PCLK boundary without incurring additional latency.

User control is provided by multiply and mode selection terminals. The multiply terminals provide selection of one of four clock frequency multiply ratios, generating BUSCLK frequencies ranging from 267 MHz to 400 MHz with clock references ranging from 33 MHz to 100 MHz. The mode select terminals can be used to select a bypass mode where the frequency multiplied reference clock is directly output to the Rambus channel for systems where synchronization between the Rambus clock and a system clock is not required. Test modes are provided to bypass the PLL and output REFCLK on the Rambus channel and to place the outputs in a high-impedance state for board testing.

The CDCR83 is characterized for operation over free-air temperatures of −40°C to 85°C.

Direct Rambus and Rambus are trademarks of Rambus Inc.

TEXAS INSTRUMENTS

functional block diagram
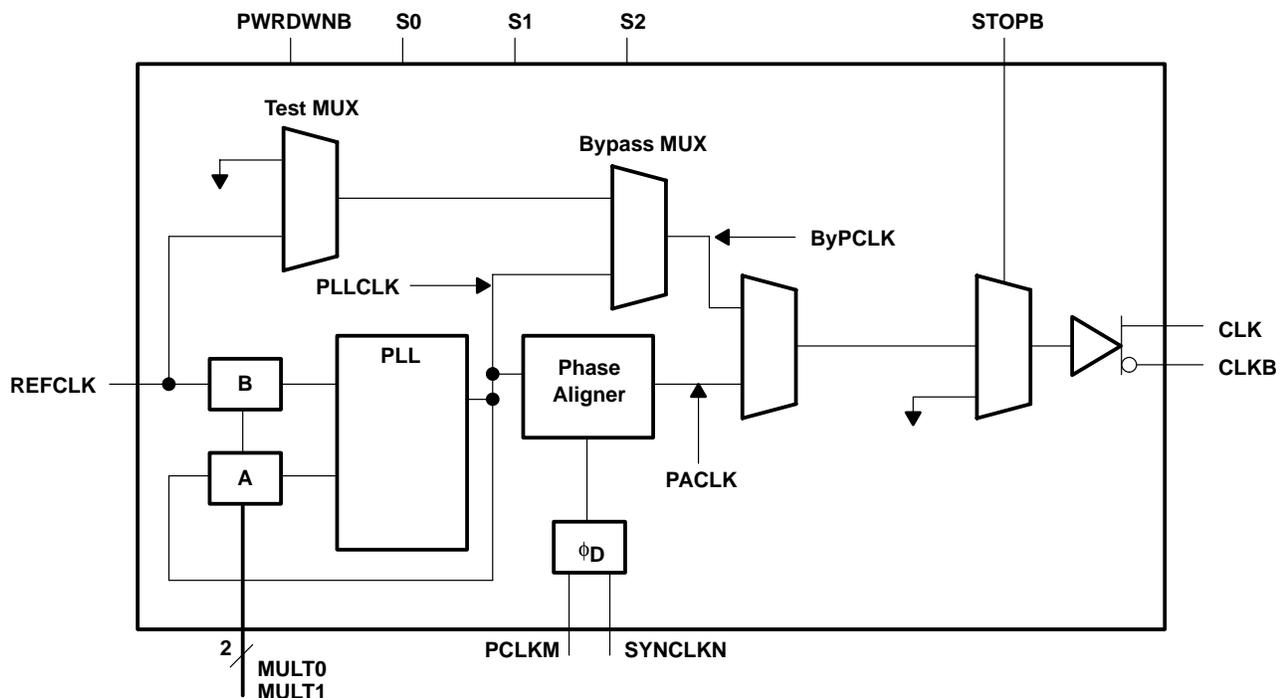
FUNCTION TABLE†

MODE	S0	S1	S2	CLK	CLKB
Normal	0	0	0	Phase aligned clock	Phase aligned clock B
Bypass	1	0	0	PLLCLK	PLLCLKB
Test	1	1	0	REFCLK	REFCLKB
Output test (OE)	0	1	X	Hi-Z	Hi-Z
Reserved	0	0	1	—	—
Reserved	1	0	1	—	—
Reserved	1	1	1	Hi-Z	Hi-Z

† X = don't care, Hi-Z = high impedance

Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CLK	20	O	Output clock
CLKB	18	O	Output clock (complement)
GNDC	8		GND for phase aligner
GNDI	5		GND for control inputs
GNDO	17, 21		GND for clock outputs
GNDP	4		GND for PLL
MULT0	15	I	PLL multiplier select
MULT1	14	I	PLL multiplier select
NC	19		Not used
PCLKM	6	I	Phase detector input
PWRDNB	12	I	Active low power down
REFCLK	2	I	Reference clock
S0	24	I	Mode control
S1	23	I	Mode control
S2	13	I	Mode control
STOPB	11	I	Active low output disable
SYNCLKN	7	I	Phase detector input
$V_{DD}C$	9		V_{DD} for phase aligner
$V_{DD}IPD$	10		Reference voltage for phase detector inputs and STOPB
$V_{DD}IR$	1		Reference voltage for REFCLK
$V_{DD}O$	16, 22		V_{DD} for clock outputs
$V_{DD}P$	3		V_{DD} for PLL

PLL divider selection

Table 1 lists the supported REFCLK and BUSCLK frequencies. Other REFCLK frequencies are permitted, provided that (267 MHz < BUSCLK < 400 MHz) and (33 MHz < REFCLK < 100 MHz).

Table 1. REFCLK and BUSCLK Frequencies

MULT0	MULT1	REFCLK (MHz)	MULTIPLY RATIO	BUSCLK (MHz)
0	0	67	4	267
0	1	50	6	300
0	1	67	6	400
1	1	33	8	267
1	1	50	8	400
1	0	67	16/3	356

Table 2. Clock Output Driver States

STATE	PWRDNB	STOPB	CLK	CLKB
Powerdown	0	X	GND	GND
CLK stop	1	0	$V_{X, STOP}$	$V_{X, STOP}$
Normal	1	1	PACLK/PLLCLK/REFCLK[†]	PACLKB/PLLCLKB/REFCLKB

[†] Depending on the state of S0, S1, and S2

absolute maximum ratings over operating free-air temperature (unless otherwise noted)[†]

Supply voltage range, V_{DD} (see Note 1) . . . . –0.5 V to 4 V
Output voltage range, V_O, at any output terminal . . . . –0.5 V to V_{DD} + 0.5 V
Input voltage range, V_I, at any input terminal . . . . –0.5 V to V_{DD} + 0.5 V
Continuous total power dissipation . . . . see Dissipation Rating Table
Operating free-air temperature range, T_A . . . . –40°C to 85°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$[‡]	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DBQ	1400 mW	11 mW/°C	905 mW	740 mW

[‡] This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

TEXAS INSTRUMENTS

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	3.135	3.3	3.465	V
High-level input voltage, V_{IH} (CMOS)	$0.7 \times V_{DD}$			V
Low-level input voltage, V_{IL} (CMOS)			$0.3 \times V_{DD}$	V
Initial phase error at phase detector inputs (required range for phase aligner)	$-0.5 \times t_{c(PD)}$		$0.5 \times t_{c(PD)}$	
REFCLK low-level input voltage, V_{IL}			$0.3 \times V_{DD}IR$	V
REFCLK high-level input voltage, V_{IH}	$0.7 \times V_{DD}IR$			V
Input signal low voltage, V_{IL} (STOPB)			$0.3 \times V_{DD}IPD$	V
Input signal high voltage, V_{IH} (STOPB)	$0.7 \times V_{DD}IPD$			V
Input reference voltage for (REFCLK) ($V_{DD}IR$)	1.235		3.465	V
Input reference voltage for (PCLKM and SYSCLKN) ($V_{DD}IPD$)	1.235		3.465	V
High-level output current, I_{OH}			−16	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	−40		85	°C

timing requirements

	MIN	MAX	UNIT
Input cycle time, $t_{c(in)}$	10	40	ns
Input cycle-to-cycle jitter		250	ps
Input duty cycle over 10,000 cycles	40%	60%	
Input frequency modulation, f_{mod}	30	33	kHz
Modulation index, nonlinear maximum 0.5%		0.6%	
Phase detector input cycle time (PCLKM and SYNCLKN)	30	100	ns
Input slew rate, SR	1	4	V/ns
Input duty cycle (PCLKM and SYNCLKN)	25%	75%	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{O(STOP)}$	Output voltage during CLK Stop (STOPB = 0)	See Figure 1		1.1		2	
$V_{O(X)}$	Output crossing-point voltage	See Figure 1 and Figure 6		1.3		1.8	V
V_O	Output voltage swing	See Figure 1		0.4		0.6	V
V_{IK}	Input clamp voltage	V_{DD} = 3.135 V, I_I = −18 mA				−1.2	V
V_{OH}	High-level output voltage	See Figure 1				2	V
		V_{DD} = min to max, I_{OH} = −1 mA		V_{DD} − 0.1 V			
		V_{DD} = 3.135 V, I_{OH} = −16 mA		2.4			
V_{OL}	Low-level output voltage	See Figure 1		1			V
		V_{DD} = min to max, I_{OL} = 1 mA				0.1	
		V_{DD} = 3.135 V, I_{OL} = 16 mA				0.5	
I_{OH}	High-level output current	V_{DD} = 3.135 V, V_O = 1 V		−32	−52		mA
		V_{DD} = 3.3 V, V_O = 1.65 V			−51		
		V_{DD} = 3.465 V, V_O = 3.135 V			−14.5	−21	
I_{OL}	Low-level output current	V_{DD} = 3.135 V, V_O = 1.95 V		43	61.5		mA
		V_{DD} = 3.3 V, V_O = 1.65 V			65		
		V_{DD} = 3.465 V, V_O = 0.4 V			25.5	36	
I_{OZ}	High-impedance-state output current	S0 = 0, S1 = 1				±10	µA
$I_{OZ(STOP)}$	High-impedance-state output current during CLK stop	Stop = 0, V_O = GND or V_{DD}				±100	µA
$I_{OZ(PD)}$	High-impedance-state output current in power-down state	PWRDNB = 0, V_O = GND or V_{DD}		−10		100	µA
I_{IH}	High-level input current	REFCLK, PCLKM, SYNCLKN, STOPB	V_{DD} = 3.465 V, V_I = V_{DD}			10	µA
		PWRDNB, S0, S1, S2, MULT0, MULT1	V_{DD} = 3.465 V, V_I = V_{DD}			10	
I_{IL}	Low-level input current	REFCLK, PCLKM, SYNCLKN, STOPB	V_{DD} = 3.465 V, V_I = 0			−10	µA
		PWRDNB, S0, S1, S2, MULT0, MULT1	V_{DD} = 3.465 V, V_I = 0			−10	
Z_O	Output impedance	High state	R_I at I_O −14.5 mA to −16.5 mA	15	35	50	Ω
		Low state	R_I at I_O 14.5 mA to 16.5 mA	11	17	35	
	Reference current	V_{DD}IR, V_{DD}IPD V_{DD} = 3.465 V	PWRDNB = 0			50	µA
			PWRDNB = 1			0.5	mA
C_I	Input capacitance	V_I = V_{DD} or GND			2		pF
C_O	Output capacitance	V_O = V_{DD} or GND			3		pF
$I_{DD(PD)}$	Supply current in power-down state	REFCLK = 0 MHz to 100 MHz, PWDNB = 0, STOPB = 1				100	µA
$I_{DD(CLKSTOP)}$	Supply current in CLK stop state	BUSCLK configured for 400 MHz				30	mA
$I_{DD(NORMAL)}$	Supply current in normal state	BUSCLK = 400 MHz				70	mA

† V_{DD} refers to any of the following; V_{DD}, V_{DD}IPD, V_{DD}IR, V_{DD}O, V_{DD}C, and V_{DD}P
‡ All typical values are at V_{DD} = 3.3 V, T_A = 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER				TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{c(out)}$	Clock output cycle time				2.5		3.75	ns
$t_{(jitter)}$	Total cycle jitter over 1, 2, 3, 4, 5, or 6 clock cycles	Infinite and stopped phase alignment	267 MHz	See Figure 3			80	ps
			300 MHz				70	
			356 MHz				60	
			400 MHz				50	
$t_{(phase)}$	Phase detector phase error for distributed loop			Static phase error‡	−100		100	ps
$t_{(phase, SSC)}$	PLL output phase error when tracking SSC			Dynamic phase error‡	−100		100	ps
$t_{(DC)}$	Output duty cycle over 10,000 cycles			See Figure 4	45%		55%	
$t_{(DC, err)}$	Output cycle-to-cycle duty cycle error	Infinite and stopped phase alignment	267 MHz	See Figure 5			80	ps
			300 MHz				70	
			356 MHz				60	
			400 MHz				50	
t_r, t_f	Output rise and fall times (measured at 20%–80% of output voltage)			See Figure 7	160		400	ps
Δt	Difference between rise and fall times on a single device (20%–80%) $|t_f − t_r|$			See Figure 7			100	ps

† All typical values are at V_{DD} = 3.3 V, T_A = 25°C.
‡ Assured by design

state transition latency specifications

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{(powerup)}$	Delay time, PWRDNB↑ to CLK/CLKB output settled (excluding $t_{(DISTLOCK)}$)	Powerdown	Normal	See Figure 8			3	ms
	Delay time, PWRDNB↑ to internal PLL and clock are on and settled						3	
$t_{(VDDpowerup)}$	Delay time, power up to CLK/CLKB output settled	V_{DD}	Normal	See Figure 8			3	ms
	Delay time, power up to internal PLL and clock are on and settled						3	
$t_{(MULT)}$	MULT0 and MULT1 change to CLK/CLKB output resettled (excluding $t_{(DISTLOCK)}$)	Normal	Normal	See Figure 9			1	ms
$t_{(CLKON)}$	STOPB↑ to CLK/CLKB glitch-free clock edges	CLK Stop	Normal	See Figure 10			10	ns
$t_{(CLKSETL)}$	STOPB↑ to CLK/CLKB output settled to within 50 ps of the phase before STOPB was disabled	CLK Stop	Normal	See Figure 10			20	cycles
$t_{(CLKOFF)}$	STOPB↓ to CLK/CLKB output disabled	Normal	CLK Stop	See Figure 10			5	ns

† All typical values are at V_{DD} = 3.3 V, T_A = 25°C.

state transition latency specifications (continued)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t(powerdown)	Delay time, PWRDNB↓ to the device in the power-down mode	Normal	Powerdown	See Figure 8			1	ms
t(STOP)	Maximum time in CLKSTOP (STOPB = 0) before reentering normal mode (STOPB = 1)	STOPB	Normal	See Figure 10			100	µs
t(ON)	Minimum time in normal mode (STOPB = 1) before reentering CLKSTOP (STOPB = 0)	Normal	CLK stop	See Figure 10	100			ms
t(DISTLOCK)	Time from when CLK/CLKB output is settled to when the phase error between SYNCLKN and PCLKM falls within t(phase)	Unlocked	Locked				5	ms

† All typical values are at V_{DD} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION
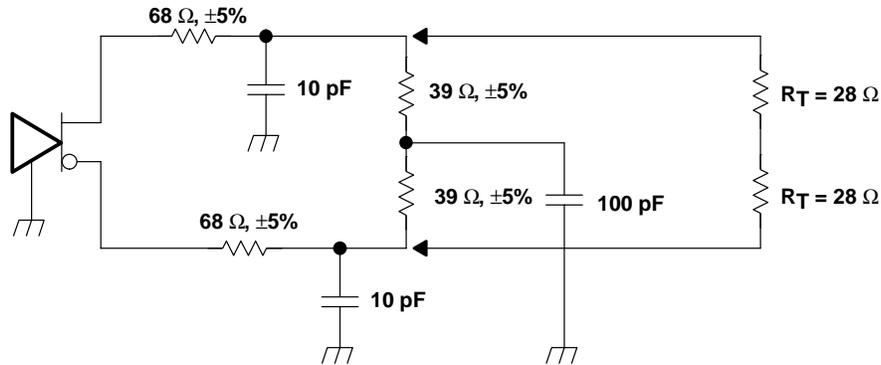
Figure 1. Test Load and Voltage Definitions ($V_{O(STOP)}$, $V_{O(X)}$, V_O, V_{OH}, V_{OL})
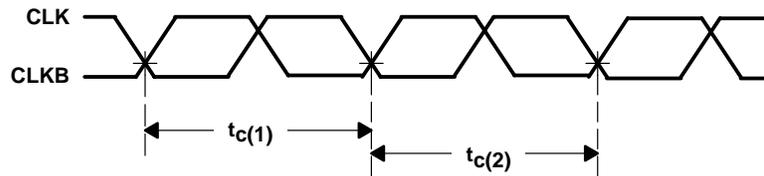
Cycle-to-cycle jitter = | $t_{c(1)}$ − $t_{c(2)}$| over 10000 consecutive cycles

Figure 2. Cycle-to-Cycle Jitter
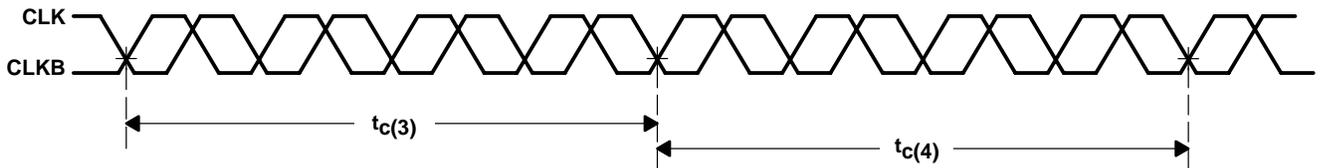
Cycle-to-cycle jitter = | $t_{c(3)}$ − $t_{c(4)}$| over 10000 consecutive cycles

Figure 3. Short Term Cycle-to-Cycle Jitter Over Four Cycles

TEXAS
INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

CLK
CLKB

$t_{pd(1)}$

$t_{c(5)}$

Duty cycle = $(t_{pd(1)}/t_{c(5)})$
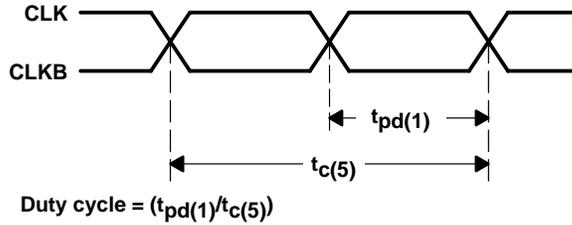
Figure 4. Output Duty Cycle

CLK
CLKB

$t_{pd(2)}$ $t_{pd(3)}$

$t_{c(6)}$ $t_{c(7)}$

Duty cycle error = $t_{pd(2)} - t_{pd(3)}$
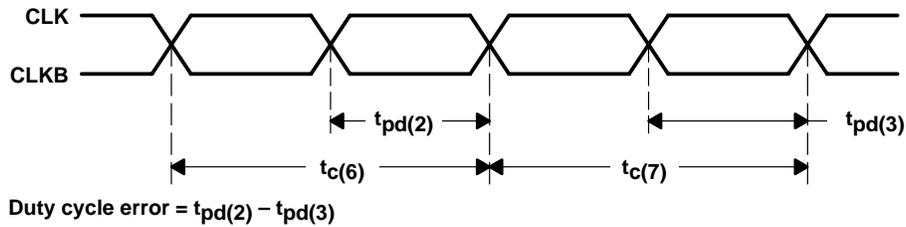
Figure 5. Duty Cycle Error (Cycle-to-Cycle)

CLK

$V_{O(X)+}$
$V_{O(X), nom}$
$V_{O(X)-}$

CLKB
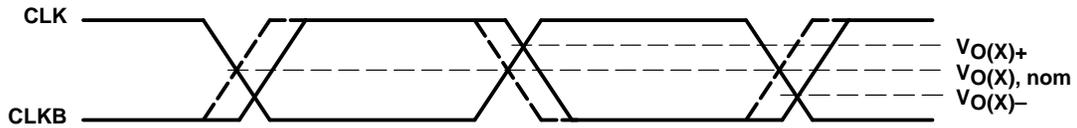
Figure 6. Crossing-Point Voltage

80% V_{OH}
20%

V_{OL}

t_r t_f
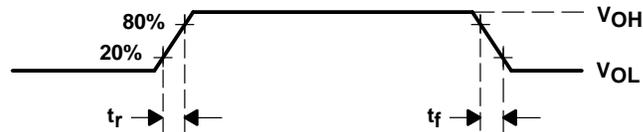
Figure 7. Voltage Waveforms

PWRDNB

$t_{(power\ up)}$ $t_{(power\ down)}$

CLK/CLKB
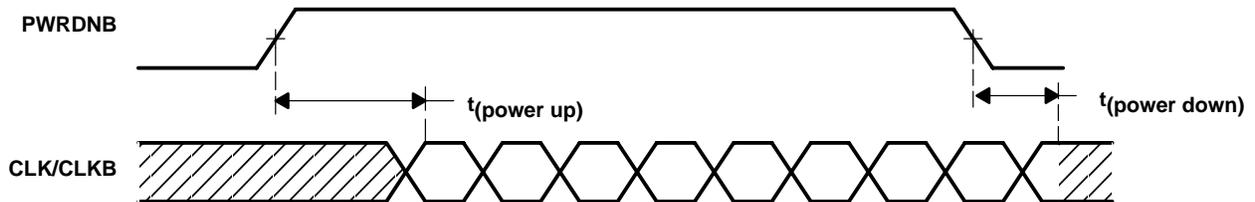
Figure 8. PWRDNB Transition Timings

TEXAS
INSTRUMENTS

PARAMETER MEASUREMENT INFORMATION

MULT0 and/or MULT1

$t_{(MULT)}$

CLK/CLKB
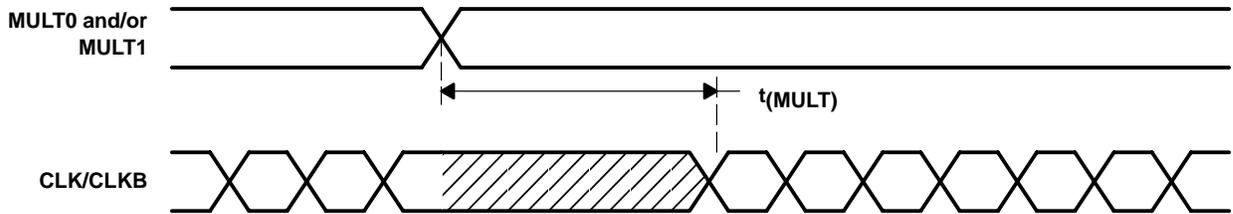
Figure 9. MULT Transition Timings

$t_{(ON)}$

$t_{(STOP)}$

STOPB

$t_{(CLKSETL)}$

$t_{(CLKOFF)}$
(see Note A)

$t_{(CLKON)}$
(see Note A)

CLK/CLKB

Output clock not specified glitches ok

Clock enabled and glitch free

Clock output settled within 50 ps of the phase before disabled
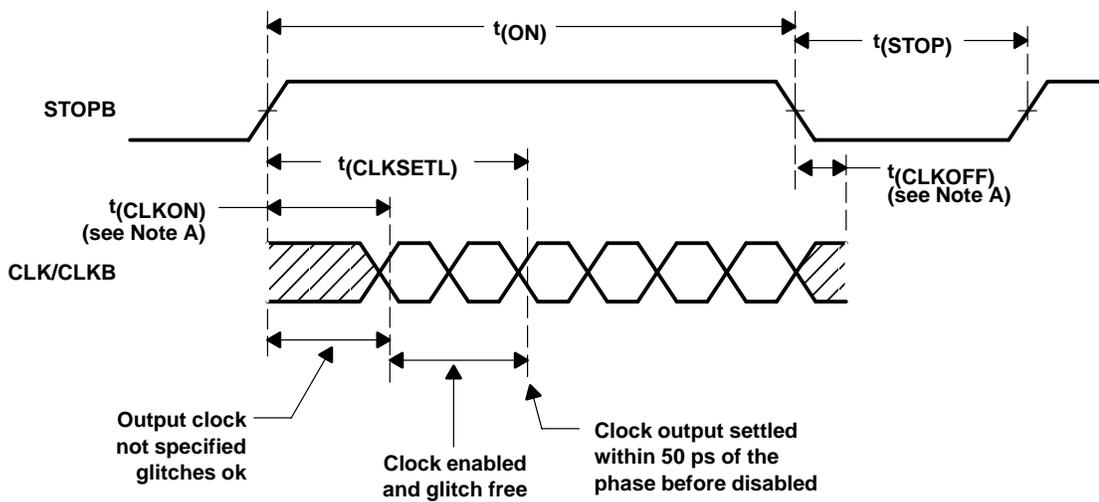
NOTE A: $V_{ref} = V_O \pm 200$ mV

Figure 10. STOPB Transition Timings

MECHANICAL DATA

DBQ (R-PDSO-G)** PLASTIC SMALL-OUTLINE PACKAGE

24-PIN SHOWN

| | PINS ** | 16 | 20 | 24 |
DIM				
A MAX		0.197 (5,00)	0.344 (8,74)	0.344 (8,74)
A MIN		0.188 (4,78)	0.337 (8,56)	0.337 (8,56)

4073301/C 02/97
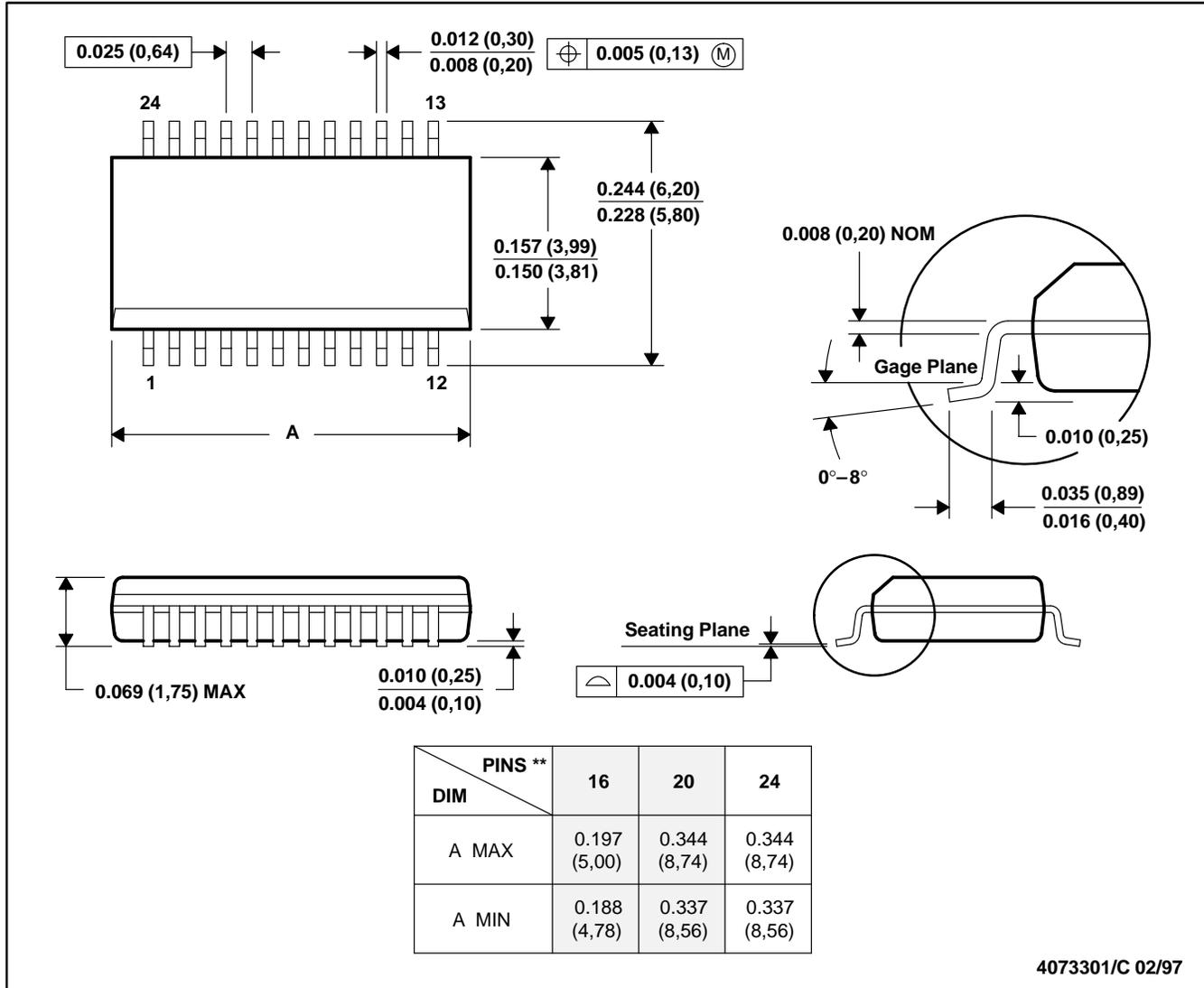
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-137

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third–party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265