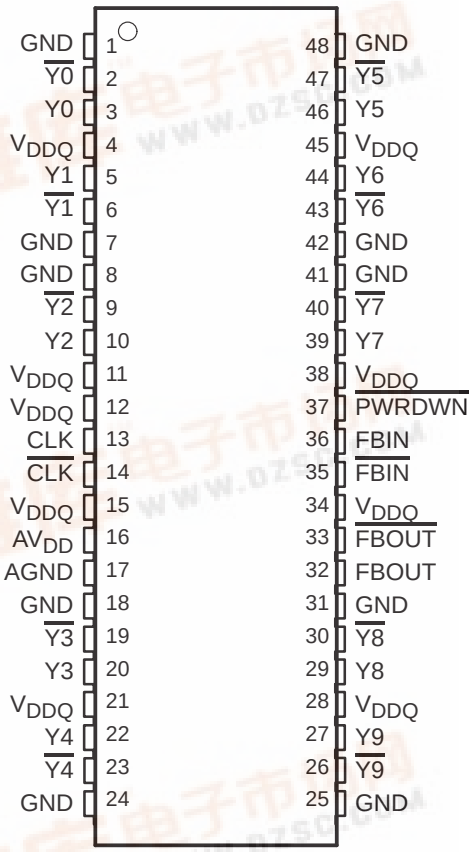
CDCV857
2.5-V PHASE LOCK LOOP CLOCK DRIVER

SCAS645A – AUGUST 2000 – REVISED OCTOBER 2000

- **Phase-Lock Loop Clock Driver for Double Data-Rate Synchronous DRAM Applications**
- **Spread Spectrum Clock Compatible**
- **Operating Frequency: 60 to 200 MHz**
- **Low Jitter (cyc–cyc): ±75 ps**
- **Distributes One Differential Clock Input to Ten Differential Outputs**
- **Three-State Outputs When the Input Differential Clocks Are <20 MHz**
- **Operates From Dual 2.5-V Supplies**
- **48-Pin TSSOP Package**
- **Consumes < 200-μA Quiescent Current**
- **External Feedback PIN (FBIN, $\overline{\text{FBIN}}$) Are Used to Synchronize the Outputs to the Input Clocks**

DGG PACKAGE
(TOP VIEW)



description

The CDCV857 is a high-performance, low-skew, low-jitter zero delay buffer that distributes a differential clock input pair (CLK, $\overline{\text{CLK}}$) to ten differential pairs of clock outputs (Y[0:9], $\overline{\text{Y[0:9]}}$) and one differential pair of feedback clock output (FBOUT, $\overline{\text{FBOUT}}$). The clock outputs are controlled by the clock inputs (CLK, $\overline{\text{CLK}}$), the feedback clocks (FBIN, $\overline{\text{FBIN}}$), and the analog power input (AV_{DD}). When $\overline{\text{PWRDWN}}$ is high, the outputs switch in phase and frequency with CLK. When $\overline{\text{PWRDWN}}$ is low, all outputs are disabled to high impedance state (3-state), and the PLL is shut down (low power mode). The device also enters this low power mode when the input frequency falls below a suggested detection frequency that is below 20 MHz (typical 10 MHz). An input frequency detection circuit will detect the low frequency condition and after applying a >20 MHz input signal this detection circuit turns on the PLL again and enables the outputs.

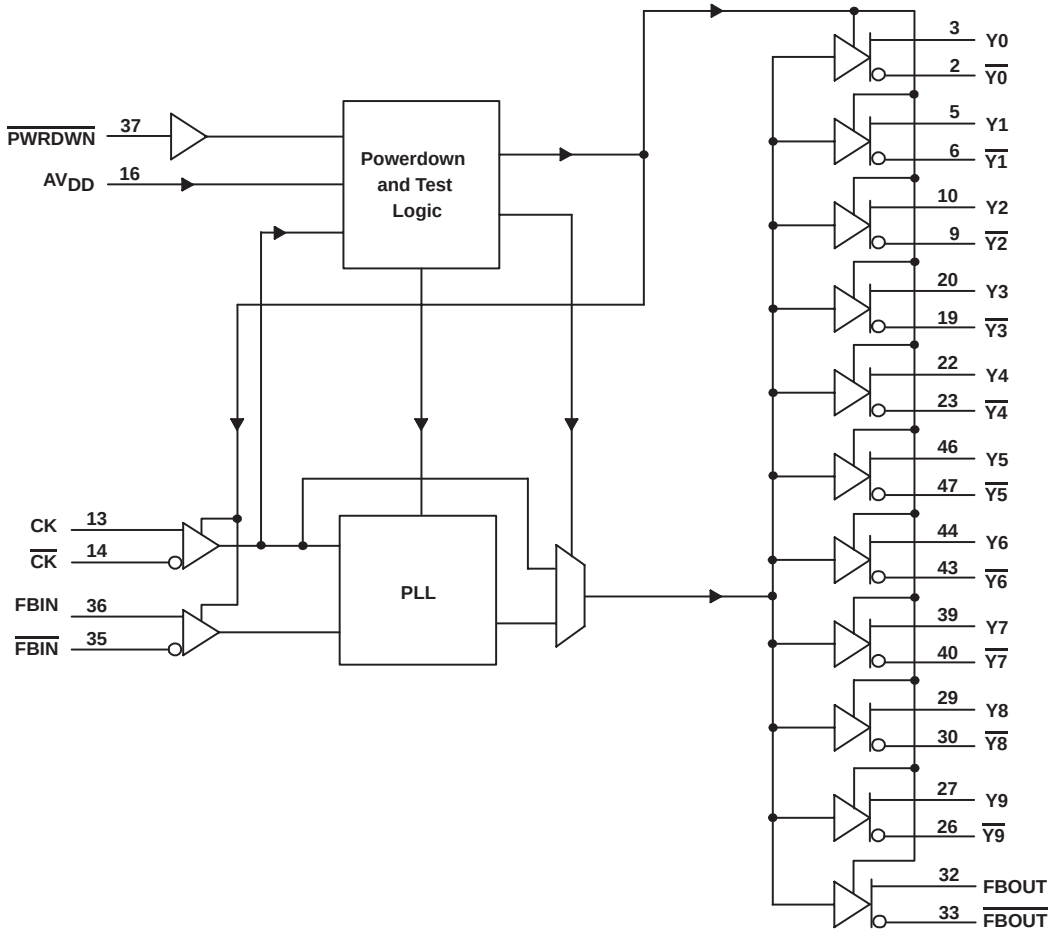
When AV_{DD} is strapped low, the PLL is turned off and bypassed for test purposes. The CDCV857 is also able to track spread spectrum clocking for reduced EMI.

Since the CDCV857 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up. The CDCV857 is characterized for operation from 0°C to 85°C.

FUNCTION TABLE
(Select Functions)

INPUTS				OUTPUTS				PLL
AV_{DD}	$\overline{PWRDWN}$	CLK	$\overline{CLK}$	Y[0:9]	$\overline{Y[0:9]}$	FBOUT	$\overline{FBOUT}$	
GND	H	L	H	L	H	L	H	Bypassed/Off
GND	H	H	L	H	L	H	L	Bypassed/Off
X	L	L	H	Z	Z	Z	Z	Off
X	L	H	L	Z	Z	Z	Z	Off
2.5 V (nom)	H	L	H	L	H	L	H	On
2.5 V (nom)	H	H	L	H	L	H	L	On
2.5 V (nom)	X	<20 MHz	<20 MHz	Z	Z	Z	Z	Off

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	17		Ground for 2.5-V analog supply
AV_{DD}	16		2.5-V Analog supply
CLK, $\overline{CLK}$	13, 14	I	Differential clock input
$\overline{FBIN}$, FBIN	35, 36	I	Feedback differential clock input
FBOUT, $\overline{FBOUT}$	32, 33	O	Feedback differential clock output
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48		Ground
$\overline{PWRDWN}$	37	I	Output enable for Y and $\overline{Y}$
V_{DDQ}	4, 11, 12, 15, 21, 28, 34, 38, 45		2.5-V Supply
Y[0:9]	3, 5, 10, 20, 22, 27, 29, 39, 44, 46	O	Buffered output copies of input clock, CLK
$\overline{Y[0:9]}$	2, 6, 9, 19, 23, 26, 30, 40, 43, 47	O	Buffered output copies of input clock, $\overline{CLK}$

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{DDQ}, AV_{DD} . . . . . 0.5 V to 3.6 V
Input voltage range, V_I (see Notes 1 and 2) . . . . . –0.5 V to V_{DDQ} 0.5 V
Output voltage range, V_O (see Notes 1 and 2) . . . . . –0.5 V to V_{DDQ} 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{DDQ}$) . . . . . ±50 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{DDQ}$) . . . . . ±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{DDQ}) . . . . . ±50 mA
Continuous current to GND or V_{DDQ} . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package . . . . . 89°C/W
Storage temperature range T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 3.6 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 4)

			MIN	TYP	MAX	UNIT
Supply voltage, V_{DDQ}, AV_{DD}			2.3		2.7	V
Low level input voltage, V_{IL}	CLK, $\overline{CLK}$, FBIN, $\overline{FBIN}$				$V_{DDQ}/2 - 0.18$	V
	$\overline{PWRDWN}$		–0.3		0.7	
High level input voltage, V_{IH}	CLK, $\overline{CLK}$, FBIN, $\overline{FBIN}$		$V_{DDQ}/2 + 0.18$			V
	$\overline{PWRDWN}$		1.7		$V_{DDQ} + 0.3$	
DC input signal voltage (see Note 5)			–0.3		V_{DDQ}	V
Differential input signal voltage, V_{ID} (see Note 6)	DC	CLK, FBIN	0.36		$V_{DDQ} + 0.6$	V
	AC	CLK, FBIN	0.7		$V_{DDQ} + 0.6$	
Output differential cross-voltage, V_{OX} (see Note 7)			$V_{DDQ}/2 - 0.2$	$V_{DDQ}/2$	$V_{DDQ}/2 + 0.2$	V
Input differential pair cross-voltage, V_{IX} (see Note 7)			$V_{DDQ}/2 - 0.2$		$V_{DDQ}/2 + 0.2$	V
High-level output current, I_{OH}					–12	mA
Low-level output current, I_{OL}					12	mA
Input slew rate, SR			1		4	V/ns
Operating free-air temperature, T_A			0		85	°C

NOTES: 4. Unused inputs must be held high or low to prevent them from floating.
5. DC input signal voltage specifies the allowable dc execution of differential input.
6. Differential input signal voltage specifies the differential voltage |VTR – VCP| required for switching, where VTR is the true input level and VCP is the complementary input level.
7. Differential cross-point voltage is expected to track variations of VCC and is the voltage at which the differential signals must be crossing.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input voltage	All inputs	V_{DDQ} = 2.3 V,	I_I = –18 mA			–1.2	V
V_{OH}	High-level output voltage		V_{DDQ} = min to max,	I_{OH} = –1 mA	V_{DDQ}– 0.1			V
			V_{DDQ} = 2.3 V,	I_{OH} = –12 mA	1.7			
V_{OL}	Low-level output voltage		V_{DDQ} = min to max,	I_{OL} = 1 mA			0.1	V
			V_{DDQ} = 2.3 V,	I_{OL} = 12 mA			0.6	
I_{OH}	High-level output current		V_{DDQ} = 2.3 V,	V_O = 1 V	–18	–32		mA
I_{OL}	Low-level output current		V_{DDQ} = 2.3 V,	V_O = 1.2 V	26	35		mA
V_O	Output voltage swing		Differential outputs are terminated with 120 Ω		1.1		V_{DDQ}– 0.4	V
V_{OX}	Output differential cross-voltage§				V_{DDQ}/2 – 0.2	V_{DDQ}/2	V_{DDQ}/2 + 0.2	
I_I	Input current		V_{DDQ} = 2.7 V,	V_I = 0 V to 2.7 V			±10	µA
I_{OZ}	High-impedance-state output current		V_{DDQ} = 2.7 V,	V_O= V_{DDQ} or GND			±10	µA
I_{DDPD}	Power down current on V_{DDQ} + AV_{DD}		CLK and $\overline{CLK}$ = 0 MHz; $\overline{PWRDWN}$ = Low; Σ of I_{DD} and AI_{DD}			100	200	µA
I_{DD}	Dynamic current on V_{DDQ}		all outputs loaded as shown in Figure 3	f_O = 200 MHz		275	330	mA
				f_O = 167 MHz		250	300	
AI_{DD}	Supply current on AV_{DD}		f_O = 200 MHz			10	12	mA
			f_O = 167 MHz			8	10	
C_I	Input capacitance		V_{CC} = 2.5 V	V_I = V_{CC} or GND	2	2.5	3	pF
C_O	Output capacitance		V_{CC} = 2.5 V	V_O = V_{CC} or GND	2.5	3	3.5	pF

† All typical values are at respective nominal V_{DDQ}.
‡ The value of V_{OC} is expected to be |VTR + VCP|/2. In case of each clock directly terminated by a 120-Ω resistor, where VTR is the true input signal voltage and VCP is the complementary input signal voltage.
§ Differential cross-point voltage is expected to track variations of VDDQ and is the voltage at which the differential signals must be crossing.

timing requirements over recommended ranges of supply voltage and operating free-air temperature

		MIN	MAX	UNIT
f_{CK}	Operating clock frequency	60	200	MHz
	Application clock frequency			
	Input clock duty cycle	40%	60%	
	Stabilization time¶ (PLL mode)		10	µs
	Stabilization time¶ (Bypass mode)		30	ns

¶ Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

switching characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}‡	Low to high level propagation delay time	Test mode/CLK to any output			4.5		ns
t_{PHL}‡	High-to low level propagation delay time	Test mode/CLK to any output			4.5		ns
$t_{jit(per)}$§	Jitter (period), See Figure 6	66 MHz		–90		90	ps
		100/133/167/200 MHz		–75		75	ps
$t_{jit(cc)}$§	Jitter (cycle-to-cycle), See Figure 3	66 MHz		–180		180	ps
		100/133/167/200 MHz		–75		75	
$t_{jit(hper)}$§	Half-period jitter, See Figure 7	66 MHz		–160		160	ps
		100/133/167/200 MHz		–100		100	
$t_{slr(i)}$	Input clock slew rate, See Figure 8			1		4	V/ns
$t_{slr(o)}$	Output clock slew rate, See Figure 8			1		2	V/ns
$t_{d(Ø)}$§	Dynamic phase offset (this includes jitter), See Figure 4(b)	SSC off	66 MHz	–180		180	ps
			100/133 MHz	–130		130	
			167/200 MHz	–90		90	
		SSC on	66 MHz	–230		230	
			100/133 MHz	–170		170	
			167/200 MHz	–100		100	
$t_{(Ø)}$	Static phase offset, See Figure 4(a)	66/100/133/167 MHz		–100		100	ps
		200 MHz		–150		50	
$tsk_{(o)}$¶	Output skew, See Figure 5					75	ps
tr, tf	Output rise and fall times (20% – 80%)	Load: 120 Ω/14 pF		650		900	ps

† All typical values are at a respective nominal V_{DDQ}.
‡ Refers to transition of noninverting output.
§ This parameter is assured by design but can not be 100% production tested.
¶ All differential output pins are terminated with 120 Ω/14 pF.

PARAMETER MEASUREMENT INFORMATION

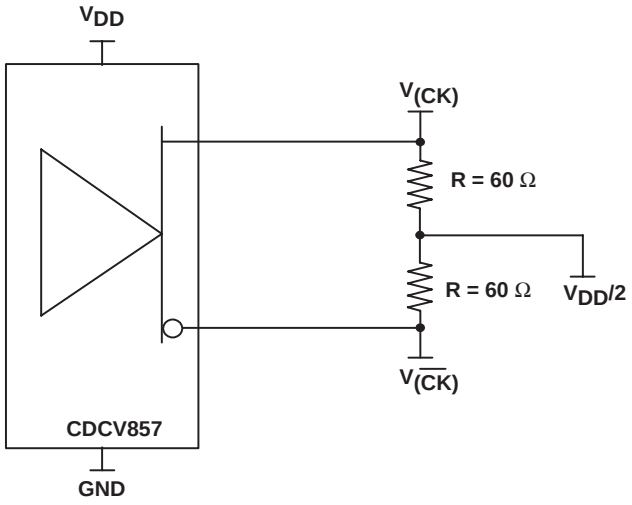
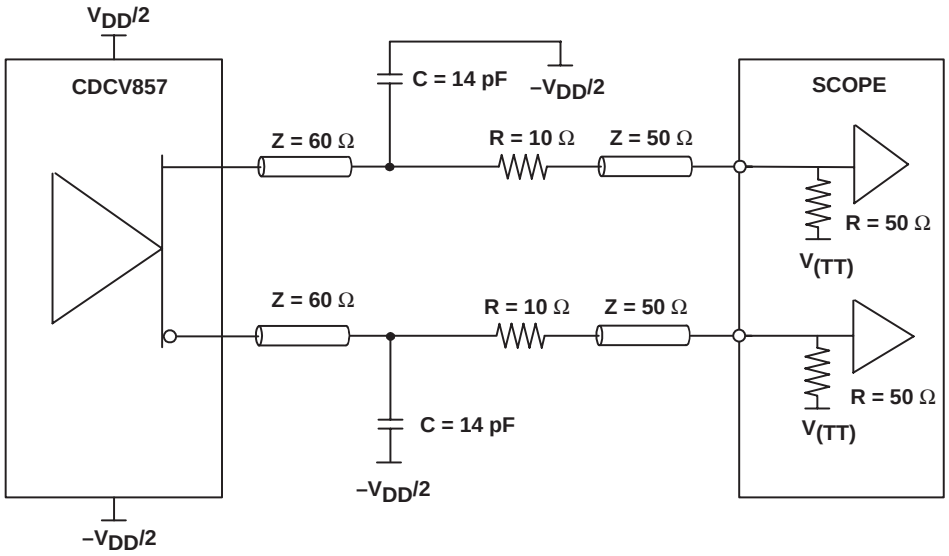
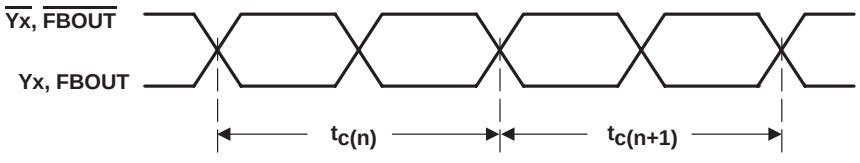


Figure 1. IBIS Model Output Load (used for slew rate measurement)



NOTE: $V_{(TT)}$= GND

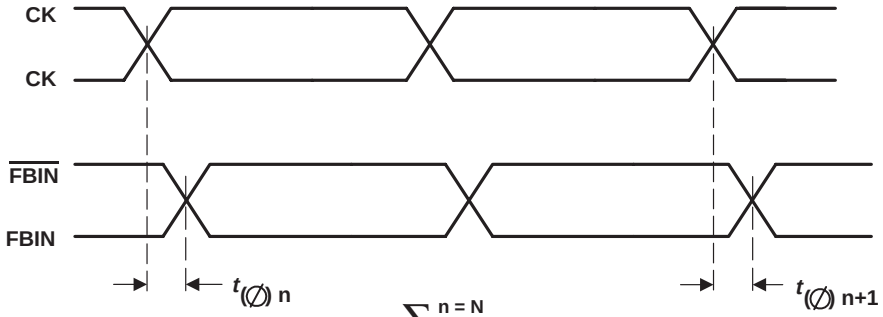
Figure 2. Output Load Test Circuit



$$t_{jit(cc)} = t_{c(n)} - t_{c(n+1)}$$

Figure 3. Cycle-to-Cycle Jitter

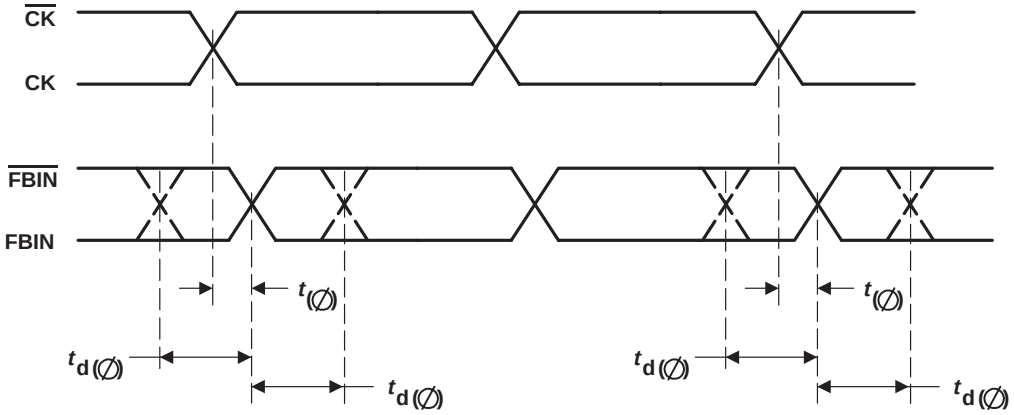
PARAMETER MEASUREMENT INFORMATION



$$t_{(\varnothing)} = \frac{\sum_{1}^{n=N} t_{(\varnothing)\,n}}{N}$$

(N is a large number of samples)

(a) Static Phase Offset



(b) Dynamic Phase Offset

Figure 4. Phase Offset

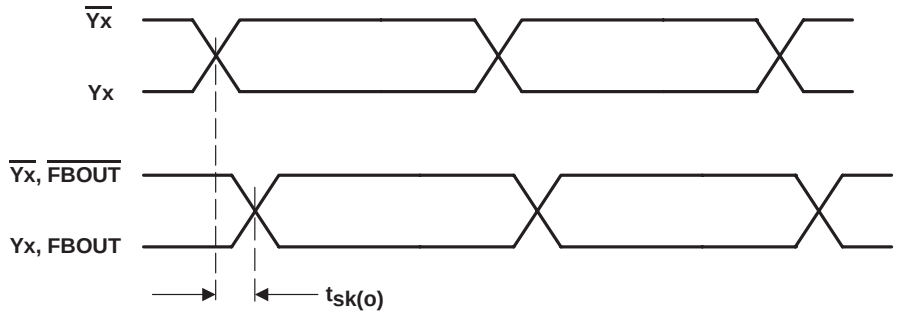
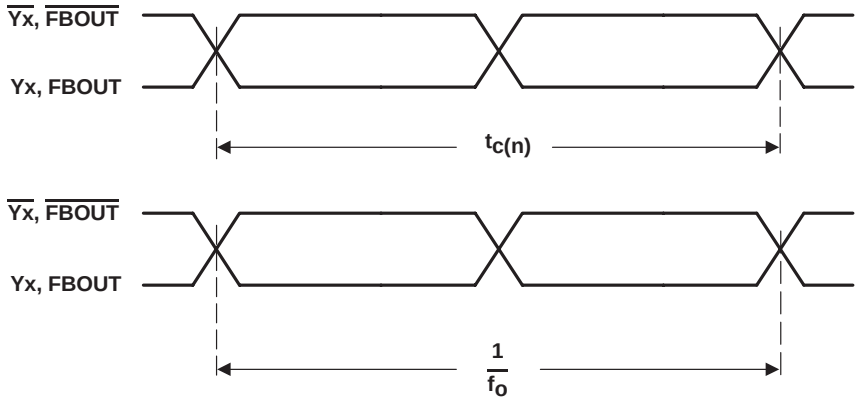


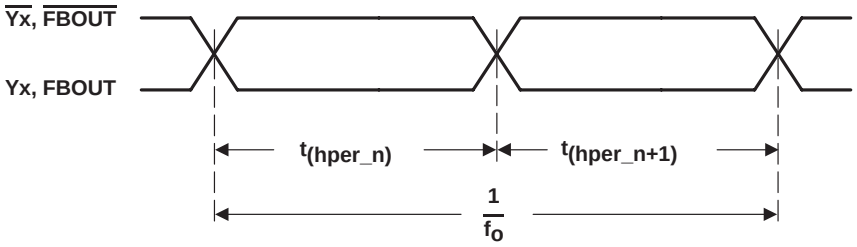
Figure 5. Output Skew

PARAMETER MEASUREMENT INFORMATION



$$t_{jit(per)} = t_{cn} - \frac{1}{f_o}$$

Figure 6. Period Jitter



$$t_{jit(hper)} = t_{(hper\_n)} - \frac{1}{2xf_o}$$

Figure 7. Half-Period Jitter

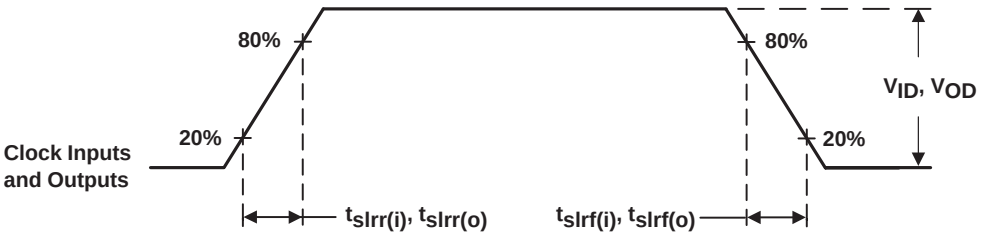
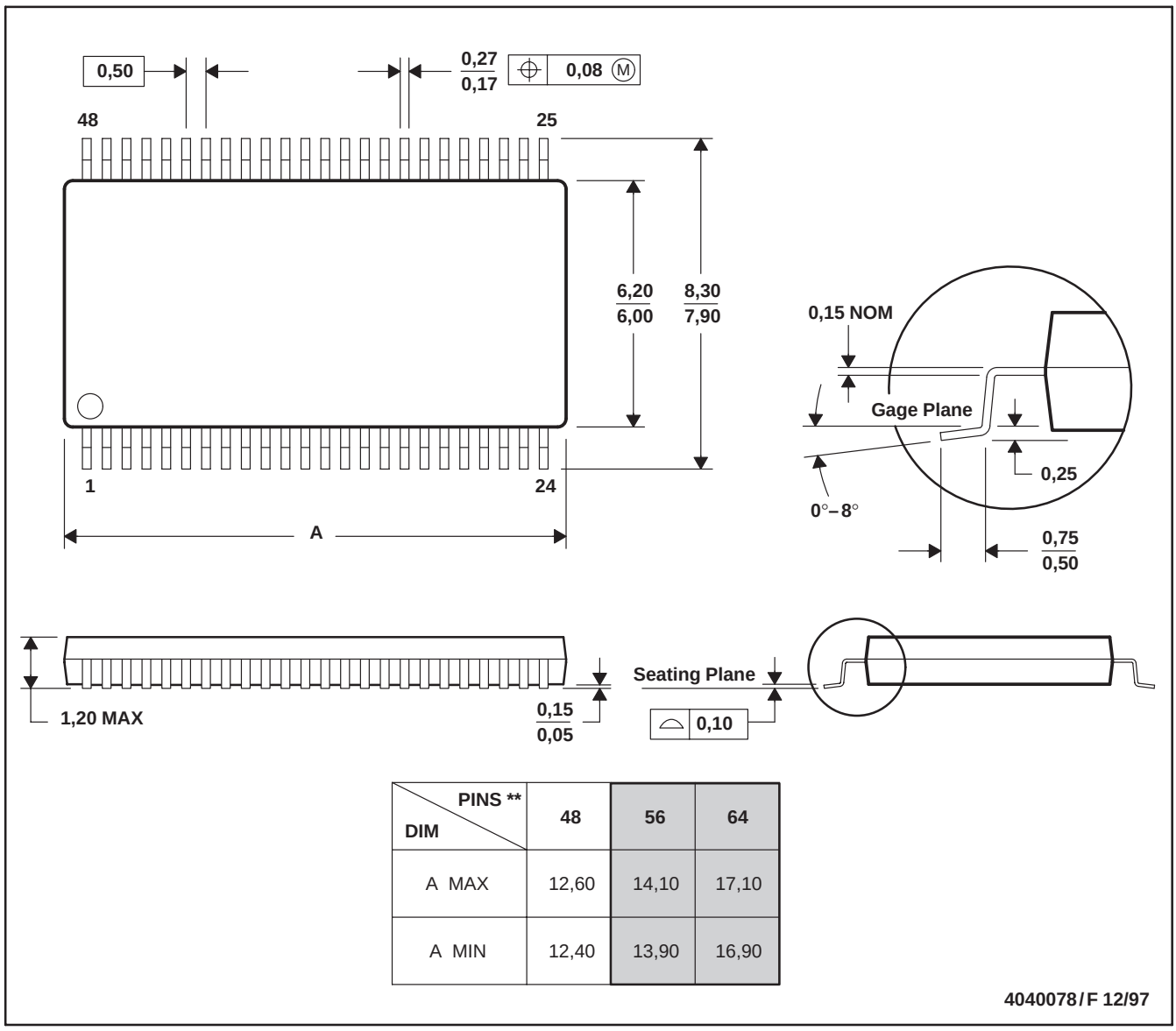


Figure 8. Input and Output Slew Rates

MECHANICAL DATA

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGE OPTION ADDENDUM

4-Mar-2005

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CDCV857DGG	ACTIVE	TSSOP	DGG	48	40	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CDCV857DGGR	ACTIVE	TSSOP	DGG	48	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM
CDCV857DGGRG4	PREVIEW	TSSOP	DGG	48	2000	None	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265