TEXAS INSTRUMENTS

CDCF5801

Evaluation Module

User's Guide

2004

High Performance Analog/CDC

SCAU010

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It is important to operate this EVM within the input voltage range of 3 V and 6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 45°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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CDCF5801 EVM

ABSTRACT

This user's guide explains how to use the EVM board for the CDCF5801 clock driver and to provide the guidelines for building a system. Please contact your local marketing or sales representative to request a CDCF5801 EVM.

Contents

List of Figures

List of Tables

1 Getting Started

The EVM has self-explanatory labeling. All words in bold and in italics in this document are the actual labeling on the EVM. Clock inputs, outputs, and phase aligner inputs have been optimized to maintain 50-Ω transmission line characteristics impedance. The EVM can be used in many ways to provide single-ended or differential clocks for the receivers.

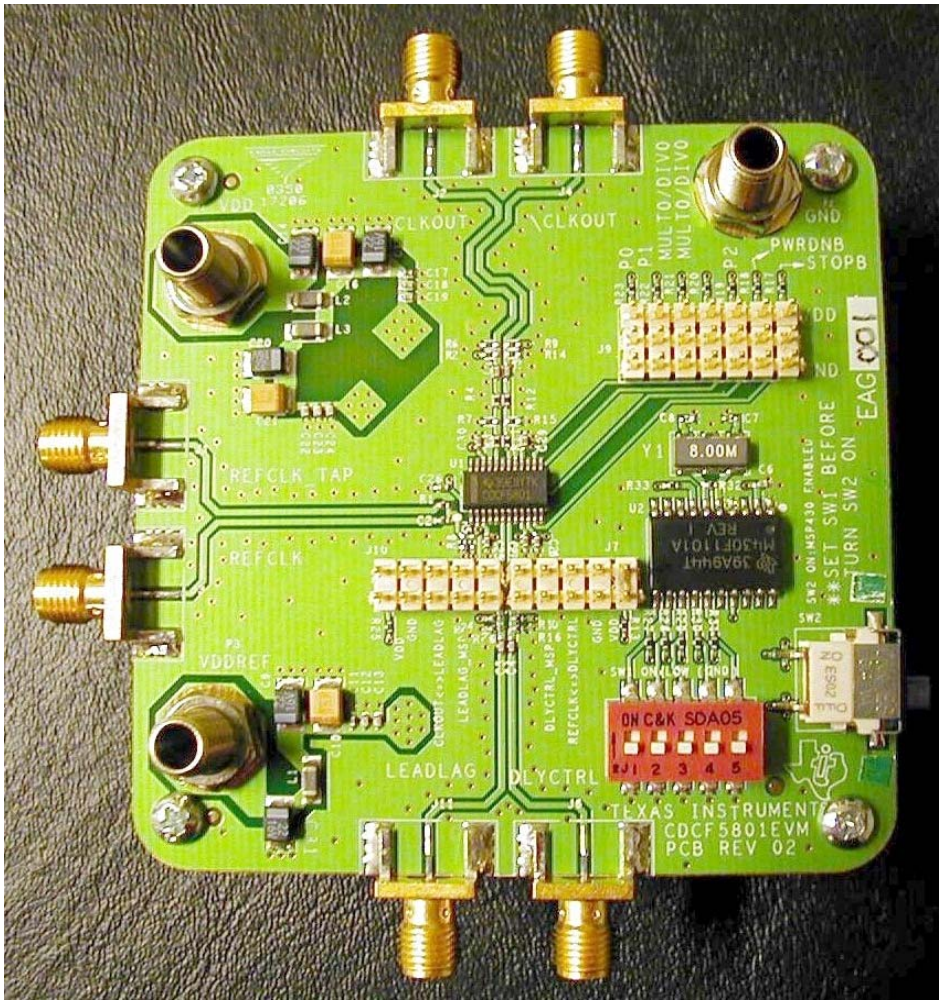

Figure 1. Board View and Connector Location

1.1 Power Supply Connection

Connect the power supply source to the banana plug labeled ***VDD*** and connect the ground of the power supply source to the ***GND*** (banana jack). There are plenty of decoupling capacitors and ferrite beads to isolate the device power pin of the PLL (VDDP) from the rest of the power pins.

For normal operation, connect a 3.3-V power supply to the **VDDREF** power pin. If a lower reference voltage (VDDREF/2) is required for the input clock, connect **VDDREF** to any value between 1.2 V and VDD.

1.2 Enabling the CDCF5801

Connect the header pins labeled ***STOPB*** and ***PWRDNB*** to the VDD side of the **J9** to enable the output buffers and the device.

1.3 Selecting the Proper Mode Through Jumper on the *J9* (3X7) Header Pins

This device has a few different modes of operation. Use jumpers to connect ***P0*** header pin to GND and the ***P1***, ***P2***, ***MULT0/DIV0***, and ***MULT1/DIV*** header pins to VDD or GND for the desired mode. The VDD side is connected to the main power supply through 10-kΩ resistors (***R17***, ***R18***, ***R19***, ***R20***, ***R21***, ***R22***, and ***R23***).

The main purpose of using the resistor is to limit the current into the pins.

Table 1. Mode Selection

Input-to-Output Ratio	Input Frequency (MHz)		Output Frequency (MHz)		Pre-Divider		Post Divider			Note
					MULT0	MULT1	P0	P1	P2	
8	12.5	35	100	280	1	0	0	1	1	Normal Operation
4	12.5	39	50	156	1	0		1	0	
	25	70	100	280	1	1		1	1	
2	12.5	39	25	78	1	0		0	1	
	25	78	50	156	1	1		1	0	
	50	140	100	280	0	0		1	1	
1	25	78	25	78	1	1		0	1	
	50	156	50	156	0	0		1	0	
	100	240	100	240	0	1		1	1	
CLKOUT high impedance					x	X	1	0	0	Special Mode of Operation
CLKOUTB high impedance										
CLKOUT = high					x	X		0	1	
CLKOUTB = high										
CLKOUT = P2					x	x		1	x	
CLKOUT = $\overline{P2}$										

1.4 SMAs Labeled *CLKOUT and $\overline{CLKOUT}$* (Output Pins)

The output pair is not true differential, but complementary. So, the outputs can be configured as any differential signal (signal swing and common-mode voltage) or single ended (out of 180 degree phase shift).

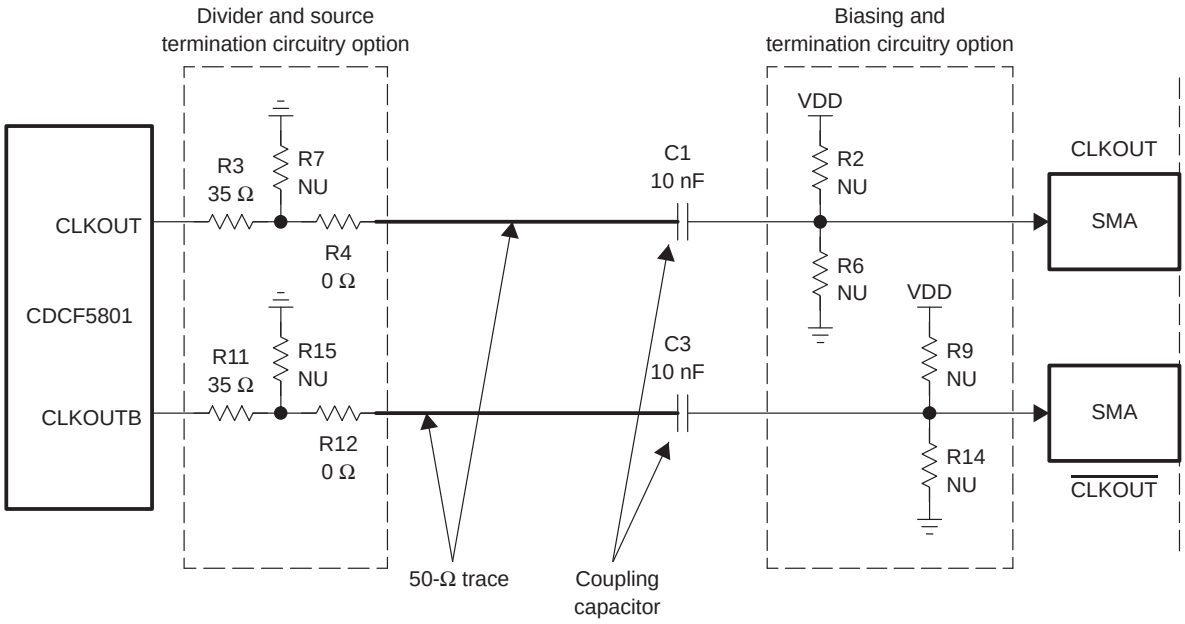

Figure 2. Output Configuration and Options

1.4.1 Output Divider and Termination Circuitry

R3, R7, R4, R11, R15, and R12 can be used to reduce the signal swing. R3 and R11 can be used as source termination for a single-ended signal (35 Ω).

1.4.2 Coupling Capacitors

C1 and C3: The purpose of having the coupling capacitors is to block the dc current and only pass the swing so that the CDCF5801 could be used to drive many different differential signaling levels such as HSTL, LVPECL, and LVDS, etc. This is recommended for driving the differential receiver input stage, assuming that the system user takes proper care to correctly bias the receiver input for the required switching level. These capacitors add no more than 1-ps to 3-ps peak-to-peak jitter.

To drive any LVTTL/LVCMOS device with CDCF5801, if dc termination is required or preferred, these capacitors need to be removed and make it short to maintain the LVTTL level.

1.4.3 Biasing and Termination Circuitry

After the coupling capacitor, proper biasing must be necessary to meet the receiver's common-mode voltage requirement. Using pullup resistors (***R2*** and ***R9***) and pulldown resistors (***R6*** and ***R14***), proper biasing can be set and besides biasing, these resistors can terminate the trace properly.

1.5 SMAs Labeled *REFCLK* and *REFCLK_TAP* (Input Pins)

The ***REFCLK*** SMA connector receives the clock signal, which can come from a number of different sources: signal generator, pulse generator, a system clock from another board, or an oscillator. The ***REFCLK_TAP*** SMA provides the user a way to see with an oscilloscope the source clock coming into the EVM. If not used, the ***REFCLK_TAP*** SMA must be terminated with a 50 Ω resistor (***R8***) for a clock generator.

If the input clock is already terminated by the system/driver clock, then ***REFCLK_TAP*** needs to be left open. ***C2*** can be used as a coupling capacitor (currently shorted with 0-Ω resistor on EVM).

After coupling the capacitor, if the signal needs to be biased, a pullup resistor (***R5***) and a pulldown resistor (***R8***) can be used.

R1 along with the scope's 50 Ω can be used as a pulldown and R5 can be used as pullup, if biasing as well as REFCLK_TAP is required.

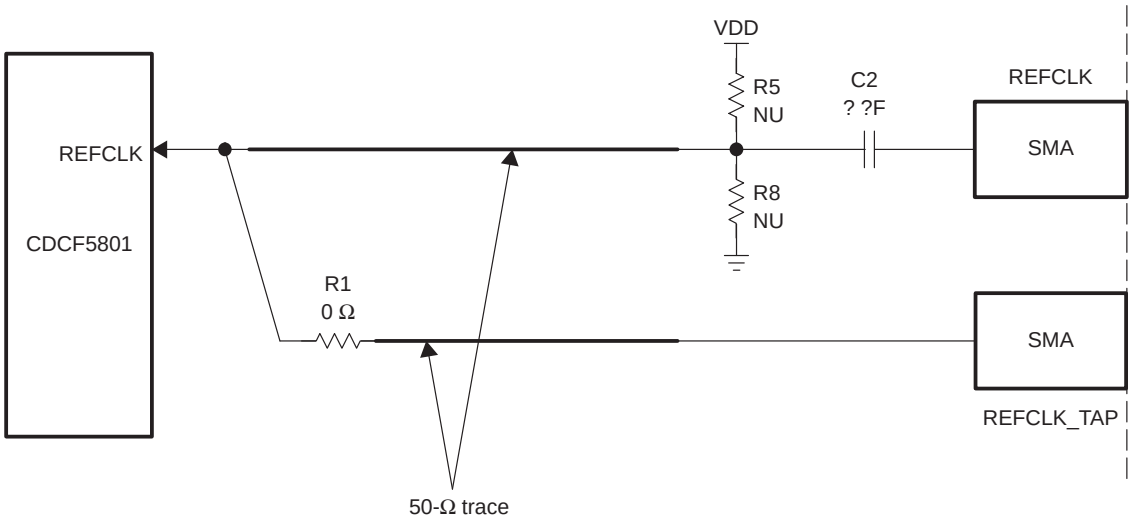

Figure 3. Input Configuration and Options

1.6 SMA's Labeled *DLYCTRL* and *LEADLAG* (Input Pins)

These SMAs are used for the programmable delay and phase aligning features of the CDCF5801. Figure 4 represents the components starting from the SMA to the actual pin on the device (pin 6 and 7).

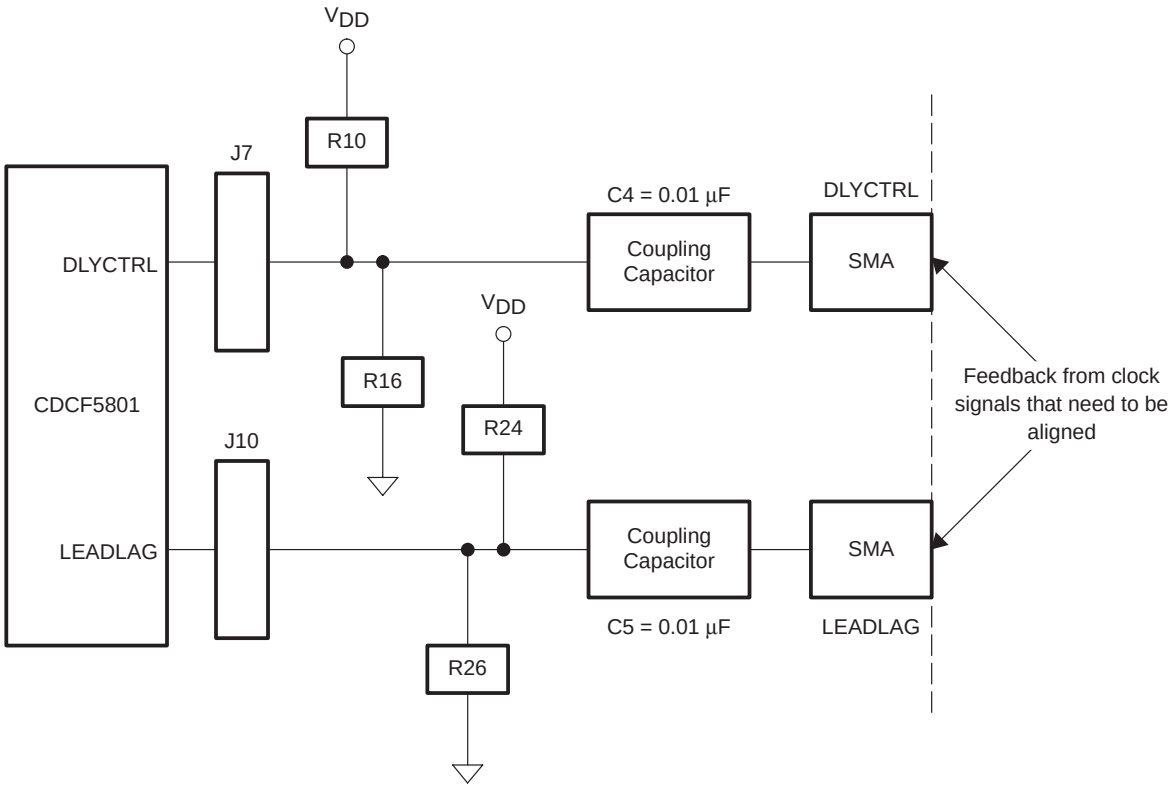

Figure 4. Setting *LEADLAG* and *DLYCTRL* Pins

R10, R16, R24, and R26 are used for two reasons, one for termination and second for dc biasing the respective pins at half the VCC. In the EVM, the four resistors are 100 Ω each and are used for biasing and termination.

C4 and C5 are used for dc blocking.

For the phase aligner and programmable functionality, the above configuration is recommended if termination and biasing are necessary.

J7 and J10 are the switches for selecting signal for LEADLAG and DLYCTRL pins.

1.7 Selecting Signals for *DLYCTRL* and *LEADLAG*

The EVM offers the options to receive the signals for the ***DLYCTRL*** and ***LEADLAG*** pins either from the input/output clock, ***DLYCTRL*** and ***LEADLAG*** labeled SMA or MSP430. ***DLYCTR***L and ***LEADLAG*** can also be connected to GND or VDD through J7 and J10 switches. Place the jumper according to the requirement.

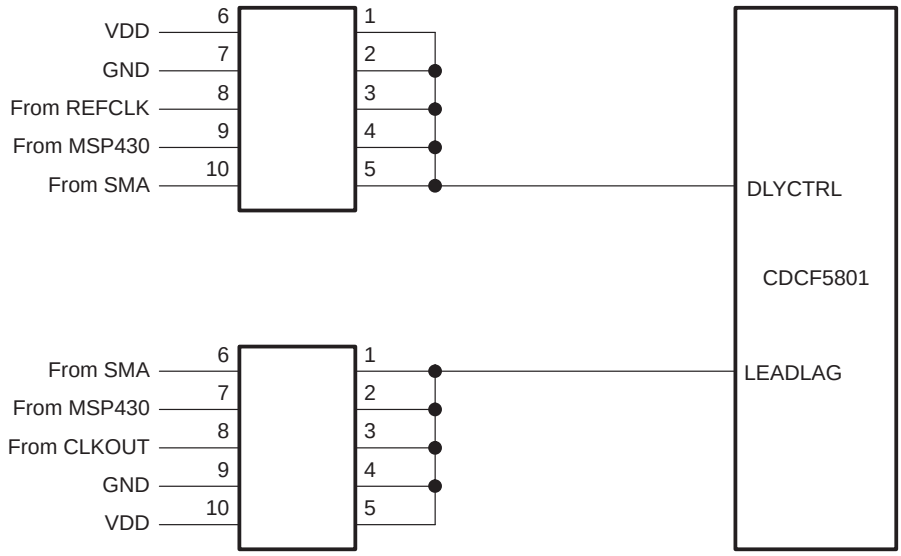

Figure 5. Selecting Signals For *DLYCTRL* and *LEADLAG*

1.8 Programming the CDCF5801 Using MSP430

The MSP430 is a simple u-controller, which generates clock pulses for the ***DLYCTRL*** pin and high or low for the ***LEADLAG*** pin.

The MSP430 generates either a 384-Hz or a 4-MHz clock using an external 8-MHz (***Y1***) crystal. Before sending the clock signal to the CDCF5801 (turning on SW2), short the path of ***J7*** and ***J10*** using jumpers.

The programming of the MSP430 is done by setting ***SW1***; when the switch is on, the pin is connected to ground.

NOTE: ON/OFF referred to in the following tables are related to SW1.

Dip Switch SW1 Pin	Function	Pins Affected (CDCF5801)
5	OFF = continuous; ON = discrete	***DLYCTRL***
4	OFF = 4 MHz; ON = 384 Hz	***DLYCTRL***
3	OFF = Low; ON = High	***LEADLAG***

Dip Switch SW1 Pin	2	1	Number of Clocks Generated
Function	OFF	OFF	3168
	ON	OFF	792
	OFF	ON	396
	ON	ON	10

NOTE: Turn off SW2 before changing SW1 setting.