Integrated Circuit Systems, Inc.

ICS9DB202
PCI Express™ Jitter Attenuator

General Description

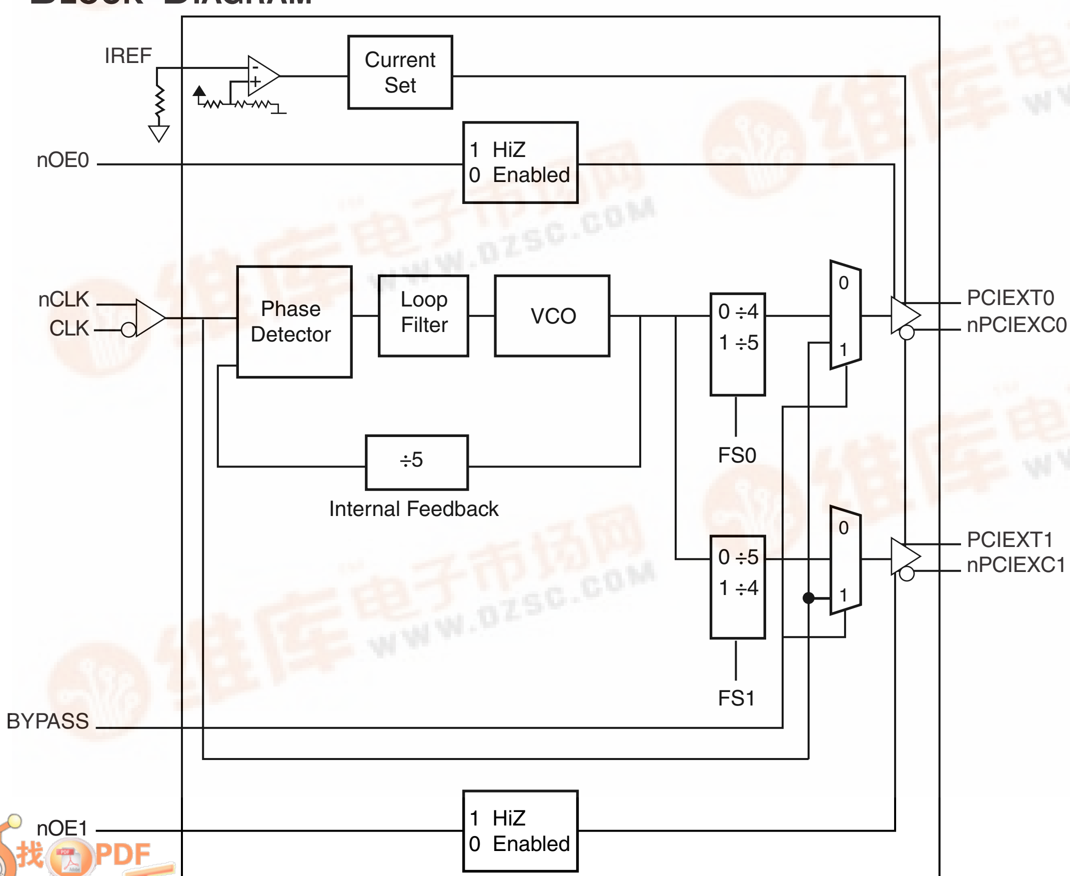
The ICS9DB202 is a high perfromance 1-to-2 Differential-to-HCSL Jitter Attenuator designed for use in PCI Express™ systems. In some PCI Express™ systems, such as those found in desktop PCs, the PCI Express™ clocks are generated from a low bandwidth, high phase noise PLL frequency synthesizer. In these systems, a jitter-attenuating device may be necessary in order to reduce high frequency random and deterministic jitter components from the PLL synthesizer and from the system board. The ICS9DB202 has two PLL bandwidth modes. In low bandwidth mode, the PLL loop bandwidth is 500kHz. This setting offers the best jitter attenuation and is still high enough to pass a triangular input spread spectrum profile. In high bandwidth mode, the PLL bandwidth is at 1MHz and allows the PLL to pass more spread spectrum modulation.

For serdes which have x10 reference multipliers instead of x12.5 multipliers, each of the two PCI Express™ outputs (PCIEX0:1) can be set for 125MHz instead of 100MHz by configuring the appropriate frequency select pins (FS0:1).

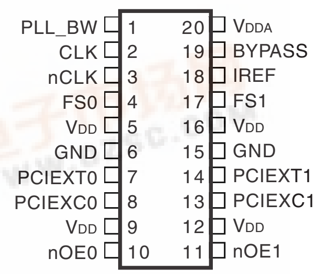
Features

- Two 0.7V current mode differential HCSL output pairs
- 1 differential clock input
- CLK and nCLK supports the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 140MHz
- Output skew: 110ps (maximum)
- Cycle-to-cycle jitter: 110ps (maximum)
- RMS phase jitter @ 100MHz, (1.5MHz - 22MHz): 2.42ps (typical)
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Lead-Free package available
- Industrial temperature information available upon request

Block Diagram



Pin Assignment



ICS9DB202
20-Lead TSSOP
6.50mm x 4.40mm x 0.92 package body
G Package
Top View

ICS9DB202
20-Lead, 209-MIL SSOP
5.30mm x 7.20mm x 1.75mm body package
F Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	PLL_BW	Input	Pullup	Selects PLL Bandwidth input. LVCMOS/LVTTL interface levels.
2	CLK	Input	Pulldown	Non-inverting differential clock input.
3	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. V_{DD}/2 default when left floating.
4	FS0	Input	Pullup	Frequency select pin. LVCMOS/LVTTL interface levels.
5, 9, 12, 16	V_{DD}	Power		Core supply pins.
6, 15	GND	Power		Power supply ground.
7, 8	PCIEXT0, PCIEXC0	Output		Differential output pairs. HCSL interface levels.
10, 11	nOE0, nOE1	Input	Pulldown	Output enable. When HIGH, forces outputs to HiZ state. When LOW, enables outputs. LVCMOS/LVTTL interface levels.
13, 14	PCIEXC1, PCIEXT1	Output		Differential output pairs. HCSL interface levels.
17	FS1	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
18	IREF	Input		A fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode PCIEX clock outputs.
19	BYPASS	Power	Pulldown	BYPASS pin. When HIGH. bypass mode, when LOW, PLL mode. LVCMOS/LVTTL interface levels.
20	V_{DDA}	Power		Analog supply pin. Requires 24Ω series resistor.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

TABLE 3A. RATIO OF OUTPUT FREQUENCY TO INPUT FREQUENCY FUNCTION TABLE, FS0

Inputs	Outputs
FS0	PCIEX0
0	5/4
1	1

TABLE 3B. RATIO OF OUTPUT FREQUENCY TO INPUT FREQUENCY FUNCTION TABLE, FS1

Inputs	Outputs
FS1	PCIEX1
0	1
1	5/4

TABLE 3C. BYPASS TABLE

Inputs	Mode
BYPASS	
0	PLL Mode
1	Bypass Mode (output = inputs)

TABLE 3D. OUTPUT ENABLE FUNCTION TABLE, nOE0

Inputs	Outputs
nOE0	PCIEX0
0	Enabled
1	HiZ

TABLE 3E. OUTPUT ENABLE FUNCTION TABLE, nOE1

Inputs	Outputs
nOE1	PCIEX1
0	Enabled
1	HiZ

TABLE 3F. PLL BANDWIDTH TABLE

Inputs	Bandwidth
PLL_BW	
0	500kHz
1	1MHz

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5 V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	
20 Lead TSSOP	73.2°C/W (0 lfpm)
20 Lead SSOP	80.8°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA}$ = 3.3V±5%, TA = 0°C TO 70°C, RREF = 475Ω

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				112	mA
I_{DDA}	Analog Supply Current				22	mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	mV
V_{IL}	Input Low Voltage			-0.3		0.8	mV
I_{IH}	Input High Current	BYPASS, nOE0, nOE1, FS1	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		FS0, PLL_BW				5	
I_{IL}	Input Low Current	BYPASS, nOE0, nOE1, FS1	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		FS0, PLL_BW		-150			

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{DD} = V_{DDA}$ = 3.3V±5%, TA = 0°C TO 70°C, RREF = 475Ω

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
I_{IL}	Input Low Current	CLK, nCLK	V_{DD} = 3.465V, V_{IN} = 0V			150	µA
V_{PP}	Peak-to-Peak Input Voltage			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			GND + 0.5		V_{DD} - 0.85	V

NOTE 1: Common mode voltage is defined as V_{IH}.
NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is V_{DD} + 0.3V.

TABLE 4D. HCSL DC CHARACTERISTICS, $V_{DD} = V_{DDA}$ = 3.3V±5%, TA = 0°C TO 70°C, RREF = 475Ω

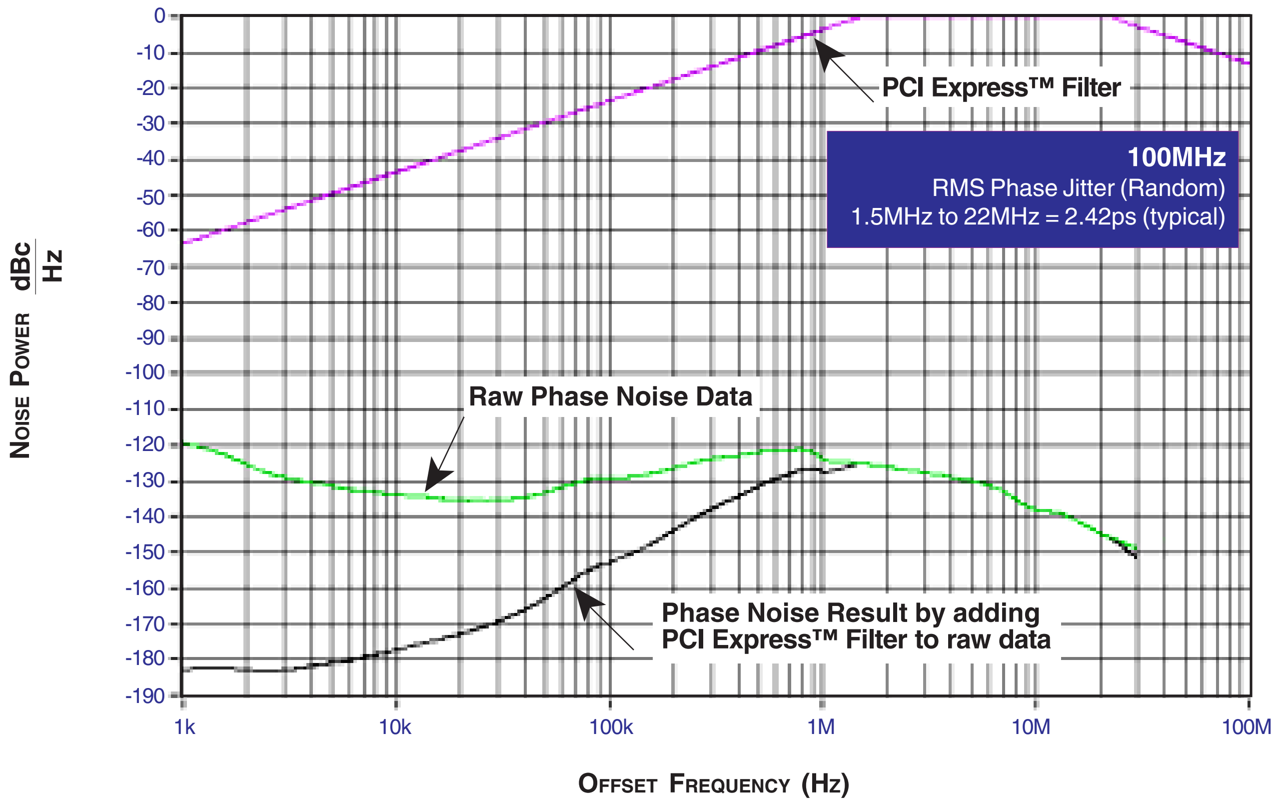
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{OH}	Output Current		12	14	16	mA
V_{OH}	Output High Voltage		680			V
V_{OL}	Output Low Voltage				65	V
I_{OZ}	High Impedance Leakage Current		-10		10	µA
V_{OX}	Output Crossover Voltage		250		550	mV

TABLE 5. AC CHARACTERISTICS, $V_{DD} = V_{DDA}$ = 3.3V±5%, TA = 0°C TO 70°C, RREF = 475Ω

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				140	MHz
*t*sk(o)	Output Skew; NOTE 1, 2			50	110	ps
*t*jit(cc)	Cycle-to-Cycle Jitter	Outputs @ Different Frequencies			110	ps
		Outputs @ Same Frequencies			50	ps
*t*jit(Ø)	RMS Phase Jitter (Random); NOTE 3	Integration Range: 1.5MHz - 22MHz		2.42		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	300		1100	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the output differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Please refer to the Phase Noise Plot following this section.

TYPICAL PHASE NOISE AT 100MHZ

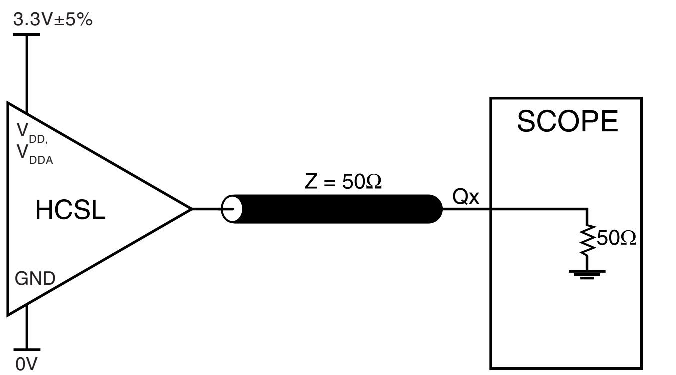


The illustrated phase noise plot was taken using a low phase noise signal generator, the noise floor of the signal generator is less than that of the device under test.

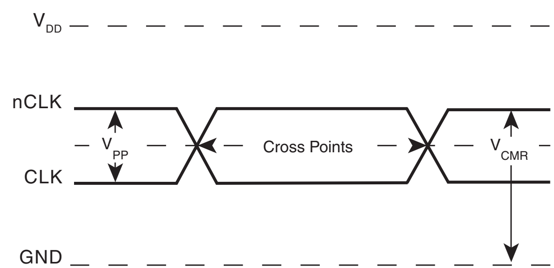
Using this configuration allows one to see the true spectral purity or phase noise performance of the PLL in the device under test.

Due to the tracking ability of a PLL, it will track the input signal up to its loop bandwidth. Therefore, if the input phase noise is greater than that of the PLL, it will increase the output phase noise performance of the device. It is recommended that the phase noise performance of the input is verified in order to achieve the above phase noise performance.

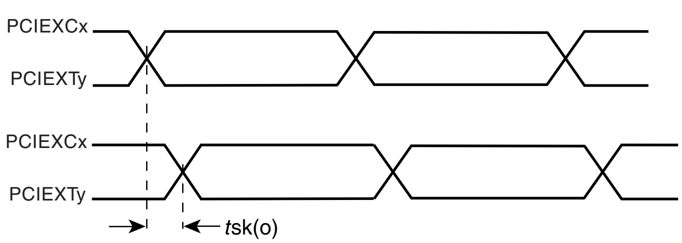
PARAMETER MEASUREMENT INFORMATION



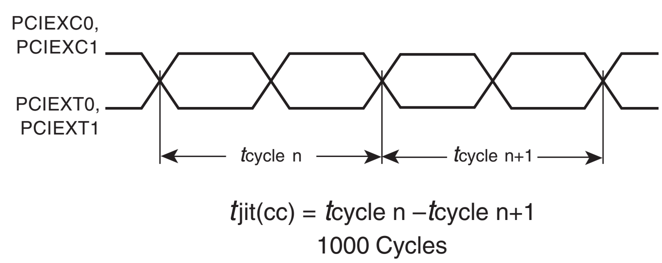
3.3V HCSL OUTPUT LOAD AC TEST CIRCUIT



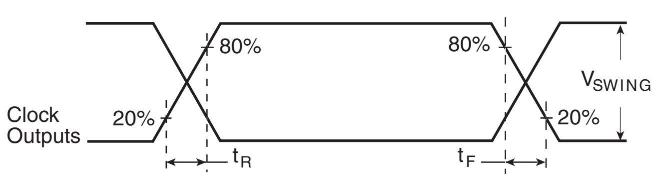
DIFFERENTIAL INPUT LEVEL



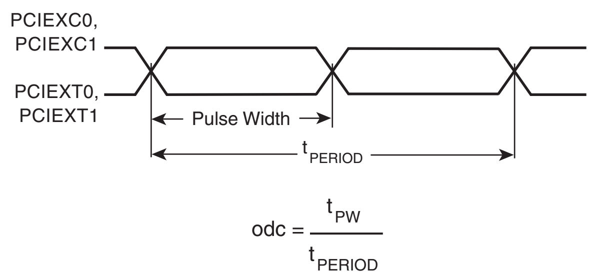
OUTPUT SKEW



CYCLE-TO-CYCLE JITTER



HCSL OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS9DB202 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 24Ω resistor along with a 10µF and a .01µF bypass capacitor should be connected to each V_{DDA} pin.

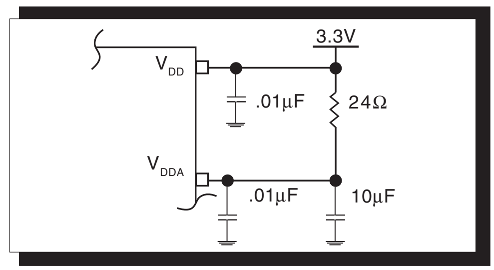


FIGURE 1. POWER SUPPLY FILTERING

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{DD}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{DD} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

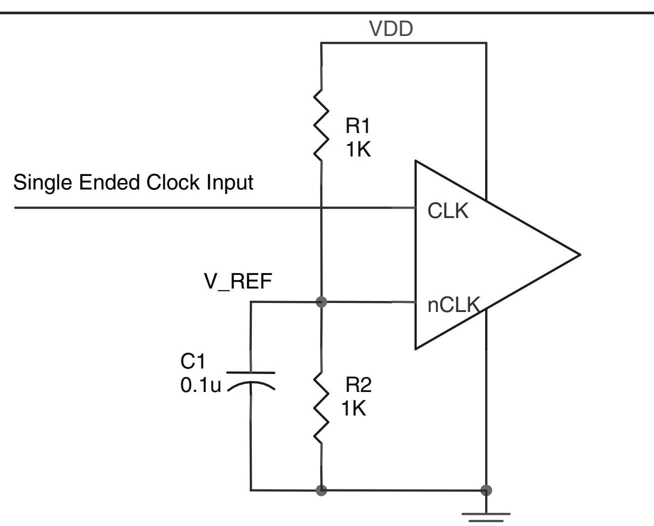


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A,* the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

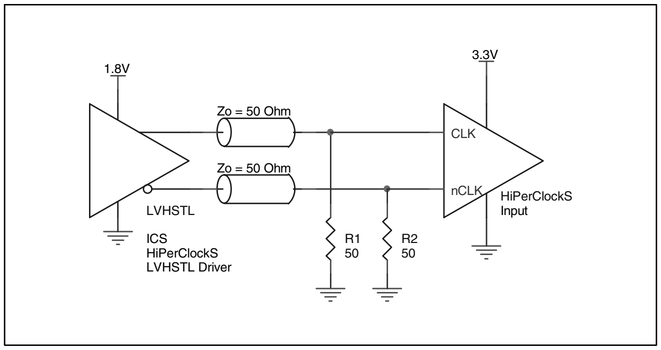


FIGURE 3A. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY ICS HIPERCLOCKS LVHSTL DRIVER

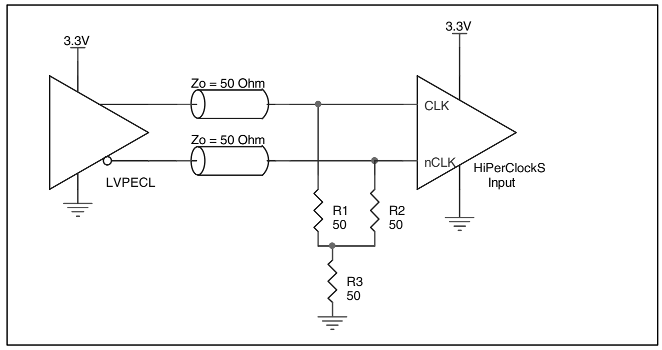


FIGURE 3B. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

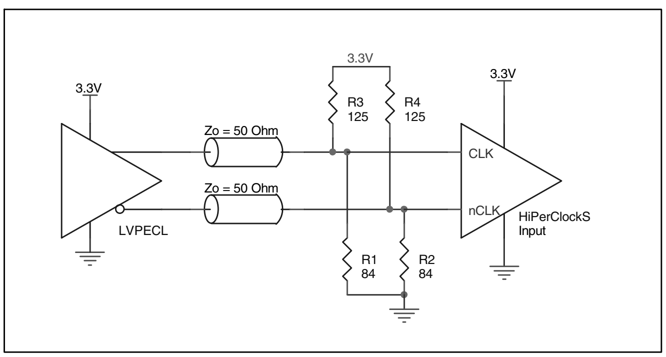


FIGURE 3C. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER

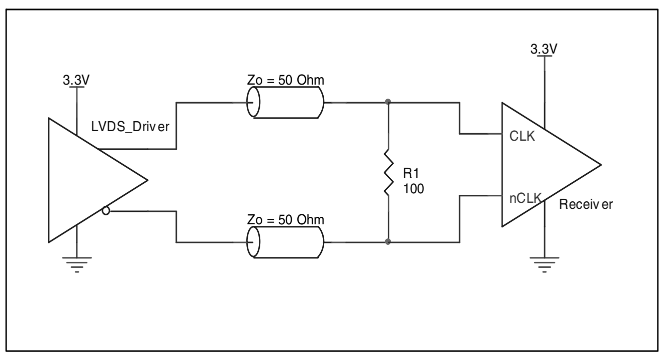


FIGURE 3D. HIPERCLOCKS CLK/NCLK INPUT DRIVEN BY 3.3V LVDS DRIVER

RELIABILITY INFORMATION

TABLE 6A. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP PACKAGE

θ_{JA} by Velocity (Linear Feet per Minute)

	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98°C/W	88°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TABLE 6B. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD SSOP PACKAGE

θ_{JA} by Velocity (Linear Feet per Minute)

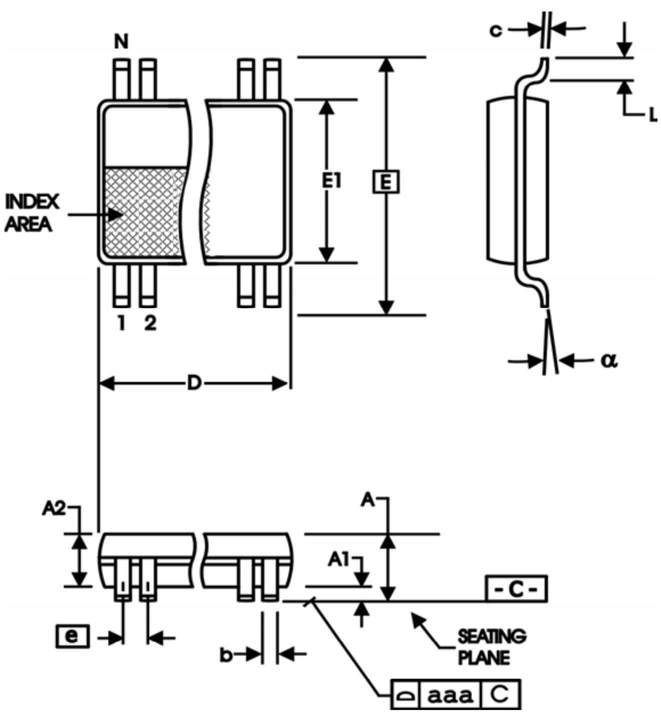
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	80.8°C/W	73.2°C/W	69.2°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS9DB202 is: 2471

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP



PACKAGE OUTLINE - F SUFFIX FOR 20 LEAD SSOP

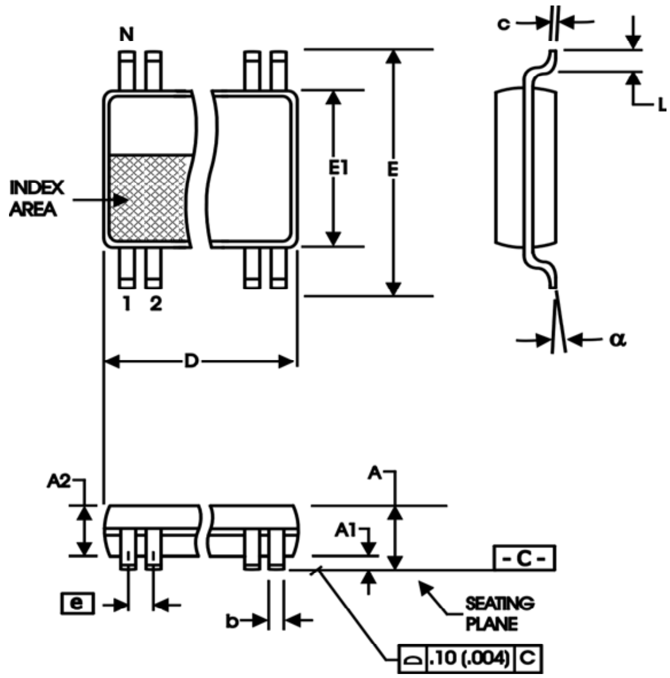


TABLE 6A. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 6B. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	2.0
A1	0.05	--
A2	1.65	1.85
b	0.22	0.38
c	0.09	0.25
D	6.90	7.50
E	7.40	8.20
E1	5.0	5.60
e	0.65 BASIC	
L	0.55	0.95
α	0°	8°

Reference Document: JEDEC Publication 95, MO-150

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS9DB202CG	ICS9DB202CG	20 Lead TSSOP	72 per Tube	0°C to 70°C
ICS9DB202CGT	ICS9DB202CG	20 Lead TSSOP on Tape and Reel	2500	0°C to 70°C
ICS9DB202CGLF	ICS9DB202CGL	20 Lead "Lead-Free" TSSOP	72 per Tube	0°C to 70°C
ICS9DB202CGLFT	ICS9DB202CGL	20 Lead "Lead-Free" TSSOP on Tape and Reel	2500	0°C to 70°C
ICS9DB202CF	ICS9DB202CF	20 Lead SSOP	64 per Tube	0°C to 70°C
ICS9DB202CFT	ICS9DB202CF	20 Lead SSOP on Tape and Reel	1000	0°C to 70°C
ICS9DB202CFLF	ICS9DB202CFLF	20 Lead "Lead-Free" SSOP	64 per Tube	0°C to 70°C
ICS9DB202CFLFT	ICS9DB202CFLF	20 Lead "Lead-Free" SSOP on Tape and Reel	1000	0°C to 70°C