

CT2100-400 MICROPROCESSOR CONTROLLED QUAD SOLID STATE RELAY

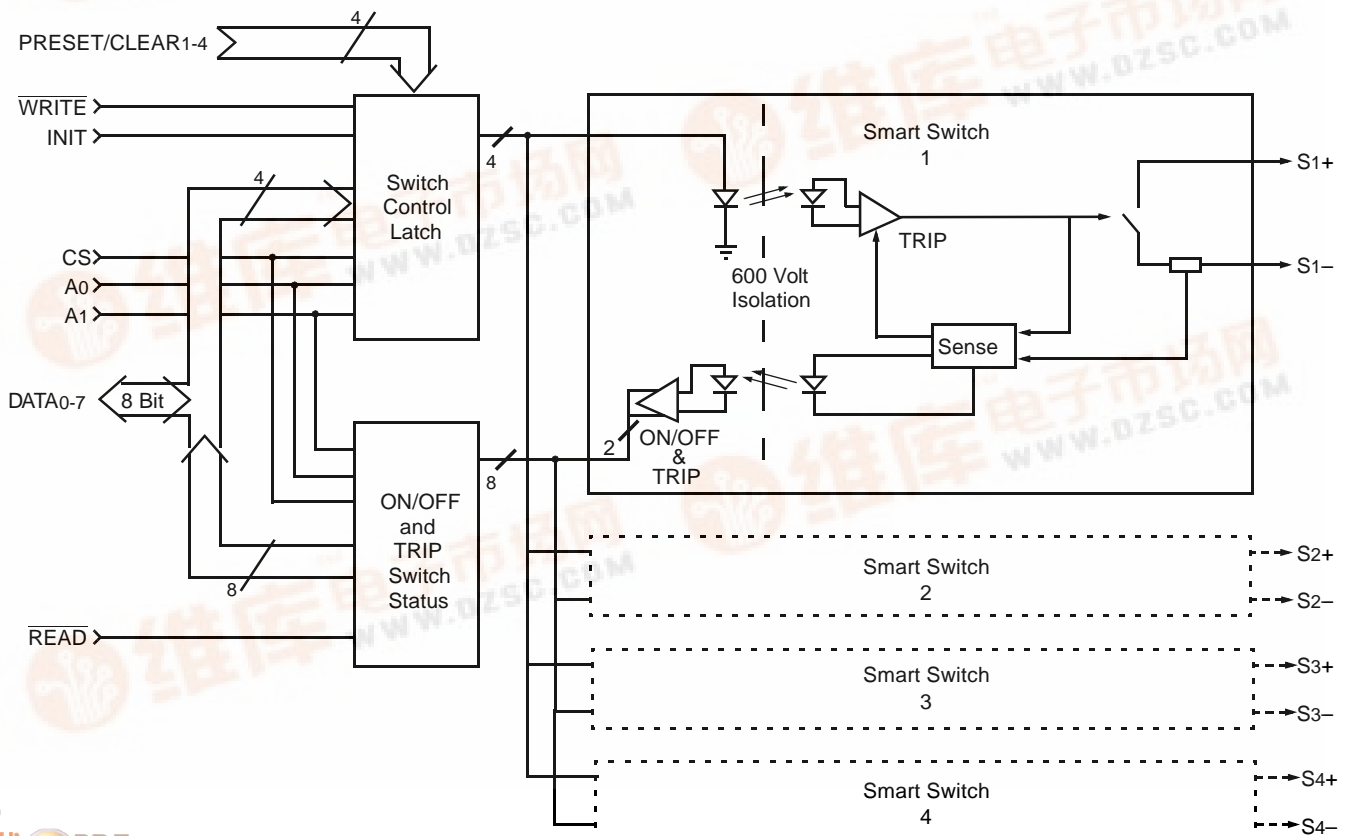
Features

- 4 Independent 1.0 Amp Switches
- 600 Volts Isolation between Switches
- Operates from a 5 Volt Logic and 15 Volt Bias
- D.C. Trip Level 1.3 Amps
- Switches are Designed to withstand Electro-Magnetic Pulse (EMP)
- Functions and Operates from -55°C to +125°C in Military Environments
- Processed and Screened to Mil-STD-883 Specifications

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The CT2100-400 is a microprocessor controlled, quad solid state relay that incorporates fully isolated switch control and built-in test. The hybrid provides 600 Volts isolation between control inputs and switch outputs. Internal control and status registers provide analog switch function which operates via simple I/O commands.

Block Diagram



DESCRIPTION

The CT2100-400 is a quad solid state relay. The device has been designed to provide an interface which operates as a simple computer I/O port. The switches are controlled by a single data word which the processor writes to an internal control latch. In addition to the basic switch function ON/OFF and Trip flags provide the operational status of each of the four switches. These signals are internally contained in an 8 bit status register which is accessible by an I/O read command. The switches may also be controlled asynchronously (without write strobes) by use of separate initialization pins. These may also be used for Power-Up control in a microprocessor based system.

SWITCH CONTROL

The CT2100-400 has four independent fully isolated switches which may be used as high side or low side drivers. The isolated design allows the user to parallel devices or place them in series as required for the specific application. Control of the switch is via I/O write (Address 0) or asynchronous control lines. The CT2100-400 has an internal switch control latch which is updated via subsystem I/O write as illustrated in Figure 2. Once the I/O write is completed the switch is latched into the OFF or ON state. The switch may also be controlled via individual PRESET and CLEAR lines. These lines asynchronously drive the switch control latch without the need for a write

strobe. The PRESET/CLEAR inputs are enabled by the initialize pin.

SWITCH STATUS

Each switch in the CT2100-400 is monitored for circuit Trip and ON/OFF. This data is contained in a 8 bit status register which is accessible via an I/O read (Address 0) command. The timing for the I/O read is shown in Figure 1. The Trip and ON/OFF flags are provided to the system to assess the operational capability of the switch versus the status of the controlled load. The Trip bit is set high when the switch has conducted between 1.1 to 3 amps of current based on the time to trip curve in Figure 3. The over current DC trip point is typically 1.3 amps.

Table 1 — Absolute Maximum Ratings

Supply Voltage (V_{CC}) — Pin 20	-0.5 to +7.0 Volts DC
Supply Voltage (V_{EE}) — Pin 1	-.5 to +18 Volts DC
Logic Input Voltage — Pins 2-9, 12-19	-0.5 to V_{CC} +.5 Volts DC
Switch Point Voltage — Pins 39-40, 29-32, 21-22	-600 to +600 Volts (200 ns) 80 Volts DC
Storage Temperature Range	-65°C to +150 °C

Table 2 — Recommended Operating Conditions

Supply Voltage (V_{CC}) — Pin 20	+5.0 VDC $\pm 10\%$
Supply Voltage (V_{EE}) — Pin 1	+14.25 to +15.75 VDC
Logic Input Maximum Voltage (High) — Pins 2-9, 12-19	+3.3 V
Logic Input Minimum Voltage (Low) — Pins 2-9, 12-19	+0.8 V
Switch Point Voltage — Pins 39-40, 29-32, 21-22	60 VDC
Operating Temperature Range	-55°C to +125 °C

Timing Waveforms

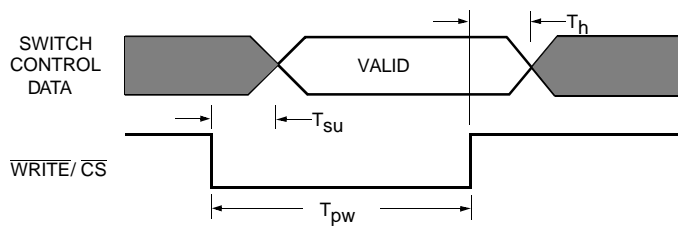


Figure 1

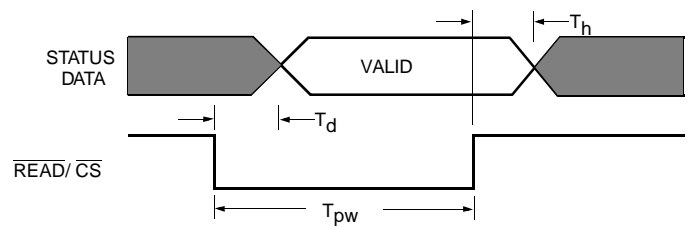


Figure 2

Table 3 — Timing Characteristics

READ Cycle					WRITE Cycle				
Parameter	Sym	Min	Max	Units	Parameter	Sym	Min	Max	Units
Pulse Width	T_{PW}	100	-	nsec	Pulse Width	TPW	100	-	nsec
Data Delay	T_D	-	50	nsec	Set-up Time	T_s	25	-	nsec
Hold Time	T_D	10	-	nsec	Hold Time	T_H	10	-	nsec

Table 4 — Switch Data

Parameter	Sym	Min	Max	Units
DC Continous Rated Current	I_C	-	1	Amps
DC Trip Current (For Time to Trip Refer to Figure 3)	I_{OT}	1.1	1.5	Amps
On Resistance	R_{ON}	-	0.6	Ohms
Output Leakage Current at 80 VDC	I_L	-	40	μA
Switch Turn-on Time	T_{SD}	-	2	msec
Isolation	V_{ISO}	600	-	Volts

Table 5 — Bus Bit Definition

<i>ADDRESS = 0</i>		
BIT	WRITE CYCLE	READ CYCLE
D0	S1 ON/OFF 0 = ON	S1 ON/OFF status (Bit = 0)(When switch on)
D1	Not Used	S1 TRIP status (Bit = 1)(When short circuit protection active))
D2	S2 ON/OFF 0 = ON	S2 ON/OFF Status
D3	Not Used	S2 TRIP Status
D4	S3 ON/OFF 0 = ON	S3 ON/OFF Status
D5	Not Used	S3 TRIP Status
D6	S4 ON/OFF 0 = ON	S4 ON/OFF Status
D7	Not Used	S4 TRIP Status
<i>ADDRESS = 1 (Wrap Around)</i>		
D0 – D7	Bit = 1 or 0	Whatever was written in the write cycle will be read
<i>ADDRESS = 2</i>		
D0	X <u>1</u>	0 = Command On (Signal being sent from the control side to Isolation Driver)
D1	X	Not Used
D2	X	0 = Command On (Signal being sent from the control side to Isolation Driver)
D3	X	Not Used
D4	X	0 = Command On (Signal being sent from the control side to Isolation Driver)
D5	X	Not Used
D6	X	0 = Command On (Signal being sent from the control side to Isolation Driver)
D7	X	Not Used

1 X = Don't care. During a write cycle (Address 2) it shall be considered as if the INIT is enabled.

Table 6 —Built-in Test Status (BIT)

Switch Control (Closed/OPEN)	TRIP Status	ON/OFF Status	Conclusion
1	0	1	Normal (OFF)
0	0	0	Normal (ON)
0	1	1	Switch Tripped off due to excessive load current

Note: All other TRIP and ON/OFF status combinations are indicative of switch, BIT or load failures

Table 7A – Pin Numbers & Functions

CT2100-400			
Pin #	Function	Pin #	Function
1	V _{EE}	21	S4-
2	CS	22	S4+
3	INIT	23	NC
4	DB0	24	NC
5	DB1	25	NC
6	PRESET/CLEAR 1	26	A1
7	PRESET/CLEAR 2	27	A0
8	DB2	28	NC
9	DB3	29	S3-
10	V _{EE} RETURN	30	S3+
11	V _{CC} RETURN	31	S2-
12	DB4	32	S2+
13	DB5	33	NC
14	PRESET/CLEAR 3	34	NC
15	PRESET/CLEAR 4	35	NC
16	DB6	36	NC
17	DB7	37	NC
18	$\overline{\text{WRITE}}$	38	NC
19	$\overline{\text{READ}}$	39	S1-
20	V _{CC}	40	S1+

Table 7B — Model CT2100-400 Dual In Line Package

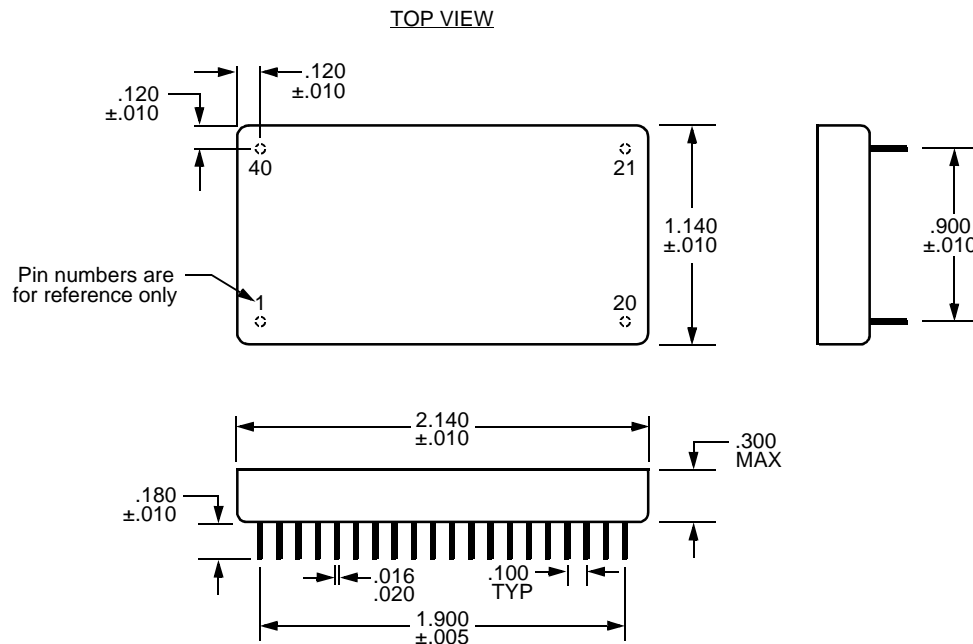
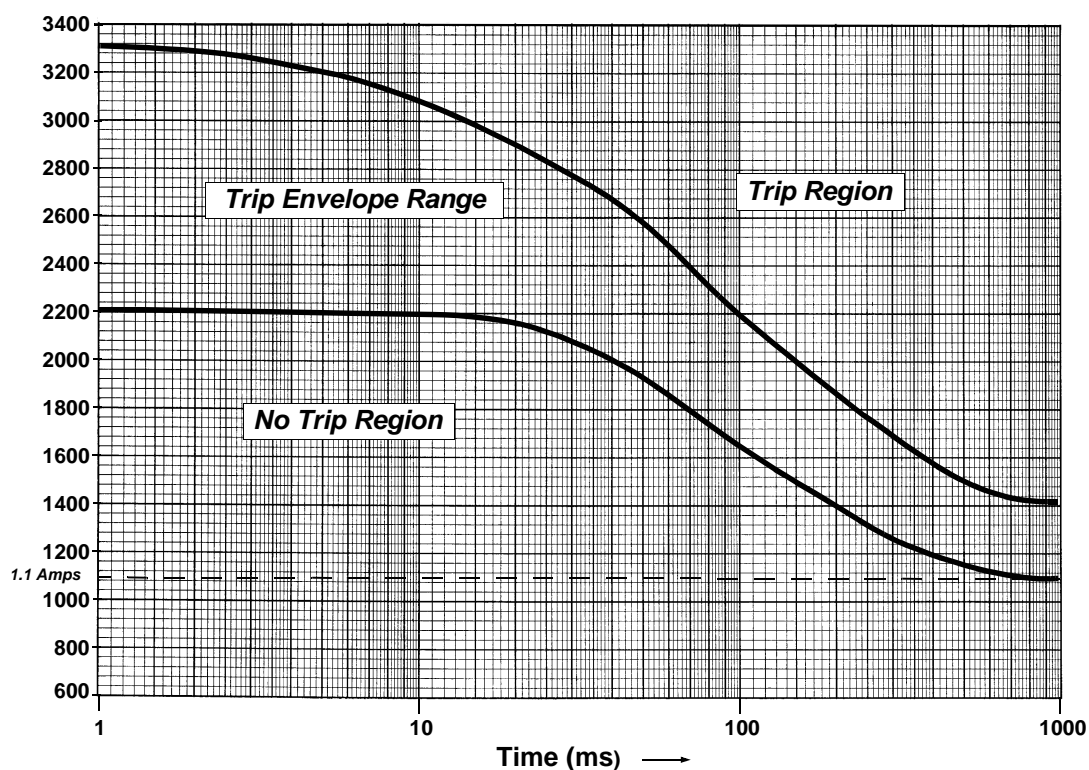




Figure 3 — Nominal Time to Trip Curve



Ordering Information

Model No.
CT2100-400

Specifications subject to change without notice.

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