DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HCU04
Hex inverter

Product specification
File under Integrated Circuits, IC06

September 1993

Philips Semiconductors

PHILIPS

Hex inverter 74HCU04

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HCU04 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A.
The 74HCU04 is a general purpose hex inverter. Each of the six inverters is a single stage

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
t_{PHL}/ t_{PLH}	propagation delay nA to nY	C_L = 15 pF; V_{CC} = 5 V	5	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per inverter	note 1	10	pF

Note

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_O)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

FUNCTION TABLE

INPUT	OUTPUT
nA	**nY**
L	H
H	L

Note

1. H = HIGH voltage level
   L = LOW voltage level

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 3, 5, 9, 11, 13	1A to 6A	data inputs
2, 4, 6, 8, 10, 12	1Y to 6Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

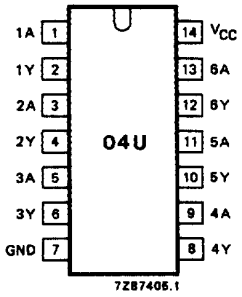


Fig.1 Pin configuration.

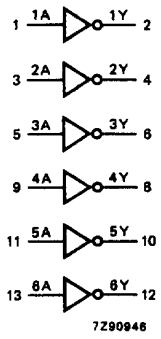


Fig.2 Logic symbol.

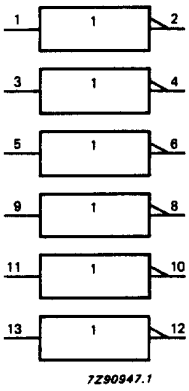


Fig.3 IEC logic symbol.

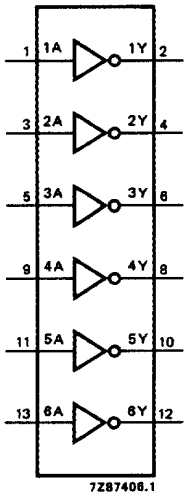


Fig.4 Functional diagram.

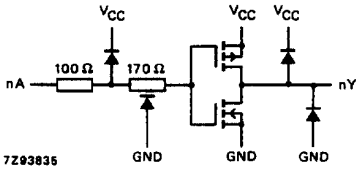


Fig.5 Schematic diagram (one inverter).

DC CHARACTERISTICS FOR 74HCU

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb}(°C)							UNIT	TEST CONDITIONS		
		74HCU										
		+25			-40 to +85		−40 to +125			V_{CC} (V)	V_I	OTHER
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	1.7 3.6 4.8	1.4 2.6 3.4		1.7 3.6 4.8		1.7 3.6 4.8		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage		0.6 1.9 2.6	0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage	1.8 4.0 5.5	2.0 4.5 6.0		1.8 4.0 5.5		1.8 4.0 5.5		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 μA $-I_O$ = 20 μA $-I_O$ = 20 μA
V_{OH}	HIGH level output voltage	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2		V	4.5 6.0	V_{CC} or GND	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage		0 0 0	0.2 0.5 0.5		0.2 0.5 0.5		0.2 0.5 0.5	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 μA I_O = 20 μA I_O = 20 μA
V_{OL}	LOW level output voltage		0.15 0.16	0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{CC} or GND	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	μA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			2.0		20.0		40.0	μA	6.0	V_{CC} or GND	I_O = 0

AC CHARACTERISTICS FOR 74HCU

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCU									
		+25			-40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay nA to nY		19 7 6	70 14 12		90 18 15		105 21 18	ns	2.0 4.5 6.0	Fig.6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

AC WAVEFORMS

(1) V_M = 50%; V_I = GND to V_{CC}.

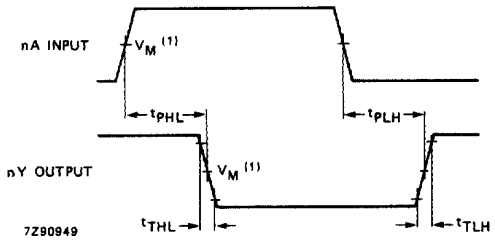


Fig.6 Waveforms showing the data input (nA) to data output (nY) propagation delays and the output transition times.

TYPICAL TRANSFER CHARACTERISTICS

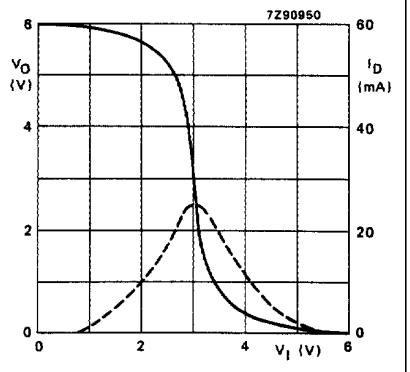


Fig.7 _____ V_O;
_ _ _ _ I_D (drain current);
I_O = 0; V_{CC} = 6.0 V.

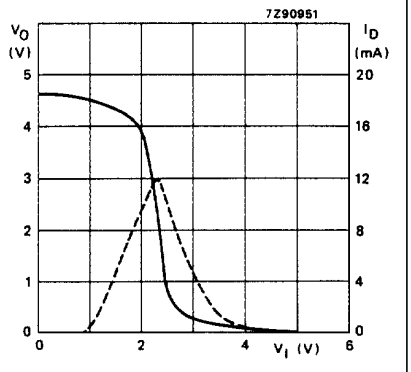


Fig.8 _____ V_O;
_ _ _ _ I_D (drain current);
I_O = 0; V_{CC} = 4.5 V.

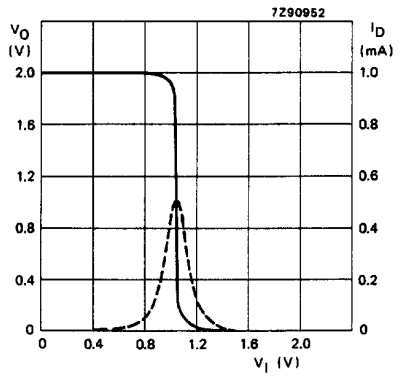


Fig.9 _____ V_O;
_ _ _ _ I_D (drain current);
I_O = 0; V_{CC} = 2.0 V.

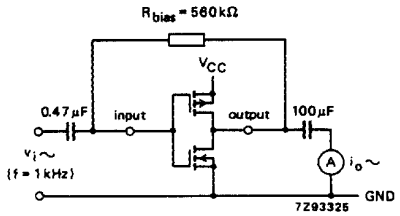


Fig.10 Test set-up for measuring forward transconductance $g_{fs} = di_o/dv_i$ at v_o is constant (see also graph Fig.11).

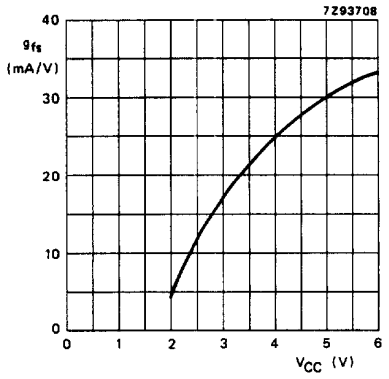
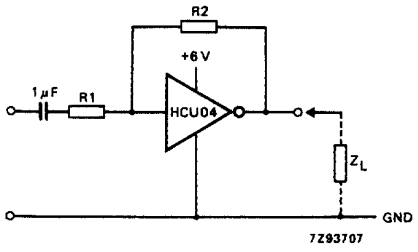


Fig.11 Typical forward transconductance g_{fs} as a function of the supply voltage V_{CC} at T_{amb} = 25°C.

APPLICATION INFORMATION

Some applications for the “HCU04” are:

- Linear amplifier (see Fig.12)
- In crystal oscillator designs (see Fig.13)
- Astable multivibrator (see Fig.14)



Z_L > 10 kΩ; A_{OL} = 20 (typ.)

$$A_u = -\frac{A_{OL}}{1 + \frac{R1}{R2}(1 + A_{OL})};$$

$V_{O\ max\ (p\text{-}p)} \approx V_{CC} - 2$ V centered at $\frac{1}{2}V_{CC}$

3 kΩ ≤ R1, R2 ≤ 1 MΩ

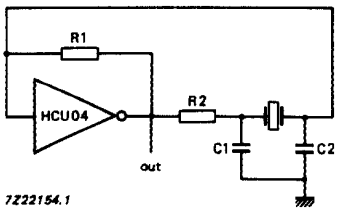
Typical unity gain bandwidth product is 5 MHz.

C_l (see Fig.15)

A_{OL} = open loop amplification

A_u = voltage amplification

Fig.12 HCU04 used as a linear amplifier.

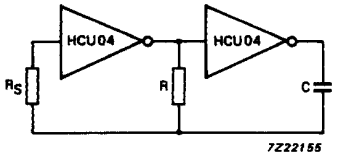


C_1 = 47 pF (typ.)
C_2 = 33 pF (typ.)
R_1 = 1 to 10 MΩ (typ.)

R_2 optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} (I_{CC} is typically 5 mA at V_{CC} = 5 V and f = 10 MHz).

Fig.13 Crystal oscillator configuration.

$$f = \frac{1}{T} \approx \frac{1}{2.2\,RC}$$



$R_S \approx 2 \times R$.

The average I_{CC} (mA) is approximately
$3.5 + 0.05 \times f$ (MHz) $\times$ C (pF) at V_{CC} = 5.0 V
(for more information refer to *"DESIGNERS GUIDE"*).

Fig.14 HCU04 used as an astable multivibrator

OPTIMUM VALUE FOR R_2

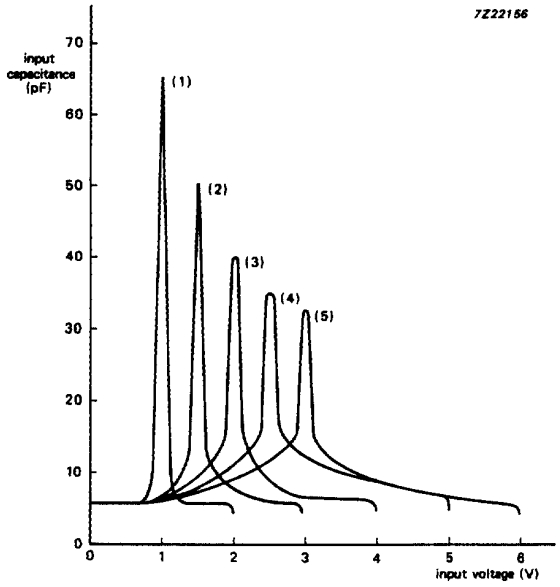
FREQUENCY (MHz)	R_2 (kΩ)	OPTIMUM FOR
3	2 8	minimum required I_{CC} minimum influence due to change in V_{CC}
6	1 4.7	minimum I_{CC} minimum influence by V_{CC}
10	0.5 2	minimum I_{CC} minimum influence by V_{CC}
14	0.5 1	minimum I_{CC} minimum influence by V_{CC}
> 14	replace R_2 by C_3 with a typical value of 35 pF	

EXTERNAL COMPONENTS FOR RESONATOR (f < 1 MHz)

FREQUENCY (kHz)	R_1 (MΩ)	R_2 (kΩ)	C_1 (pF)	C_2 (pF)
10 to 15.9	22	220	56	20
16 to 24.9	22	220	56	10
25 to 54.9	22	100	56	10
55 to 129.9	22	100	47	5
130 to 199.9	22	47	47	5
200 to 349.9	10	47	47	5
350 to 600	10	47	47	5

Note

1. All values given are typical and must be used as an initial set-up.



(1) V_{CC} = 2.0 V.
(2) V_{CC} = 3.0 V.
(3) V_{CC} = 4.0 V.
(4) V_{CC} = 5.0 V.
(5) V_{CC} = 6.0 V.

Fig.15 Typical input capacitance as a function of input voltage.

Note to Application information

All values given are typical unless otherwise specified.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.