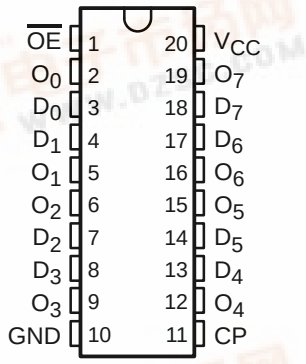
CY54FCT374T, CY74FCT374T 8-BIT REGISTERS WITH 3-STATE OUTPUTS

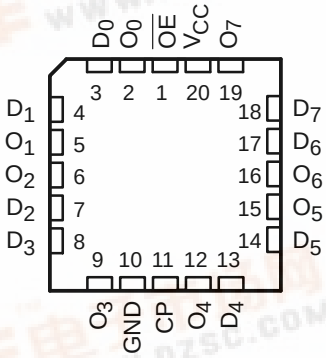
SCCS022A – MAY 1994 – REVISED OCTOBER 2001

- **Function, Pinout, and Drive Compatible With FCT and F Logic**
- **Reduced V_{OH} (Typically = 3.3 V) Versions of Equivalent FCT Functions**
- **Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Matched Rise and Fall Times**
- **Fully Compatible With TTL Input and Output Logic Levels**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **Edge-Triggered D-Type Inputs**
- **250-MHz Typical Switching Rate**
- **CY54FCT374T**
  - **32-mA Output Sink Current**
  - **12-mA Output Source Current**
- **CY74FCT374T**
  - **64-mA Output Sink Current**
  - **32-mA Output Source Current**
- **3-State Outputs**

CY54FCT374T . . . D PACKAGE
CY74FCT374T . . . P, Q, OR SO PACKAGE
(TOP VIEW)



CY54FCT374T . . . L PACKAGE
(TOP VIEW)



description

The ’FCT374T devices are high-speed, low-power, octal D-type flip-flops, featuring separate D-type inputs for each flip-flop. These devices have 3-state outputs for bus-oriented applications. A buffered clock (CP) and output-enable ($\overline{OE}$) inputs are common to all flip-flops. The eight flip-flops in the ’FCT374T store the state of their individual D inputs that meet the setup-time and hold-time requirements on the low-to-high CP transition. When $\overline{OE}$ is low, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state. The state of $\overline{OE}$ does not affect the state of the flip-flops.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	5.2	CY74FCT374CTQCT	FCT374C
	SOIC – SO	Tube	5.2	CY74FCT374CTSOC	FCT374C
		Tape and reel	5.2	CY74FCT374CTSOCT	
	DIP – P	Tube	6.5	CY74FCT374ATPC	CY74FCT374ATPC
	QSOP – Q	Tape and reel	6.5	CY74FCT374ATQCT	FCT374A
	SOIC – SO	Tube	6.5	CY74FCT374ATSOC	FCT374A
		Tape and reel	6.5	CY74FCT374ATSOCT	
	QSOP – Q	Tape and reel	10	CY74FCT374TQCT	FCT374
	SOIC – SO	Tube	10	CY74FCT374TSOC	FCT374
		Tape and reel	10	CY74FCT374TSOCT	
–55°C to 125°C	CDIP – D	Tube	6.2	CY54FCT374CTDMB	
	LCC – L	Tube	6.2	CY54FCT374CTLMB	
	CDIP – D	Tube	7.2	CY54FCT374ATDMB	
	LCC – L	Tube	7.2	CY54FCT374ATLMB	
	CDIP – D	Tube	11	CY54FCT374TDMB	
	LCC – L	Tube	11	CY54FCT374TLMB	

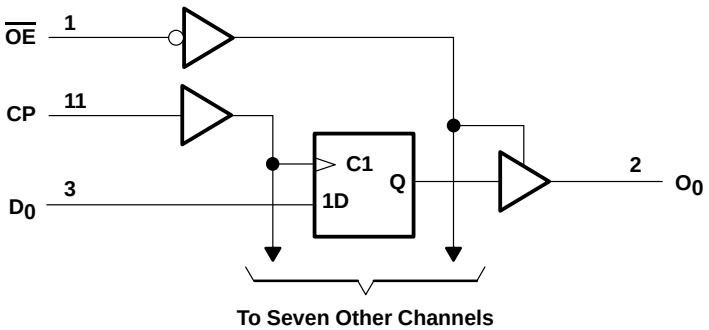
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			OUTPUT
D	CP	$\overline{OE}$	O
H	↑	L	H
L	↑	L	L
X	X	H	Z

H = High logic level, L = Low logic level,
X = Don't care, Z = High-impedance state,
↑ = Low-to-high clock transition

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range to ground potential . . . . . –0.5 V to 7 V
DC input voltage range . . . . . –0.5 V to 7 V
DC output voltage range . . . . . –0.5 V to 7 V
DC output current (maximum sink current/pin) . . . . . 120 mA
Package thermal impedance, θ_{JA} (see Note 1): P package . . . . . 69°C/W
Q package . . . . . 68°C/W
SO package . . . . . 58°C/W
Ambient temperature range with power applied, T_A . . . . . –65°C to 135°C
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 2)

		CY54FCT374T			CY74FCT374T			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–32	mA
I_{OL}	Low-level output current			32			64	mA
T_A	Operating free-air temperature	–55		125	–40		85	°C

NOTE 2: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			CY54FCT374T			CY74FCT374T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_{IN} = –18 mA			–0.7	–1.2				V
	V_{CC} = 4.75 V,	I_{IN} = –18 mA						–0.7	–1.2	
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –12 mA		2.4	3.3					V
	V_{CC} = 4.75 V	I_{OH} = –32 mA					2			
		I_{OH} = –15 mA					2.4	3.3		
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 32 mA			0.3	0.55				V
	V_{CC} = 4.75 V,	I_{OL} = 64 mA						0.3	0.55	
V_{hys}	All inputs				0.2			0.2		V
I_I	V_{CC} = 5.5 V,	V_{IN} = V_{CC}				5				µA
	V_{CC} = 5.25 V,	V_{IN} = V_{CC}							5	
I_{IH}	V_{CC} = 5.5 V,	V_{IN} = 2.7 V				±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 2.7 V							±1	
I_{IL}	V_{CC} = 5.5 V,	V_{IN} = 0.5 V				±1				µA
	V_{CC} = 5.25 V,	V_{IN} = 0.5 V							±1	
I_{off}	V_{CC} = 0 V,	V_{OUT} = 4.5 V				±1			±1	µA
I_{OS}‡	V_{CC} = 5.5 V,	V_{OUT} = 0 V		–60	–120	–225				mA
	V_{CC} = 5.25 V,	V_{OUT} = 0 V					–60	–120	–225	
I_{OZH}	V_{CC} = 5.5 V,	V_{IN} = 2.7 V				10				µA
	V_{CC} = 5.25 V,	V_{IN} = 2.7 V							10	
I_{OZL}	V_{CC} = 5.5 V,	V_{IN} = 0.5 V				–10				µA
	V_{CC} = 5.25 V,	V_{IN} = 0.5 V							–10	
I_{CC}	V_{CC} = 5.5 V,	V_{IN} ≤ 0.2 V,	V_{IN} ≥ V_{CC} – 0.2 V		0.1	0.2				mA
	V_{CC} = 5.25 V,	V_{IN} ≤ 0.2 V,	V_{IN} ≥ V_{CC} – 0.2 V					0.1	0.2	
ΔI_{CC}	V_{CC} = 5.5 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open				0.5	2				mA
	V_{CC} = 5.25 V, V_{IN} = 3.4 V§, f_1 = 0, Outputs open							0.5	2	

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

§ Per TTL-driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS			CY54FCT374T			CY74FCT374T			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CCD}¶	V_{CC} = 5.5 V, Outputs open, One bit switching at 50% duty cycle, $\overline{OE}$ = GND, $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V				0.06	0.12				mA/ MHz
	V_{CC} = 5.25 V, Outputs open, One bit switching at 50% duty cycle, $\overline{OE}$ = GND, $V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V							0.06	0.12	
I_C	V_{CC} = 5.5 V, f_0 = 10 MHz, Outputs open, $\overline{OE}$ = GND	One bit switching at f_1 = 5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V		0.7	1.4				mA
			V_{IN} = 3.4 V or GND		1.2	3.4				
		Eight bits switching at f_1 = 2.5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V		1.6	3.2‖				
			V_{IN} = 3.4 V or GND		3.9	12.2‖				
	V_{CC} = 5.25 V, f_0 = 10 MHz, Outputs open, $\overline{OE}$ = GND	One bit switching at f_1 = 5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V					0.7	1.4	
			V_{IN} = 3.4 V or GND					1.2	3.4	
		Eight bits switching at f_1 = 2.5 MHz at 50% duty cycle	$V_{IN} \le 0.2$ V or $V_{IN} \ge V_{CC} - 0.2$ V					1.6	3.2‖	
			V_{IN} = 3.4 V or GND					3.9	12.2‖	
C_i					5	10		5	10	pF
C_o					9	12		9	12	pF

† Typical values are at V_{CC} = 5 V, T_A = 25°C.

¶ This parameter is derived for use in total power-supply calculations.

$I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current
I_{CC} = Power-supply current with CMOS input levels
ΔI_{CC} = Power-supply current for a TTL high input (V_{IN} = 3.4 V)
D_H = Duty cycle for TTL inputs high
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)
f_0 = Clock frequency for registered devices, otherwise zero
f_1 = Input signal frequency
N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

‖ Values for these conditions are examples of the I_{CC} formula.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		CY54FCT374T		CY54FCT374AT		CY54FCT374CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CP high or low	7		6		6		ns
t_{su}	Setup time, data before CP↑	2		2		2		ns
t_h	Hold time, data after CP↑	1.5		1.5		1.5		ns

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		CY74FCT374T		CY74FCT374AT		CY74FCT374CT		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, CP high or low	7		5		5		ns
t_{su}	Setup time, data before CP↑	2		2		2		ns
t_h	Hold time, data after CP↑	1.5		1.5		1.5		ns

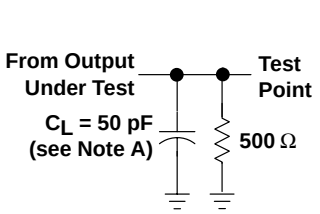
switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY54FCT374T		CY54FCT374AT		CY54FCT374CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	CP	O	2	11	2	7.2	2	6.2	ns
t_{PHL}			2	11	2	7.2	2	6.2	
t_{PZH}	$\overline{OE}$	O	1.5	14	1.5	7.5	1.5	6.2	ns
t_{PZL}			1.5	14	1.5	7.5	1.5	6.2	
t_{PHZ}	$\overline{OE}$	O	1.5	8	1.5	6.5	1.5	5.7	ns
t_{PLZ}			1.5	8	1.5	6.5	1.5	5.7	

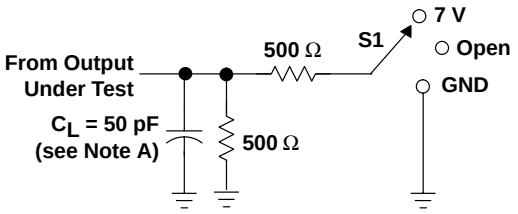
switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CY74FCT374T		CY74FCT374AT		CY74FCT374CT		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	CP	O	2	10	2	6.5	2	5.2	ns
t_{PHL}			2	10	2	6.5	2	5.2	
t_{PZH}	$\overline{OE}$	O	1.5	12.5	1.5	6.5	1.5	5.5	ns
t_{PZL}			1.5	12.5	1.5	6.5	1.5	5.5	
t_{PHZ}	$\overline{OE}$	O	1.5	8	1.5	5.5	1.5	5	ns
t_{PLZ}			1.5	8	1.5	5.5	1.5	5	

PARAMETER MEASUREMENT INFORMATION

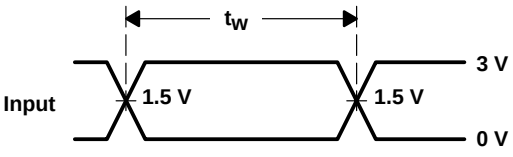


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

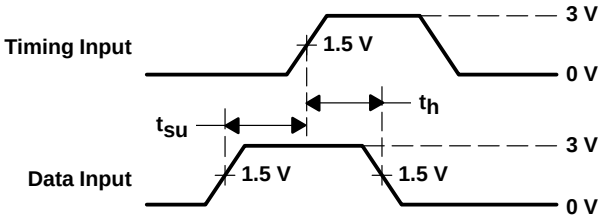


LOAD CIRCUIT FOR
3-STATE OUTPUTS

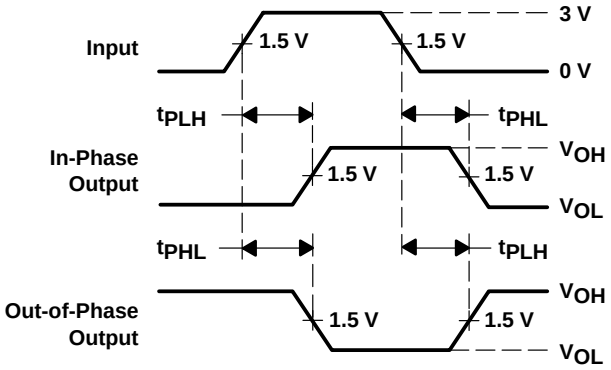
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



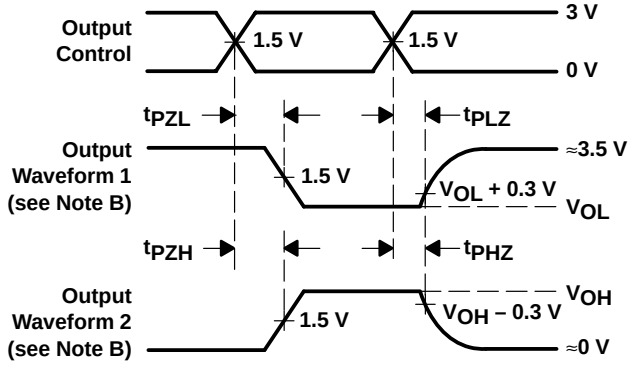
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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