12-BIT, ULTRALOW GLITCH, VOLTAGE OUTPUT DIGITAL-TO-ANALOG CONVERTER

FEATURES

- 2.7-V to 5.5-V Single Supply
- 12-Bit Linearity and Monotonicity
- Rail-to-Rail Voltage Output
- Settling Time: 5 µs (Max)
- Ultralow Glitch Energy: 0.1 nVs
- Low Power: 200 µA (Max)
- Power Down: 2 µA (Max)
- Power-On Reset to Zero Scale
- SPI-Compatible Serial Interface: Up to 50 MHz
- Daisy-Chain Capability
- Asynchronous Hardware Clear
- Specified Temperature Range: –40°C to 105°C
- Small, 2-mm x 3-mm, 12-Lead SON Package

APPLICATIONS

- Portable Battery-Powered Instruments
- Digital Gain and Offset Adjustment
- Programmable Voltage and Current Sources
- Programmable Attenuators
- Industrial Process Control

DESCRIPTION

The DAC7551 is a single-channel, voltage-output DAC with exceptional linearity and monotonicity. Its proprietary architecture minimizes glitch energy. The low-power DAC7551 operates from a single 2.7-V to 5.5-V supply. The DAC7551 output amplifiers can drive a 2-kΩ, 200-pF load rail-to-rail with 5-µs settling time; the output range is set using an external voltage reference.

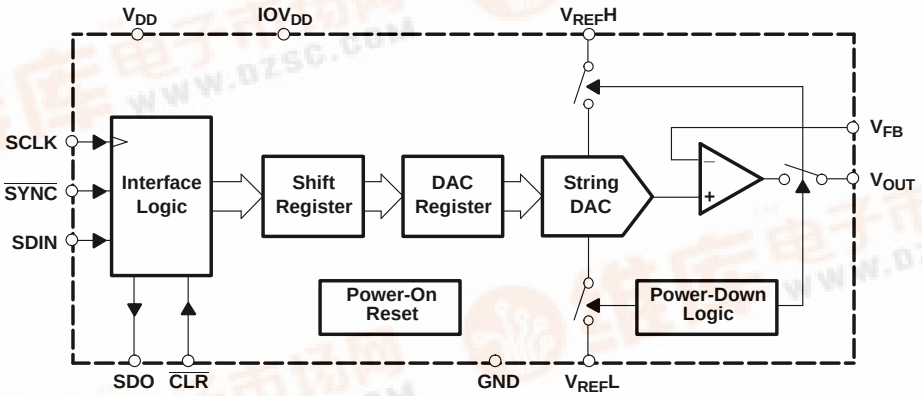
The 3-wire serial interface operates at clock rates up to 50 MHz and is compatible with SPI, QSPI, Microwire™, and DSP interface standards. The parts incorporate a power-on-reset circuit to ensure that the DAC outputs power up to zero volts and remain there until a valid write cycle to the device takes place. The parts contain a power-down feature that reduces the current consumption of the device to under 2 µA.

The small size and low-power operation makes the DAC7551 ideally suited for battery-operated portable applications. The power consumption is typically 0.5 mW at 5 V, 0.23 mW at 3 V, and reduces to 1 µW in power-down mode.

The DAC7551 is available in a 12-lead SON package and is specified over –40°C to 105°C.

PRODUCT PREVIEW

FUNCTIONAL BLOCK DIAGRAM



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
DAC7551	12 SON	DRN	–40°C TO 105°C	D51	DAC7551IDRNT	250-piece Tape and Reel
					DAC7551IDRNR	2500-piece Tape and Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

	UNIT
V_{DD} to GND	–0.3 V to 6 V
Digital input voltage to GND	–0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	–0.3 V to V_{DD}+ 0.3 V
Operating temperature range	–40°C to 105°C
Storage temperature range	–65°C to 150°C
Junction temperature (T_J Max)	150°C

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = GND, R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications –40°C to 105°C, unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE(1)					
Resolution			12		Bits
Relative accuracy			±0.35	±1	LSB
Differential nonlinearity	Specified monotonic by design		±0.08	±0.5	LSB
Offset error				±12	mV
Zero-scale error	All zeroes loaded to DAC register			±12	mV
Gain error				±0.15	%FSR
Full-scale error				±0.5	%FSR
Zero-scale error drift			7		µV/°C
Gain temperature coefficient			3		ppm of FSR/°C
PSRR	V_{DD} = 5 V		0.75		mV/V
OUTPUT CHARACTERISTICS(2)					
Output voltage range		2 x $V_{REF}L$		$V_{REF}H$	V
Output voltage settling time	R_L = 2 kΩ; 0 pF < C_L < 200 pF			5	µs
Slew rate			1		V/µs
Capacitive load stability	R_L = ∞		470		pF
	R_L = 2 kΩ		1000		
Digital-to-analog glitch impulse	1 LSB change around major carry		0.1		nV-s
Digital feedthrough			0.1		nV-s
Output noise density (10-kHz offset frequency)			70		nV/rtHz
Total harmonic distortion	F_{OUT} = 1 kHz, F_S = 1 MSPS, BW = 20 kHz		–85		dB
DC output impedance			1		Ω
Short-circuit current	V_{DD} = 5 V		50		mA
	V_{DD} = 3 V		20		
Power-up time	Coming out of power-down mode, V_{DD} = 5 V		15		µs
	Coming out of power-down mode, V_{DD} = 3 V		15		
REFERENCE INPUT					
$V_{REF}H$, Input range		0		V_{DD}	V
$V_{REF}L$, Input range	$V_{REF}L < V_{REF}H$	0	GND	V_{DD}	V
Reference input impedance			100		kΩ
Reference current	$V_{REF} = V_{DD}$ = 5 V		130	250	µA
	$V_{REF} = V_{DD}$ = 3 V		65	123	
LOGIC INPUTS(2)					
Input current				±1	µA
V_{IN_L}, Input low voltage	V_{DD} = 5 V			0.3 V_{DD}	V
V_{IN_H}, Input high voltage	V_{DD} = 3 V	0.7 V_{DD}			V
Pin capacitance				3	pF

(1) Linearity tested using a reduced code range of 30 to 4065; output unloaded.
(2) Specified by design and characterization, not production tested.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (Continued)

V_{DD} = 2.7 V to 5.5 V, $V_{REF}H = V_{DD}$, $V_{REF}L$ = GND, R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications –40°C to 105°C, unless otherwise specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER REQUIREMENTS					
V_{DD}		2.7		5.5	V
I_{DD}(normal operation)	DAC active and excluding load current $V_{IH} = V_{DD}$ and V_{IL} = GND				
V_{DD} = 3.6 V to 5.5 V			150	200	µA
V_{DD} = 2.7 V to 3.6 V			100	150	
I_{DD} (all power-down modes)	$V_{IH} = V_{DD}$ and V_{IL} = GND				
V_{DD} = 3.6 V to 5.5 V			0.2	2	µA
V_{DD} = 2.7 V to 3.6 V			0.05	2	
Reference input impedance			100		kΩ
POWER EFFICIENCY					
I_{OUT}/I_{DD}	I_{LOAD} = 2 mA, V_{DD} = 5 V		93%		

PRODUCT PREVIEW

TIMING CHARACTERISTICS(1)(2)

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND; all specifications –40°C to 105°C, unless otherwise specified

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
t_1(3)	SCLK cycle time	V_{DD} = 2.7 V to 3.6 V	20			ns
		V_{DD} = 3.6 V to 5.5 V	20			
t_2	SCLK HIGH time	V_{DD} = 2.7 V to 3.6 V	10			ns
		V_{DD} = 3.6 V to 5.5 V	10			
t_3	SCLK LOW time	V_{DD} = 2.7 V to 3.6 V	10			ns
		V_{DD} = 3.6 V to 5.5 V	10			
t_4	$\overline{SYNC}$ falling edge to SCLK falling edge setup time	V_{DD} = 2.7 V to 3.6 V	4			ns
		V_{DD} = 3.6 V to 5.5 V	4			
t_5	Data setup time	V_{DD} = 2.7 V to 3.6 V	5			ns
		V_{DD} = 3.6 V to 5.5 V	5			
t_6	Data hold time	V_{DD} = 2.7 V to 3.6 V	4.5			ns
		V_{DD} = 3.6 V to 5.5 V	4.5			
t_7	SCLK falling edge to $\overline{SYNC}$ rising edge	V_{DD} = 2.7 V to 3.6 V	0			ns
		V_{DD} = 3.6 V to 5.5 V	0			
t_8	Minimum $\overline{SYNC}$ HIGH time	V_{DD} = 2.7 V to 3.6 V	20			ns
		V_{DD} = 3.6 V to 5.5 V	20			
t_9	SCLK falling edge to SDO valid	V_{DD} = 2.7 V to 3.6 V	TBD			ns
		V_{DD} = 3.6 V to 5.5 V	TBD			
t_{10}	$\overline{CLR}$ pulse width low	V_{DD} = 2.7 V to 3.6 V	TBD			ns
		V_{DD} = 3.6 V to 5.5 V	TBD			

(1) All input signals are specified with $t_R = t_F$ = 1 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) See Serial Write Operation timing diagram Figure 1.
(3) Maximum SCLK frequency is 50 MHz at V_{DD} = 2.7 V to 5.5 V.

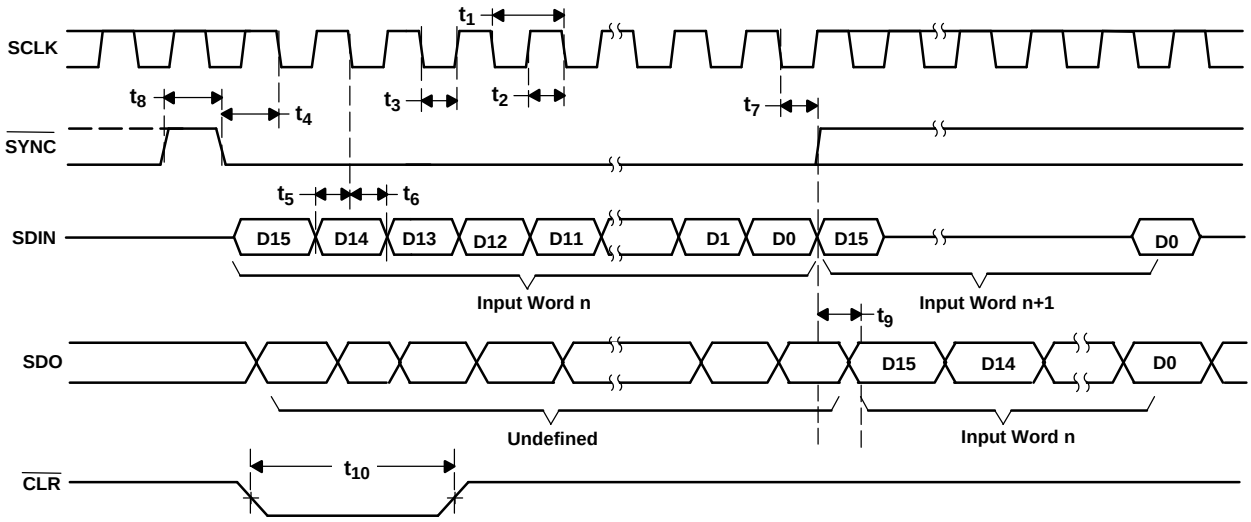
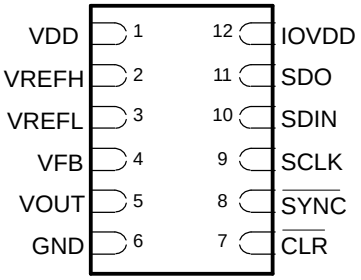


Figure 1. Serial Write Operation

PRODUCT PREVIEW

PIN DESCRIPTION

DRN PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL		DESCRIPTION
NO.	NAME	
1	VDD	Analog voltage supply input
2	VREFH	Positive reference voltage input
3	VREFL	Negative reference voltage input
4	VFB	DAC amplifier sense input.
5	VOUT	Analog output voltage from DAC
6	GND	Ground
7	$\overline{\text{CLR}}$	Asynchronous input to clear the DAC registers. When CLR is low, the DAC register is set to 000H and the output voltage to 0 V.
8	$\overline{\text{SYNC}}$	Frame synchronization input. The falling edge of the $\overline{\text{SYNC}}$ pulse indicates the start of a serial data frame shifted out to the DAC7551.
9	SCLK	Serial clock input
10	SDIN	Serial data input
11	SDO	Serial data output
12	IOVDD	I/O voltage supply input

TYPICAL CHARACTERISTICS

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR VS DIGITAL INPUT CODE

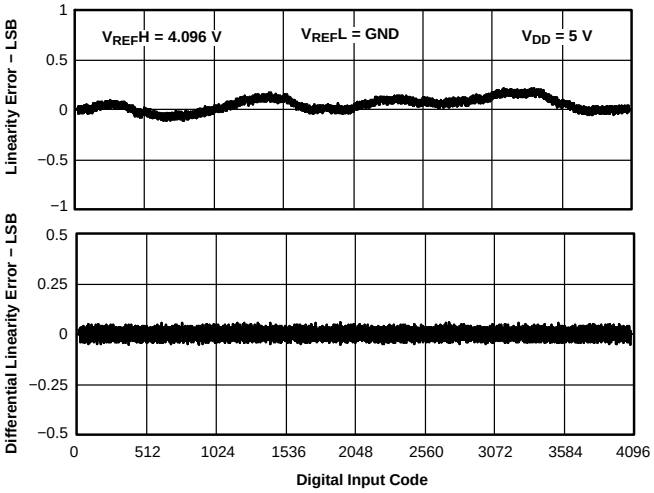


Figure 2.

LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR VS DIGITAL INPUT CODE

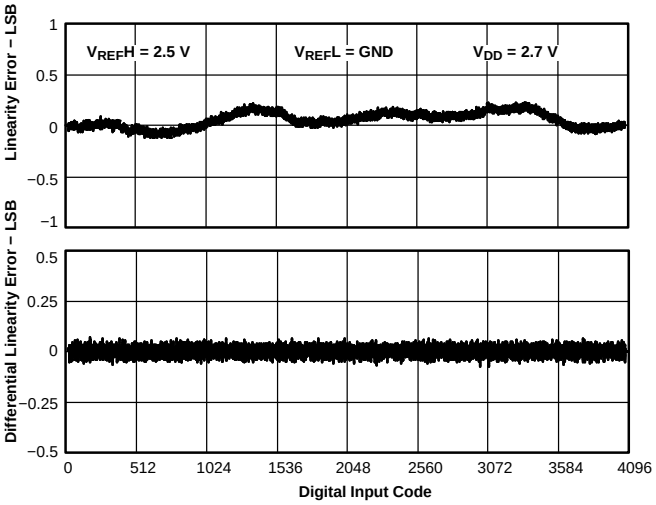


Figure 3.

ZERO-SCALE ERROR VS FREE-AIR TEMPERATURE

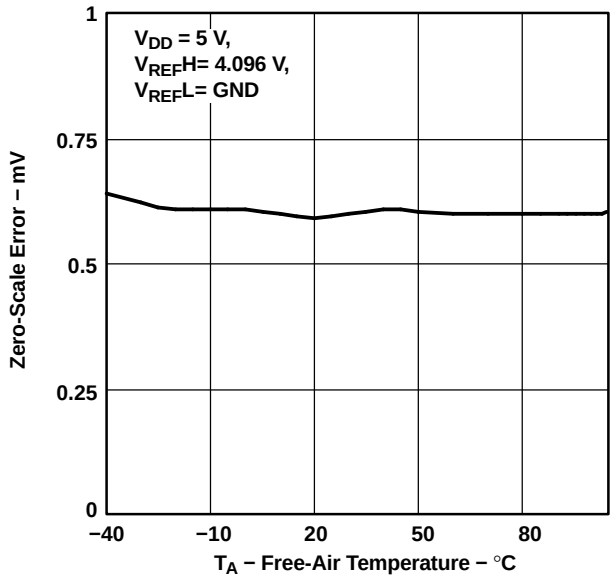


Figure 4.

ZERO-SCALE ERROR VS FREE-AIR TEMPERATURE

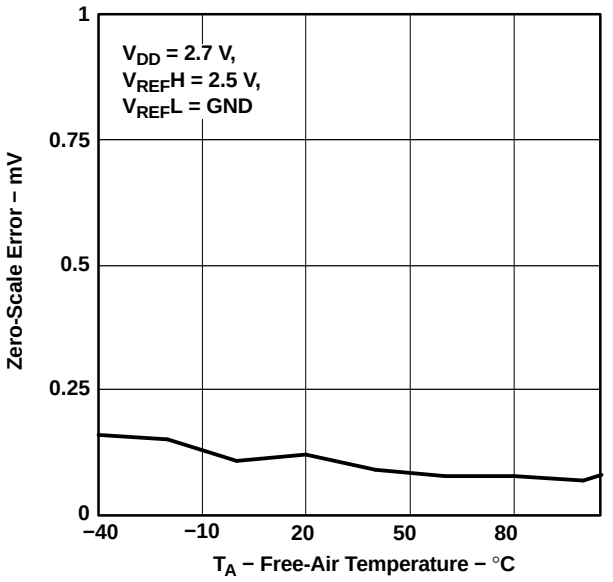


Figure 5.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

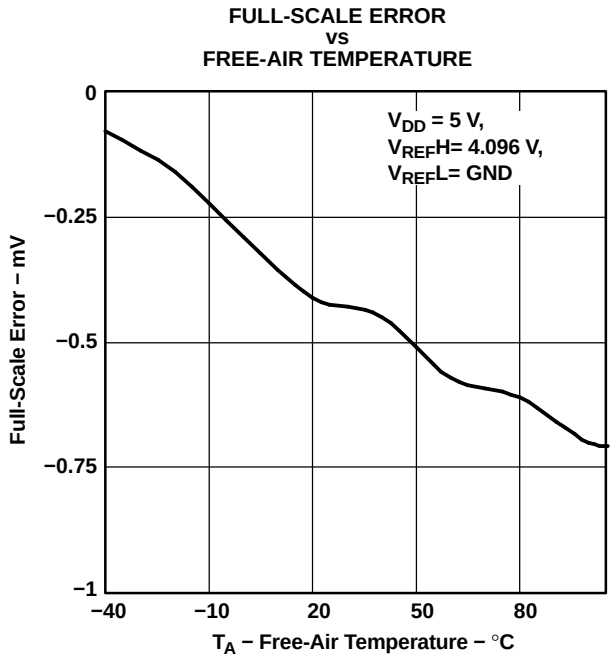


Figure 6.

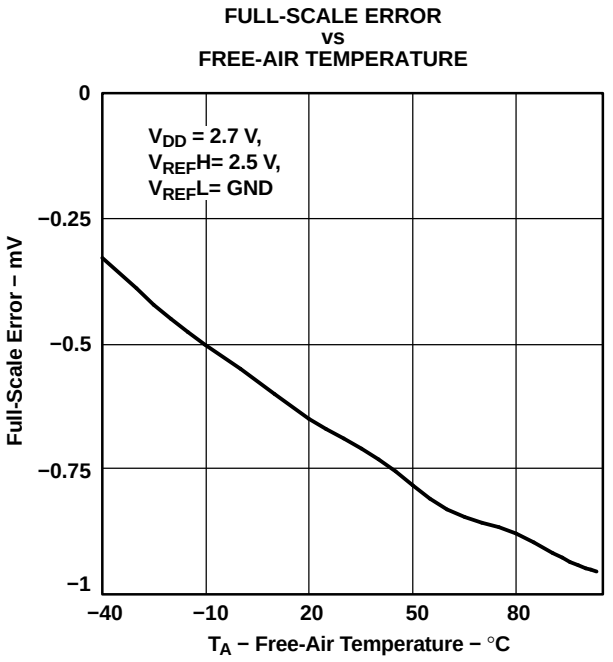


Figure 7.

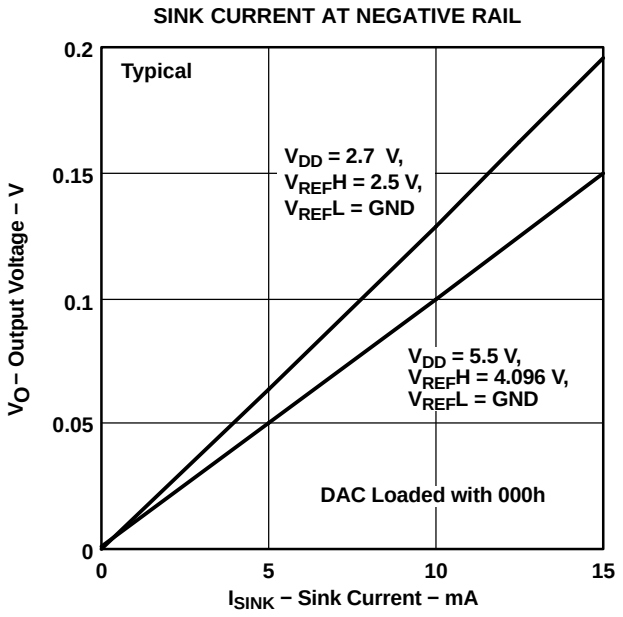


Figure 8.

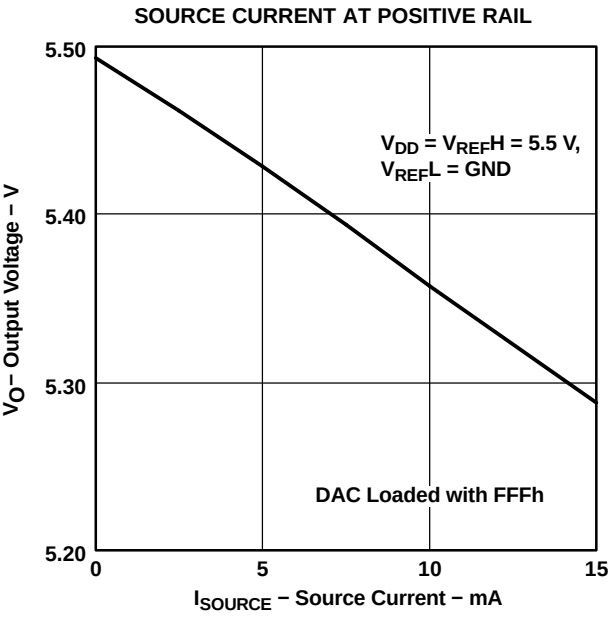


Figure 9.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

SOURCE CURRENT AT POSITIVE RAIL

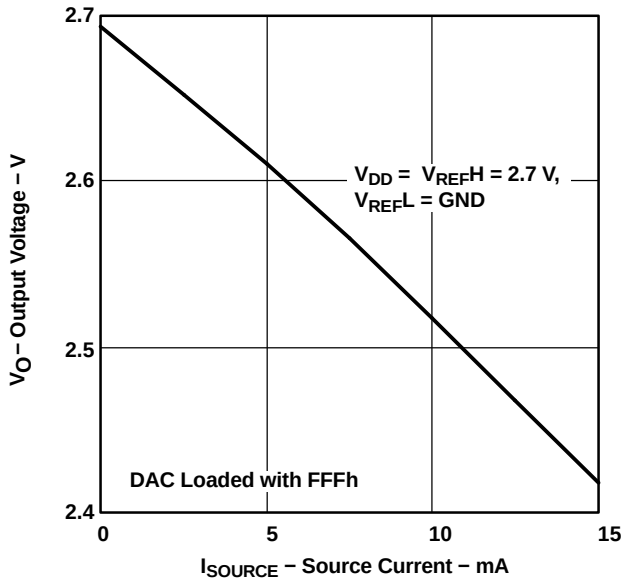


Figure 10.

SUPPLY CURRENT
vs
DIGITAL INPUT CODE

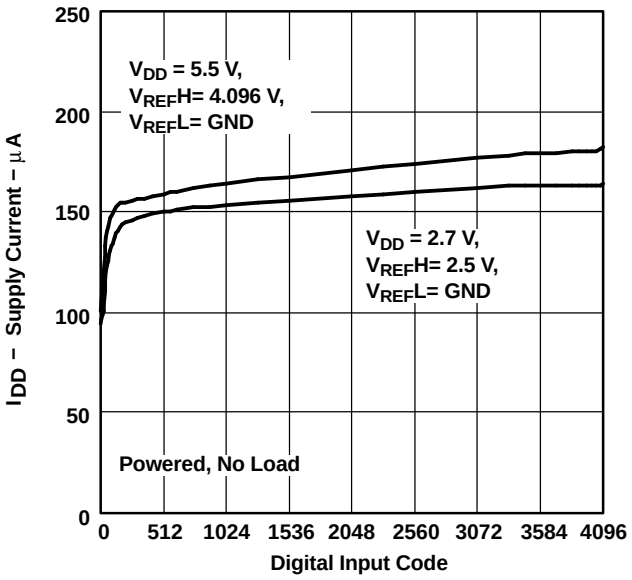


Figure 11.

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

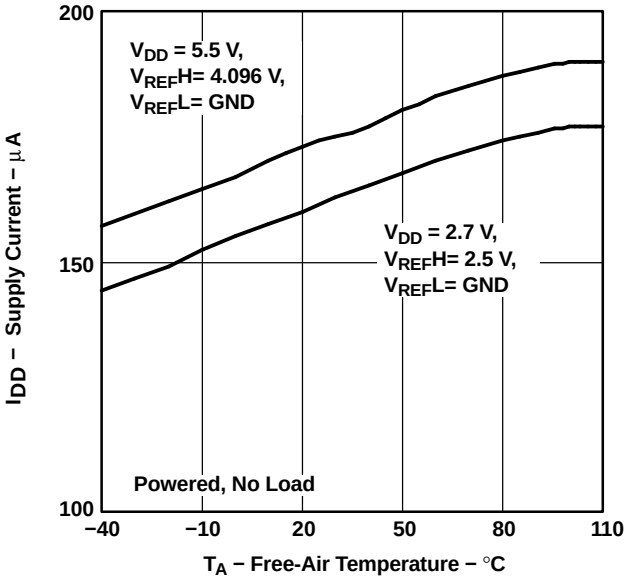


Figure 12.

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

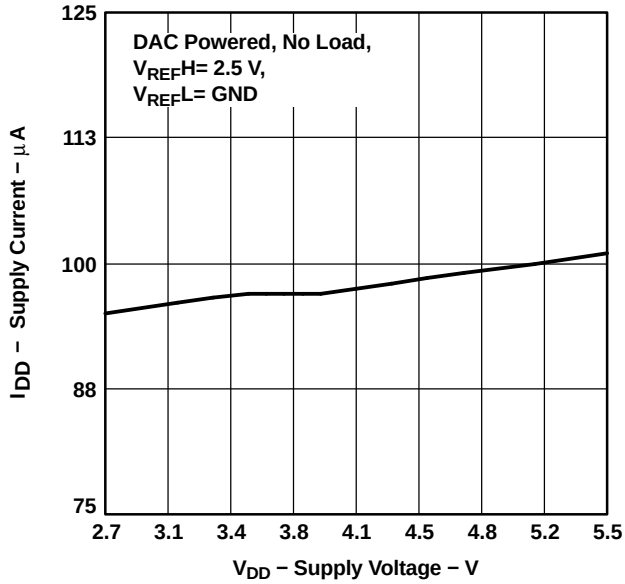


Figure 13.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

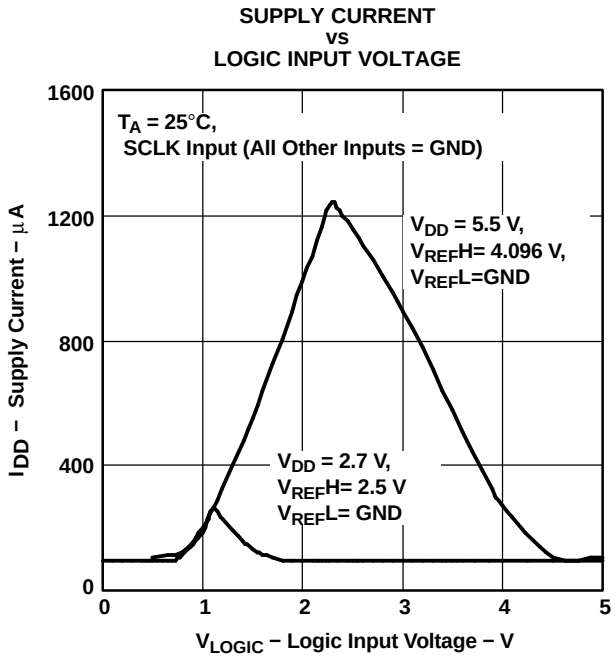


Figure 14.

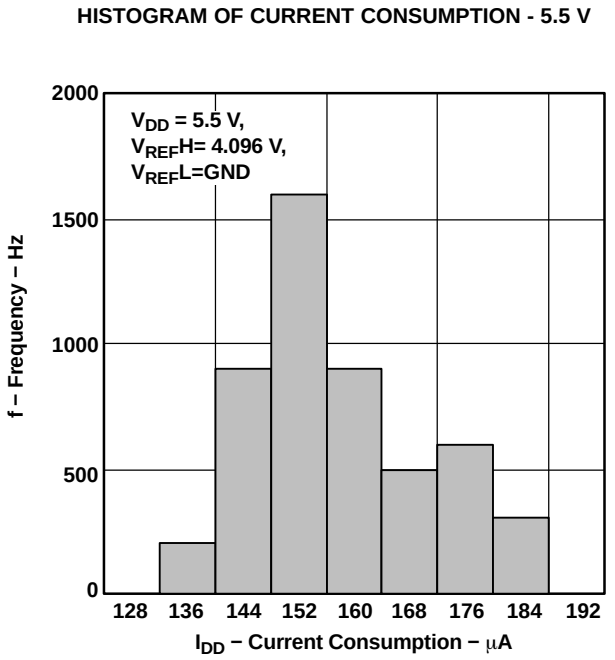


Figure 15.

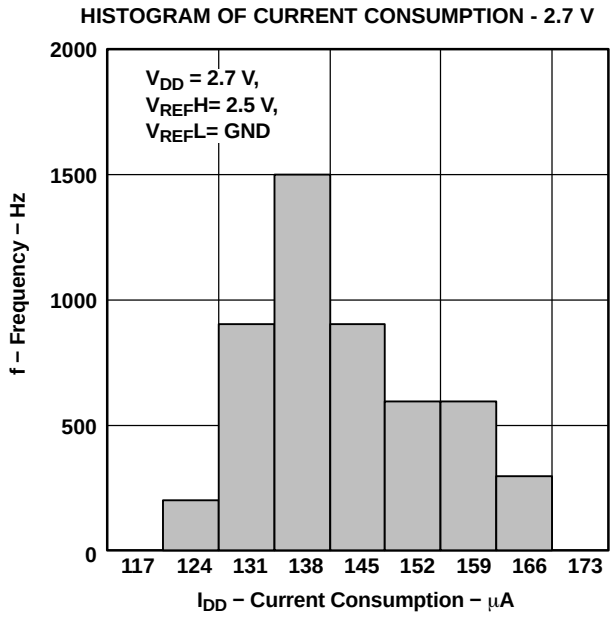


Figure 16.

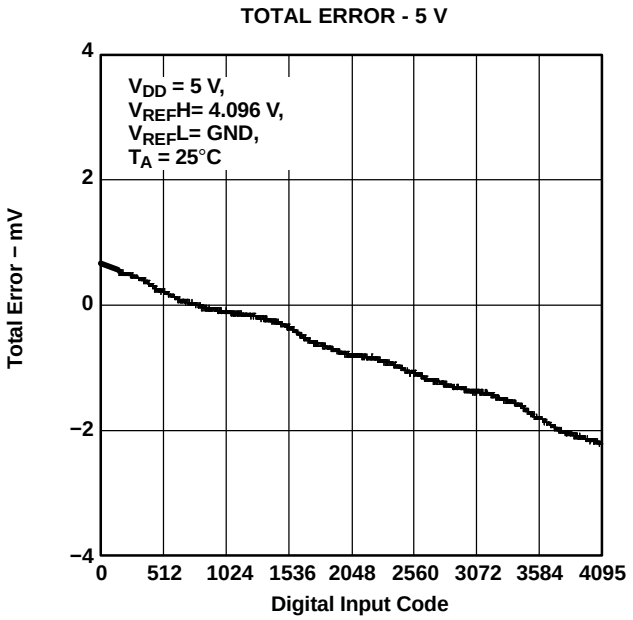


Figure 17.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

TOTAL ERROR - 2.7 V

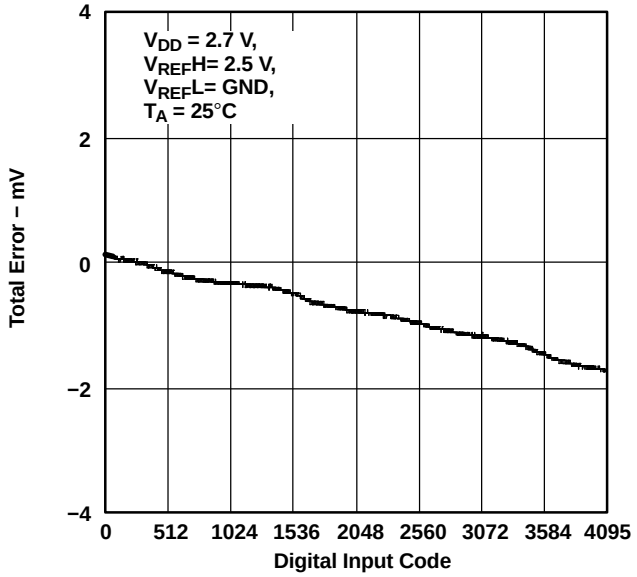


Figure 18.

EXITING POWER-DOWN MODE

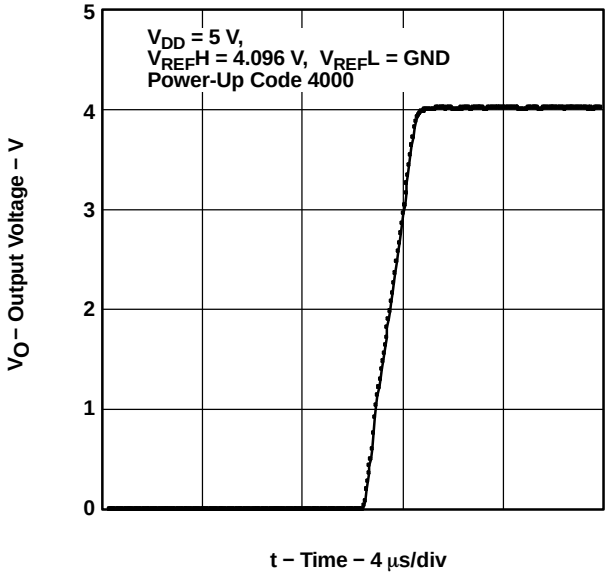


Figure 19.

LARGE-SIGNAL SETTLING TIME - 5 V

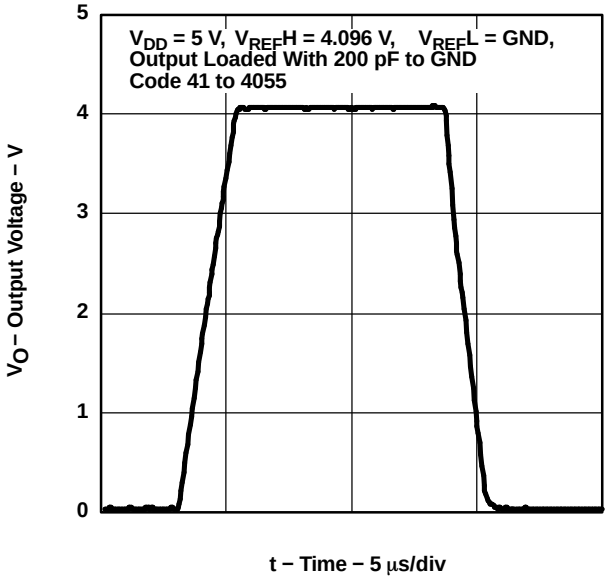


Figure 20.

LARGE-SIGNAL SETTLING TIME - 2.7 V

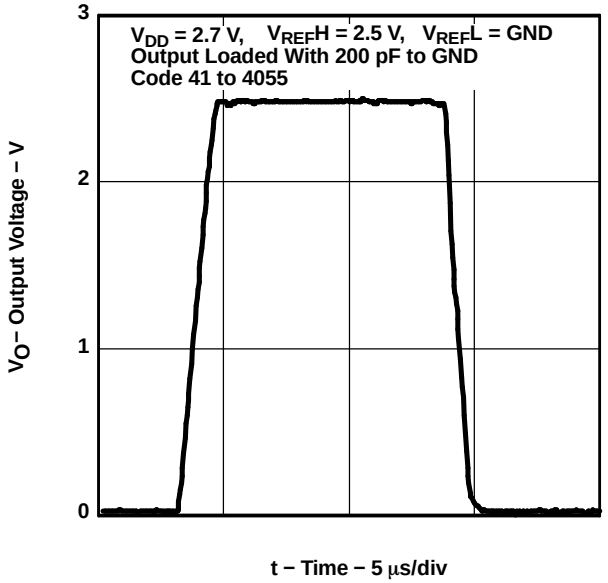


Figure 21.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

MIDSCALE GLITCH

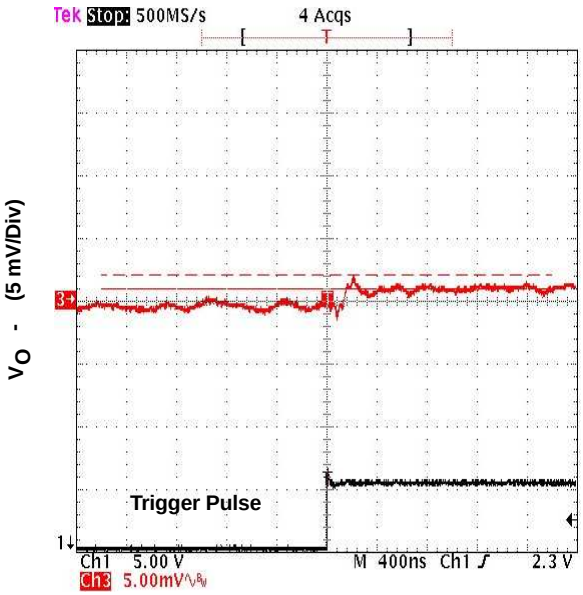


Figure 22.

WORST-CASE GLITCH

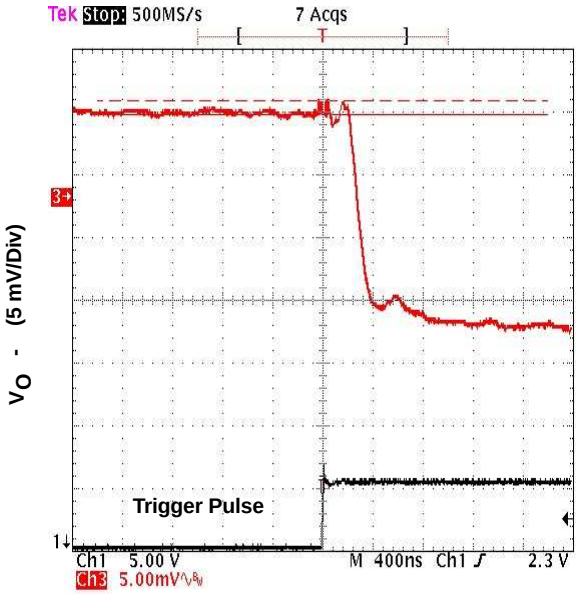


Figure 23.

DIGITAL FEEDTHROUGH ERROR

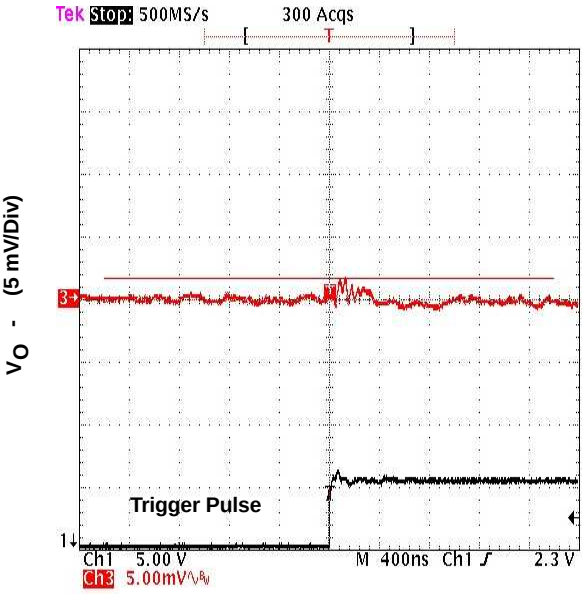


Figure 24.

TOTAL HARMONIC DISTORTION
vs
OUTPUT FREQUENCY

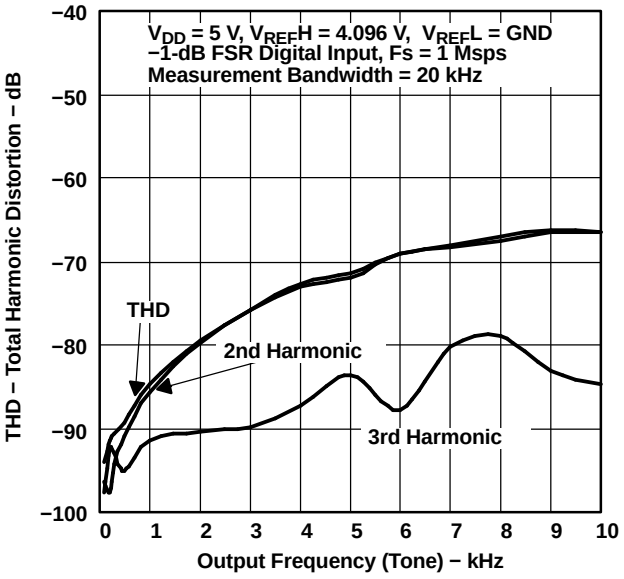


Figure 25.

PRODUCT PREVIEW

TYPICAL CHARACTERISTICS (continued)

3-Wire Serial Interface

The DAC7551 digital interface is a standard 3-wire SPI/QSPI/Microwire/DSP-compatible interface.

Table 1. Serial Interface Programming

CONTROL				DATA BITS	FUNCTION
DB15	DB14	DB13 (PD1)	DB12 (PD0)	DB11–DB0	
X	X	0	0	data	Normal mode
X	X	0	1	X	Powerdown 1 kΩ
X	X	1	0	X	Powerdown 100 kΩ
X	X	1	1	X	Powerdown Hi-Z

THEORY OF OPERATION

D/A SECTION

The architecture of the DAC7551 consists of a string DAC followed by an output buffer amplifier. Figure 26 shows a generalized block diagram of the DAC architecture.

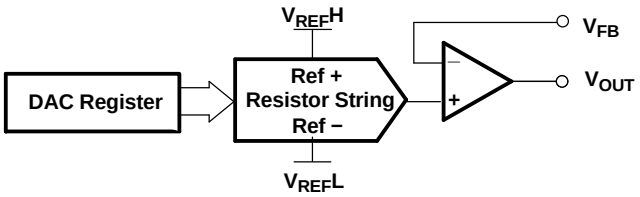


Figure 26. Typical DAC Architecture

The input coding to the DAC7551 is unsigned binary, which gives the ideal output voltage as:

$$V_{OUT} = 2 \times V_{REF}L + (V_{REF}H - V_{REF}L) \times D/4096$$

Where D = decimal equivalent of the binary code that is loaded to the DAC register which can range from 0 to 4095.

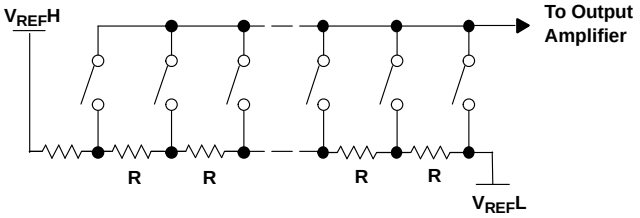


Figure 27. Typical Resistor String

RESISTOR STRING

The resistor string section is shown in Figure 27. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is specified monotonic.

OUTPUT BUFFER AMPLIFIERS

The output buffer amplifier is capable of generating rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. It is capable of driving a load of 2 kΩ in parallel with up to 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical curves. The slew rate is 1 V/µs with a half-scale settling time of 3 µs with the output unloaded.

DAC External Reference Input

There is a single reference input pin for the DAC. The reference input is unbuffered. The user can have a reference voltage as low as 0.25 V and as high as V_{DD} because there is no restriction due to headroom and footroom of any reference amplifier.

It is recommended to use a buffered reference in the external circuit (e.g., REF3140). The input impedance is typically 100 kΩ.

Power-On Reset

On power up, the internal register is cleared and the DAC channel is updated with zero-scale voltage. The DAC output remains in this state until valid data is written. This is particularly useful in applications where it is important to know the state of the DAC output while the device is powering up. In order not to turn on ESD protection devices, V_{DD} should be applied before any other pin is brought high.

Power Down

The DAC7551 has a flexible power-down capability. During a power-down condition, the user has flexibility to select the output impedance of the DAC. During power-down operation, the DAC can have either 1-kΩ, 100-kΩ, or Hi-Z output impedance to ground.

Asynchronous Clear

The DAC7551 output is asynchronously set to zero-scale voltage immediately after the $\overline{CLR}$ pin is brought low. The $\overline{CLR}$ signal resets all internal registers and therefore behaves like the Power-On Reset. The DAC7551 updates at the first rising edge of the $\overline{SYNC}$ signal that occurs after the $\overline{CLR}$ pin is brought back to high.

SERIAL INTERFACE

The DAC7551 is controlled over a versatile 3-wire serial interface, which operates at clock rates up to 50 MHz and is compatible with SPI, QSPI, Microwire, and DSP interface standards.

In order to initialize the serial interface for the next update, the DAC7551 requires a falling SCLK edge after the rising $\overline{SYNC}$.

16-Bit Word and Input Shift Register

The input shift register is 16 bits wide. DAC data is loaded into the device as a 16-bit word under the control of a serial clock input, SCLK, as shown in the Figure 1 timing diagram. The 16-bit word, illustrated in Table 1, consists of four control bits followed by 12 bits of DAC data. The data format is straight binary

with all zeroes corresponding to 0-V output and all ones corresponding to full-scale output (V_{REF} – 1 LSB). Data is loaded MSB first (Bit 15) where the first two bits (DB15 and DB14) are don't care bits. Bit 13 and bit 12 (DB13 and DB12) determine either normal mode operation or power-down mode (see Table 1).

The $\overline{SYNC}$ input is a level-triggered input that acts as a frame synchronization signal and chip enable. Data can only be transferred into the device while $\overline{SYNC}$ is low. To start the serial data transfer, $\overline{SYNC}$ should be taken low, observing the minimum $\overline{SYNC}$ to SCLK falling edge setup time, t_4. After $\overline{SYNC}$ goes low, serial data is shifted into the device's input shift register on the falling edges of SCLK for 16 clock pulses.

The SPI interface is enabled after $\overline{SYNC}$ becomes low and the data is continuously shifted into the shift register at each falling edge of SCLK. When $\overline{SYNC}$ is brought high the last 16 bits stored in the shift register get latched into the DAC register, and the DAC updates.

Daisy-Chain Operation

Serial Data Output (SDO) pin is provided to daisy-chain multiple DAC7551 devices in a system. As long as $\overline{SYNC}$ is high the SDO pin is in a high-impedance state. When $\overline{SYNC}$ is brought low the output of the internal shift register is tied to the SDO pin. As long as $\overline{SYNC}$ is low, at each falling edge of SCLK, SDO duplicates SDIN signal with a 16-cycle delay. To support multiple devices in a daisy chain, SCLK and $\overline{SYNC}$ signals are shared across all devices, and SDO of one DAC7551 should be tied to the SDIN of the next DAC7551. For *n* devices in such a daisy chain, 16*n* SCLK cycles are required to shift the entire input data stream. After 16*n* SCLK falling edges are received following a falling $\overline{SYNC}$, the data stream becomes complete, and $\overline{SYNC}$ can be brought high to update *n* devices simultaneously. SDO operation is specified at a maximum SCLK speed of 10 MHz.

INTEGRAL AND DIFFERENTIAL LINEARITY

The DAC7551 uses precision thin-film resistors providing exceptional linearity and monotonicity. Integral linearity error is typically within (+/-) 0.35 LSBs, and differential linearity error is typically within (+/-) 0.08 LSBs.

GLITCH ENERGY

The DAC7551 uses a proprietary architecture that minimizes glitch energy. The code-to-code glitches are so low, they are usually buried within the wide-band noise and cannot be easily detected. The DAC7551 glitch is typically well under 0.1 nV-s. Such low glitch energy provides more than 10X improvement over industry alternatives.

APPLICATION INFORMATION

Waveform Generation

Due to its exceptional linearity and low glitch, the DAC7551 is well suited for waveform generation (from DC to 10 kHz). The DAC7551 large-signal settling time is 5 µs, supporting an update rate of 200 KSPS. However, the update rates can exceed 1 MSPS if the waveform to be generated consists of small voltage steps between consecutive DAC updates. To obtain a high dynamic range, REF3140 (4.096 V) or REF02 (5.0 V) are recommended for reference voltage generation.

Generating ±5-V, ±10-V, and ±12-V Outputs For Precision Industrial Control

Industrial control applications can require multiple feedback loops consisting of sensors, ADCs, MCUs, DACs, and actuators. Loop accuracy and loop speed are the two important parameters of such control loops.

Loop Accuracy:

In a control loop, the ADC has to be accurate. Offset, gain, and the integral linearity errors of the DAC are not factors in determining the accuracy of the loop. As long as a voltage exists in the transfer curve of a monotonic DAC, the loop can find it and settle to it. On the other hand, DAC resolution and differential linearity do determine the loop accuracy, because each DAC step determines the minimum incremental change the loop can generate. A DNL error less than –1 LSB (non-monotonicity) can create loop instability. A DNL error greater than +1 LSB implies unnecessarily large voltage steps and missed voltage targets. With high DNL errors, the loop loses its stability, resolution, and accuracy. Offering 12-bit ensured monotonicity and ± 0.08 LSB typical DNL error, 755X DACs are great choices for precision control loops.

Loop Speed:

Many factors determine control loop speed. Typically, the ADC's conversion time, and the MCU's computation time are the two major factors that dominate the time constant of the loop. DAC settling time is rarely a dominant factor because ADC conversion times usually exceed DAC conversion times. DAC offset, gain, and linearity errors can slow the loop

down only during the start-up. Once the loop reaches its steady-state operation, these errors do not affect loop speed any further. Depending on the ringing characteristics of the loop's transfer function, DAC glitches can also slow the loop down. With its 1 MSPS (small-signal) maximum data update rate, DAC7551 can support high-speed control loops. Ultralow glitch energy of the DAC7551 significantly improves loop stability and loop settling time.

Generating Industrial Voltage Ranges:

For control loop applications, DAC gain and offset errors are not important parameters. This could be exploited to lower trim and calibration costs in a high-voltage control circuit design. Using a quad operational amplifier (OPA4130), and a voltage reference (REF3140), the DAC7551 can generate the wide voltage swings required by the control loop.

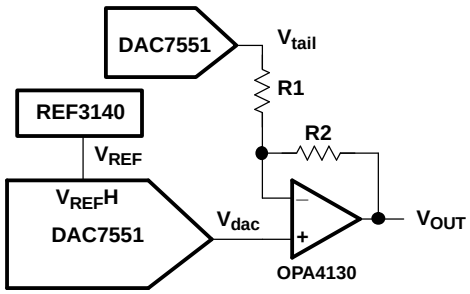


Figure 28. Low-cost, Wide-swing Voltage Generator for Control Loop Applications

The output voltage of the configuration is given by:

$$V_{out} = V_{REF}\left(\frac{R2}{R1} + 1\right)\frac{Din}{4096} - V_{tail}\ \frac{R2}{R1} \quad (1)$$

Fixed R1 and R2 resistors can be used to coarsely set the gain required in the first term of the equation. Once R2 and R1 set the gain to include some minimal over-range, a single DAC7551 could be used to set the required offset voltages. Residual errors are not an issue for loop accuracy because offset and gain errors could be tolerated. One DAC7551 can provide the V_{tail} voltages, while four additional DAC7551 devices can provide V_{dac} voltages to generate four high-voltage outputs. A single SPI interface is sufficient to control all five DAC7551 devices in a daisy-chain configuration.

For ±5-V operation: R1 = 10 kΩ, R2 = 15 kΩ, V_{tail} = 3.33 V, V_{REF} = 4.096 V

For ±10-V operation: R1 = 10 kΩ, R2 = 39 kΩ, V_{tail} = 2.56 V, V_{REF} = 4.096 V

For ±12-V operation: R1 = 10 kΩ, R2 = 49 kΩ, V_{tail} = 2.45 V, V_{REF} = 4.096 V

PRODUCT PREVIEW

PACKAGE OPTION ADDENDUM

30-Mar-2005

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DAC7551IDRNR	PREVIEW	SON	DRN	12	250	TBD	Call TI	Call TI
DAC7551IDRNT	PREVIEW	SON	DRN	12	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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