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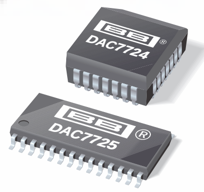


DAC7724
DAC7725

For most current data sheet and other product information, visit www.burr-brown.com

12-Bit Quad Voltage Output DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW POWER: 250mW max
- SINGLE SUPPLY OUTPUT RANGE: +10V
- DUAL SUPPLY OUTPUT RANGE: ±10V
- SETTLING TIME: 10µs to 0.012%
- 12-BIT LINEARITY AND MONOTONICITY: –40°C to +85°C
- RESET TO MID-SCALE (DAC7724) OR ZERO-SCALE (DAC7725)
- DATA READBACK
- DOUBLE-BUFFERED DATA INPUTS

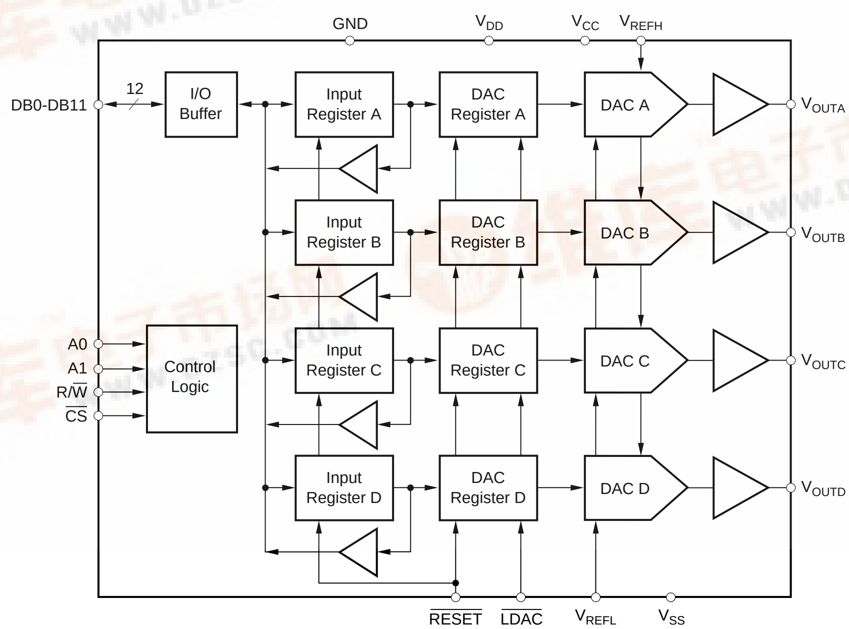
APPLICATIONS

- PROCESS CONTROL
- CLOSED-LOOP SERVO-CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS

DESCRIPTION

The DAC7724 and DAC7725 are 12-bit quad voltage output digital-to-analog converters with guaranteed 12-bit monotonic performance over the specified temperature range. They accept 12-bit parallel input data, have double-buffered DAC input logic (allowing simultaneous update of all DACs), and provide a readback mode of the internal input registers. An asynchronous reset clears all registers to a mid-scale code of 800_H (DAC7724) or to a zero-scale of 000_H (DAC7725). The DAC7724 and DAC7725 can operate from a single +15V supply, or from +15V and –15V supplies.

Low power and small size per DAC make the DAC7724 and DAC7725 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The DAC7724 and DAC7725 are available in a PLCC-28 or a SO-28 package, and offer guaranteed specifications over the –40°C to +85°C temperature range.



SPECIFICATION (DUAL SUPPLY)

At T_A = –40°C to +85°C, V_{CC} = +15V, V_{DD} = +5V, V_{SS} = –15V, V_{REFH} = +10V, V_{REFL} = –10V, unless otherwise noted.

		DAC7724N, U DAC7725N, U			DAC7724NB, UB DAC7725NB, UB			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
ACCURACY								
Linearity Error				±2			±1	LSB(1)
Linearity Matching(2)				±2			±1	LSB
Differential Linearity Error				±1			±1	LSB
Monotonicity	T_{MIN} to T_{MAX}	12			*			Bits
Zero-Scale Error	Code = 000_H			±2			*	LSB
Zero-Scale Drift			1			*		ppm/°C
Zero-Scale Matching(2)				±2			±1	LSB
Full-Scale Error	Code = FFF_H			±2			*	LSB
Full-Scale Matching(2)				±2			±1	LSB
Power Supply Sensitivity	At Full Scale		10			*		ppm/V
ANALOG OUTPUT								
Voltage Output(3)		V_{REFL}		V_{REFH}	*		*	V
Output Current		±5			*		*	mA
Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			±20			*		mA
Short-Circuit Duration	To V_{SS}, V_{CC}, or GND		Indefinite			*		
REFERENCE INPUT								
V_{REFH} Input Range		V_{REFL} +1.25		+10	*		*	V
V_{REFL} Input Range		–10		V_{REFH} – 1.25	*		*	V
Ref High Input Current		–0.5		3.0	*		*	mA
Ref Low Input Current		–3.5		0	*		*	mA
DYNAMIC PERFORMANCE								
Settling Time	To ±0.012%, 20V Output Step		8	10		*	*	µs
Channel-to-Channel Crosstalk	Full-Scale Step		0.25			*		LSB
Digital Feedthrough			2				*	nV-s
Output Noise Voltage	f = 10kHz		65			*		$nV/\sqrt{Hz}$
DIGITAL INPUT/OUTPUT								
Logic Family		TTL-Compatible CMOS			*			
Logic Levels								
V_{IH}	I_{IH} ≤ ±10µA	2.4		V_{DD} +0.3	*		*	V
V_{IL}	I_{IL} ≤ ±10µA	–0.3		0.8	*		*	V
V_{OH}	I_{OH} = –0.8mA	3.6		V_{DD}	*		*	V
V_{OL}	I_{OL} = 1.6mA	0.0		0.4	*		*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENTS								
V_{DD}		+4.75		+5.25	*		*	V
V_{CC}		+14.25		+15.75	*		*	V
V_{SS}		–14.25		–15.75	*		*	V
I_{DD}			50			*	*	µA
I_{CC}			6	8.5		*	*	mA
I_{SS}		–8	–6		*	*		mA
Power Dissipation			180	250		*	*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

NOTES: (1) LSB means Least Significant Bit, when V_{REFH} equals +10V and V_{REFL} equals –10V, then one LSB equals 4.88mV. (2) All DAC outputs will match within the specified error band. (3) Ideal output voltage, does not take into account zero or full-scale error.

SPECIFICATION (SINGLE SUPPLY)

At T_A = –40°C to +85°C, V_{CC} = +15V, V_{DD} = +5V, V_{SS} = GND, V_{REFH} = +10V, V_{REFL} = 0V, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7724N, U / DAC7725N, U MIN	TYP	MAX	DAC7724NB, UB / DAC7725NB, UB MIN	TYP	MAX	UNITS
ACCURACY								
Linearity Error(1)				±2			±1	LSB(2)
Linearity Matching(3)				±2			±1	LSB
Differential Linearity Error				±1			±1	LSB
Monotonicity	T_{MIN} to T_{MAX}	12			*			Bits
Zero-Scale Error	Code = 004_H			±4			*	LSB
Zero-Scale Drift			2			*		ppm/°C
Zero-Scale Matching(3)				±4			±2	LSB
Full-Scale Error	Code = FFF_H			±4			*	LSB
Full-Scale Matching(3)				±4			±2	LSB
Power Supply Sensitivity	At Full Scale		20			*		ppm/V
ANALOG OUTPUT								
Voltage Output(4)		V_{REFL}		V_{REFH}	*		*	V
Output Current		±5			*			mA
Load Capacitance	No Oscillation		500			*		pF
Short-Circuit Current			±20			*		mA
Short-Circuit Duration	To V_{CC} or GND		Indefinite			*		
REFERENCE INPUT								
V_{REFH} Input Range		V_{REFL} +1.25		+10	*		*	V
V_{REFL} Input Range		0		V_{REFH} – 1.25	*		*	V
Ref High Input Current		–0.3		1.5	*		*	mA
Ref Low Input Current		–2.0		0	*		*	mA
DYNAMIC PERFORMANCE								
Settling Time(5)	To ±0.012%, 10V Output Step		8	10		*	*	µs
Channel-to-Channel Crosstalk			0.25			*		LSB
Digital Feedthrough			2				*	nV-s
Output Noise Voltage	f = 10kHz		65			*		nV/√Hz
DIGITAL INPUT/OUTPUT								
Logic Family			TTL-Compatible CMOS		*			
Logic Levels								
V_{IH}	$I_{IH} \le \pm 10\mu A$	2.4		V_{DD} +0.3	*		*	V
V_{IL}	$I_{IL} \le \pm 10\mu A$	–0.3		0.8	*		*	V
V_{OH}	I_{OH} = –0.8mA	3.6		V_{DD}	*		*	V
V_{OL}	I_{OL} = 1.6mA	0.0		0.4	*		*	V
Data Format			Straight Binary			*		
POWER SUPPLY REQUIREMENTS								
V_{DD}		+4.75		+5.25	*		*	V
V_{CC}		14.25		15.75	*		*	V
I_{DD}			50			*	*	µA
I_{CC}			3.0			*	*	mA
Power Dissipation			45			*		mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

NOTES: (1) If V_{SS} = 0V, specification applies at code 004_H and above. (2) LSB means Least Significant Bit, when V_{REFH} equals +10V and V_{REFL} equals 0V, then one LSB equals 2.44mV. (3) All DAC outputs will match within the specified error band. (4) Ideal output voltage, does not take into account zero or full-scale error. (5) Full-scale positive 10V step and negative step from code FFF_H to 004_H.

ABSOLUTE MAXIMUM RATINGS[1]

V_{CC} to V_{SS}	–0.3V to +32V
V_{CC} to GND	–0.3V to +16V
V_{SS} to GND	+0.3V to –16V
V_{DD} to GND	–0.3V to 6V
V_{REF}H to GND	–9V to +11V
V_{REF}L to GND (V_{SS} = –15V)	–11V to +9V
V_{REF}L to GND (V_{SS} = 0V)	–0.3V to +9V
V_{REFH} to V_{REFL}	–1V to +22V
Digital Input Voltage to GND	–0.3V to V_{DD} + 0.3V
Digital Output Voltage to GND	–0.3V to V_{DD} + 0.3V
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

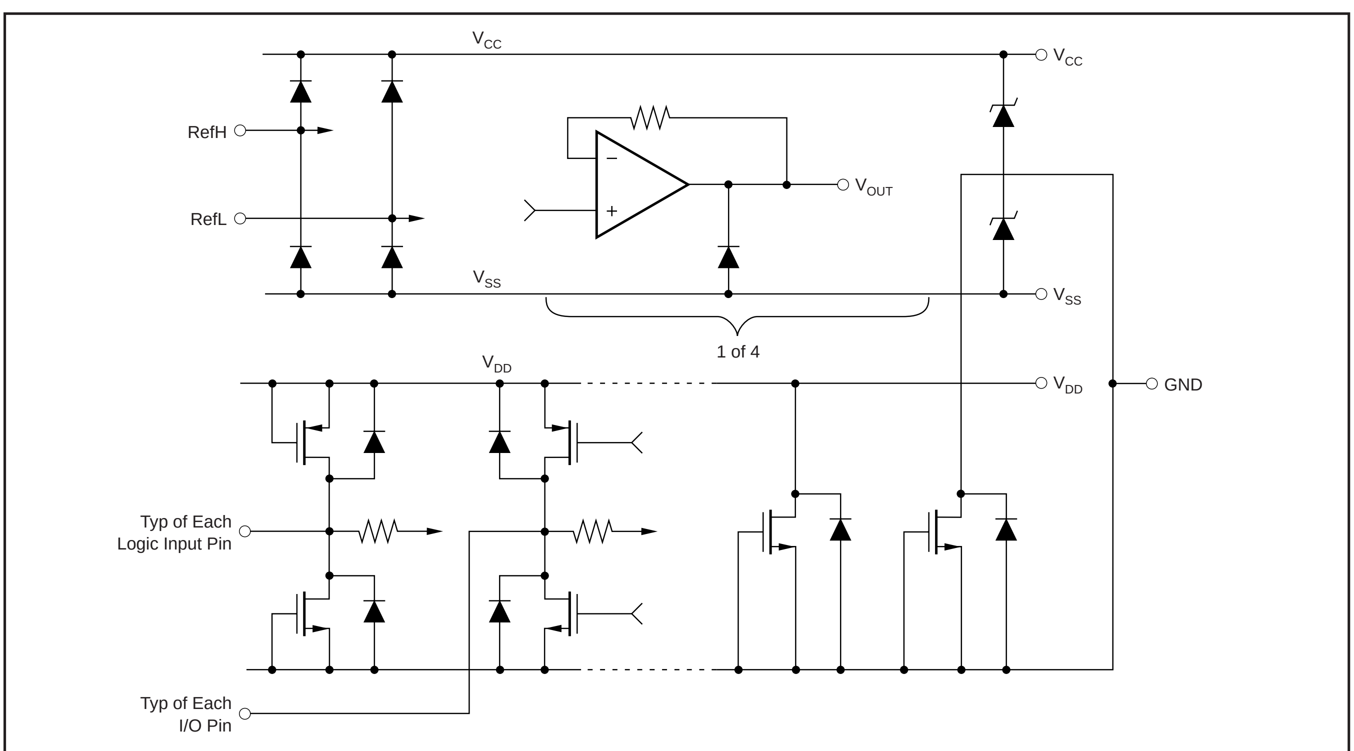
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	MAXIMUM DIFFERENTIAL NONLINEARITY ERROR (LSB)	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFICATION TEMPERATURE RANGE	ORDERING NUMBER[1]	TRANSPORT MEDIA
DAC7724N	±2	±1	PLCC-28	251	–40°C to +85°C	DAC7724N	Rails
"	"	"	"	"	"	DAC7724N/750	Tape and Reel
DAC7724NB	±1	±1	PLCC-28	251	–40°C to +85°C	DAC7724NB	Rails
"	"	"	"	"	"	DAC7724NB/750	Tape and Reel
DAC7724U	±2	±1	SO-28	217	–40°C to +85°C	DAC7724U	Rails
"	"	"	"	"	"	DAC7724U/1K	Tape and Reel
DAC7724UB	±1	±1	SO-28	217	–40°C to +85°C	DAC7724UB	Rails
"	"	"	"	"	"	DAC7724UB/1K	Tape and Reel
DAC7725N	±2	±1	PLCC-28	251	–40°C to +85°C	DAC7725N	Rails
"	"	"	"	"	"	DAC7725N/750	Tape and Reel
DAC7725NB	±1	±1	PLCC-28	251	–40°C to +85°C	DAC7725NB	Rails
"	"	"	"	"	"	DAC7725NB/750	Tape and Reel
DAC7725U	±2	±1	SO-28	217	–40°C to +85°C	DAC7725U	Rails
"	"	"	"	"	"	DAC7725U/1K	Tape and Reel
DAC7725UB	±1	±1	SO-28	217	–40°C to +85°C	DAC7725UB	Rails
"	"	"	"	"	"	DAC7725UB/1K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /750 indicates 750 devices per reel). Ordering 750 pieces of "DAC7724/750" will get a single 750-piece Tape and Reel.

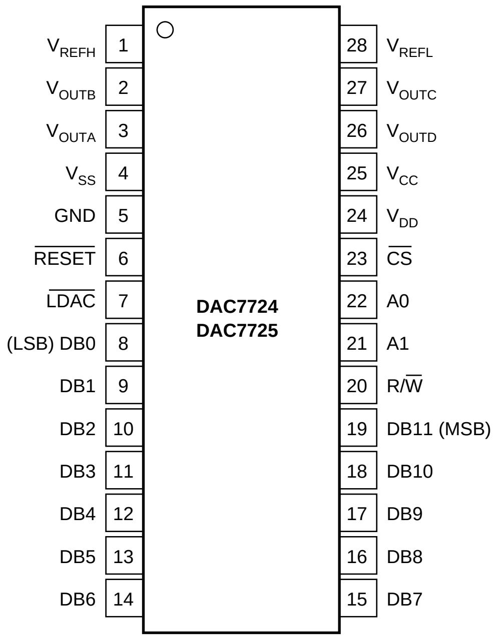
ESD PROTECTION CIRCUITS



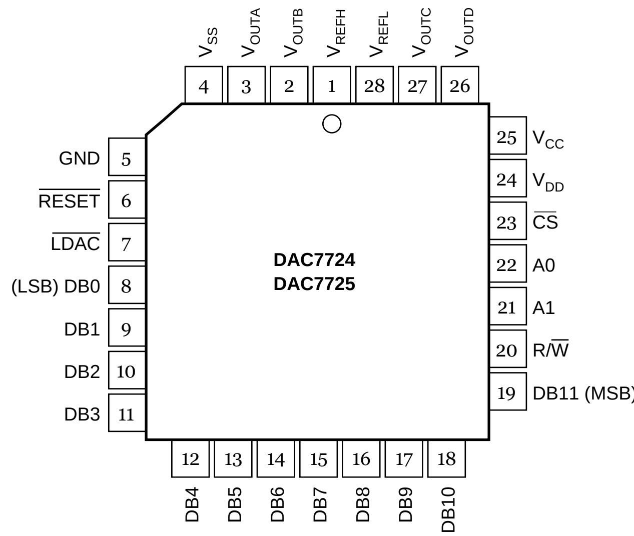
PIN CONFIGURATIONS

Top View

SO



PLCC



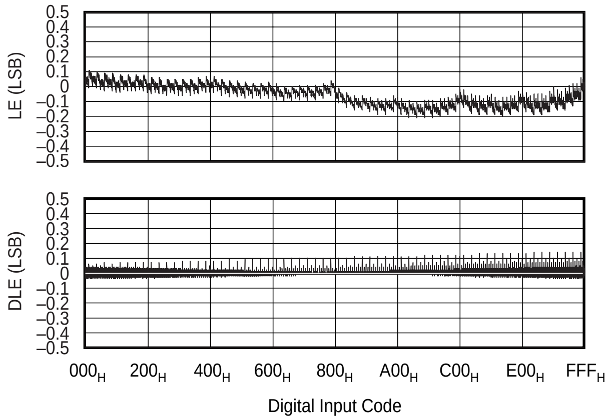
PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	V_{REFH}	Reference Input Voltage High. Sets maximum output voltage for all DACs.
2	V_{OUTB}	DAC B Voltage Output.
3	V_{OUTA}	DAC A Voltage Output.
4	V_{SS}	Negative Analog Supply Voltage, 0V or –15V.
5	GND	Ground.
6	$\overline{RESET}$	Asynchronous Reset Input. Sets DAC and input registers to either mid-scale (800_H, DAC7724) or zero-scale (000_H, DAC7725) when LOW.
7	$\overline{LDAC}$	Load DAC Input. All DAC Registers are transparent when LOW.
8	DB0	Data Bit 0. Least significant bit of 12-bit word.
9	DB1	Data Bit 1
10	DB2	Data Bit 2
11	DB3	Data Bit 3
12	DB4	Data Bit 4
13	DB5	Data Bit 5
14	DB6	Data Bit 6
15	DB7	Data Bit 7
16	DB8	Data Bit 8
17	DB9	Data Bit 9
18	DB10	Data Bit 10
19	DB11	Data Bit 11. Most significant bit of 12-bit word.
20	R/$\overline{W}$	Read/Write Control Input (read = HIGH, write = LOW).
21	A1	Register/DAC Select (C or D = HIGH, A or B = LOW).
22	A0	Register/DAC Select (B or D = HIGH, A or C = LOW).
23	$\overline{CS}$	Chip Select Input.
24	V_{DD}	Positive Digital Supply, +5V.
25	V_{CC}	Positive Analog Supply Voltage, +15V nominal.
26	V_{OUTD}	DAC D Voltage Output.
27	V_{OUTC}	DAC C Voltage Output.
28	V_{REFL}	Reference Input Voltage Low. Sets minimum output voltage for all DACs.

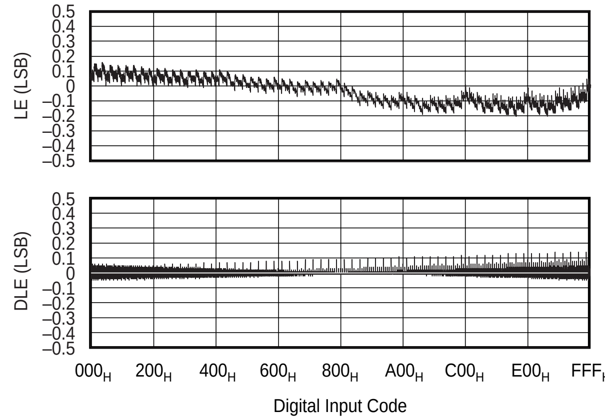
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V

At T_A = +25°C, V_{CC} = +15V, V_{DD} = +5V, V_{SS} = 0V, V_{REFH} = +10V, V_{REFL} = 0V, representative unit, unless otherwise specified.

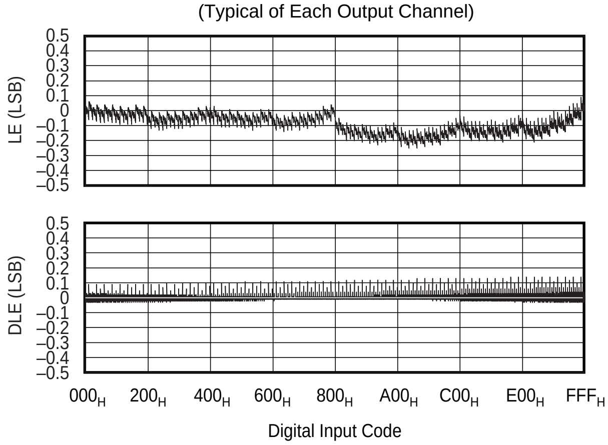
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel 25°C
(Typical of Each Output Channel)



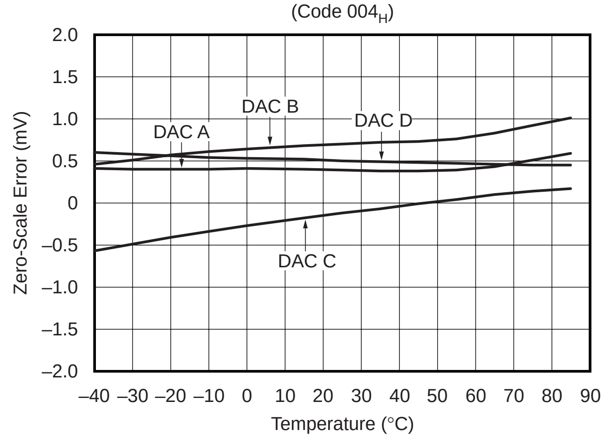
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel 85°C
(Typical of Each Output Channel)



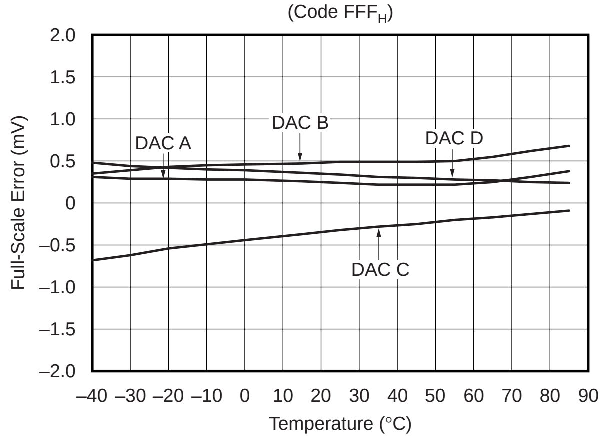
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel –40°C
(Typical of Each Output Channel)



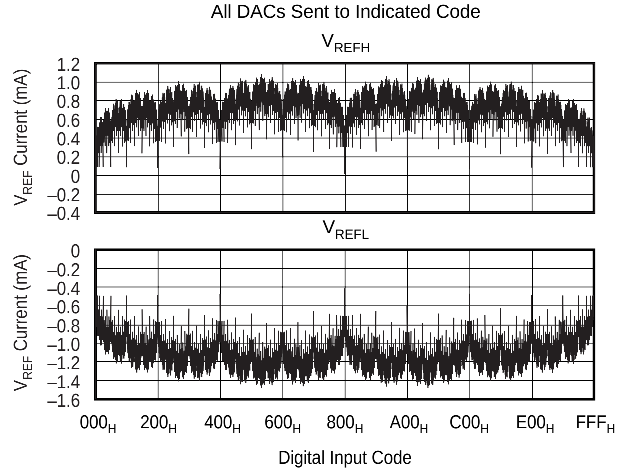
ZERO-SCALE ERROR vs TEMPERATURE
(Code 004_H)



FULL-SCALE ERROR vs TEMPERATURE
(Code FFF_H)

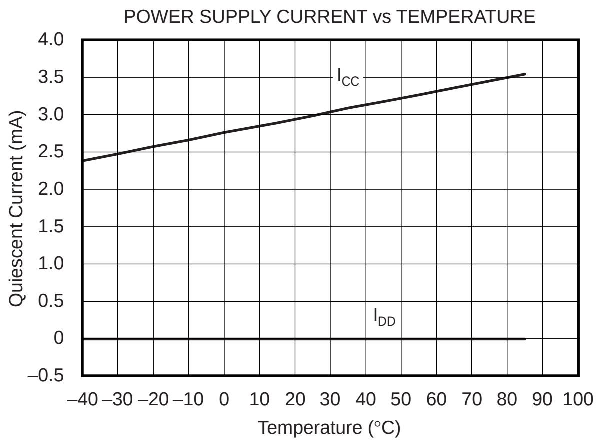


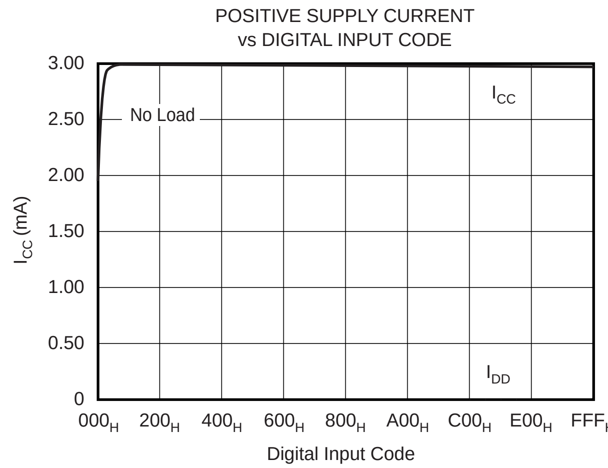
CURRENT vs CODE
All DACs Sent to Indicated Code

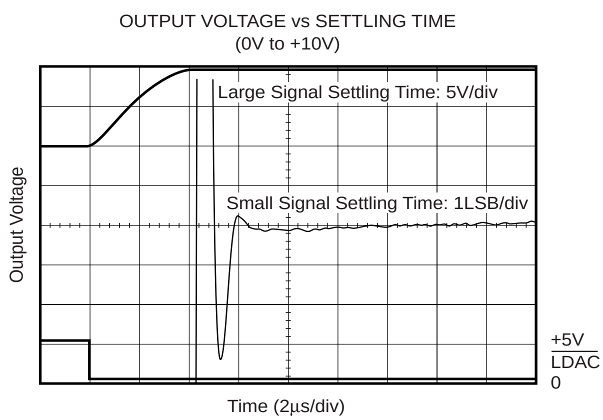


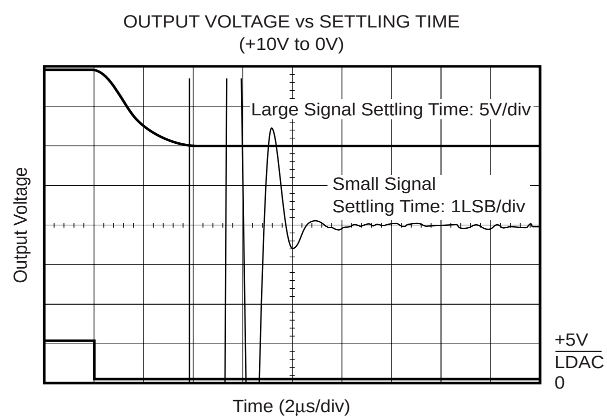
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (Cont.)

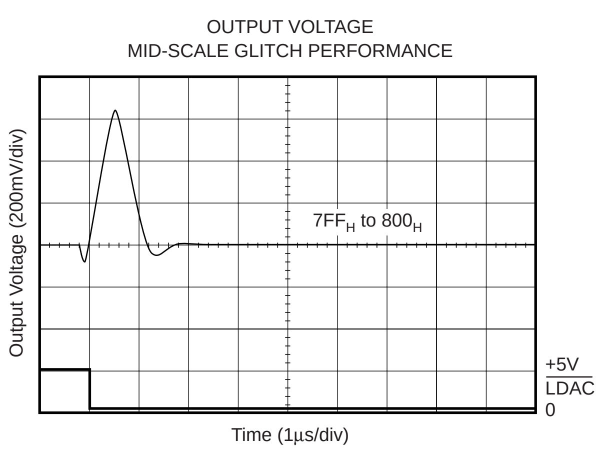
At T_A = +25°C, V_{CC} = +15V, V_{DD} = +5V, V_{SS} = 0V, V_{REFH} = +10V, V_{REFL} = 0V, representative unit, unless otherwise specified.

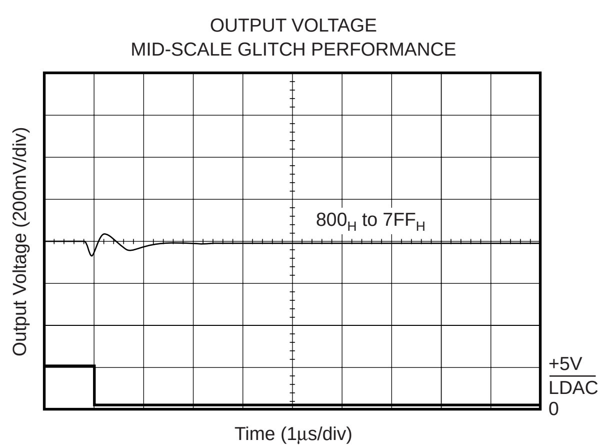








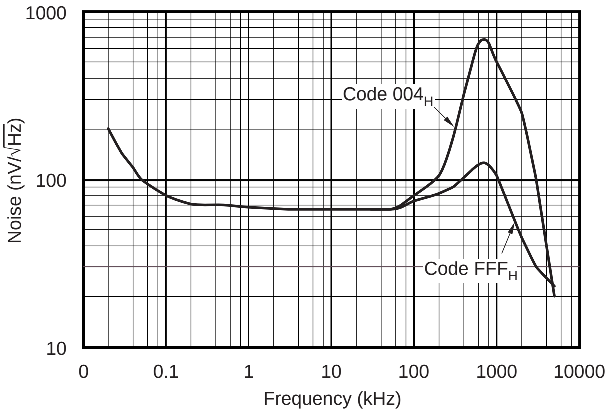




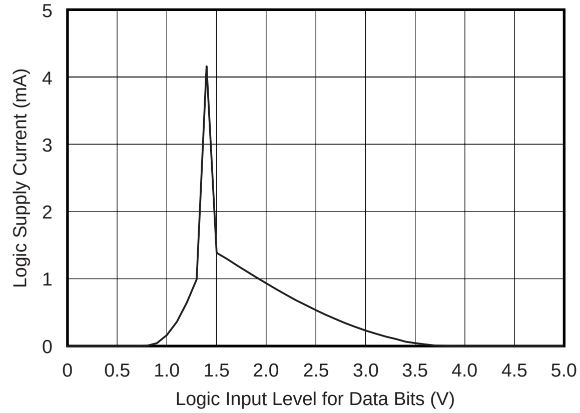
TYPICAL PERFORMANCE CURVES: V_{SS} = 0V (Cont.)

At T_A = +25°C, V_{CC} = +15V, V_{DD} = +5V, V_{SS} = 0V, V_{REFH} = +10V, V_{REFL} = 0V, representative unit, unless otherwise specified.

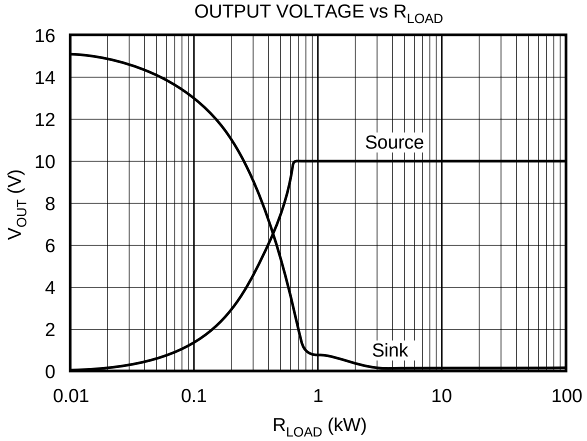
OUTPUT NOISE vs FREQUENCY



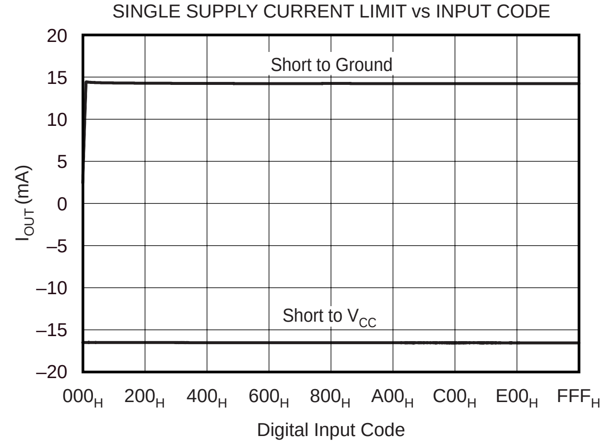
LOGIC SUPPLY CURRENT vs LOGIC INPUT LEVEL FOR DATA BITS



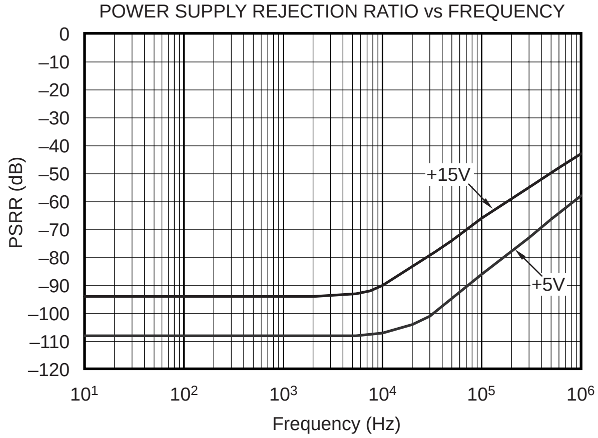
OUTPUT VOLTAGE vs R_{LOAD}



SINGLE SUPPLY CURRENT LIMIT vs INPUT CODE



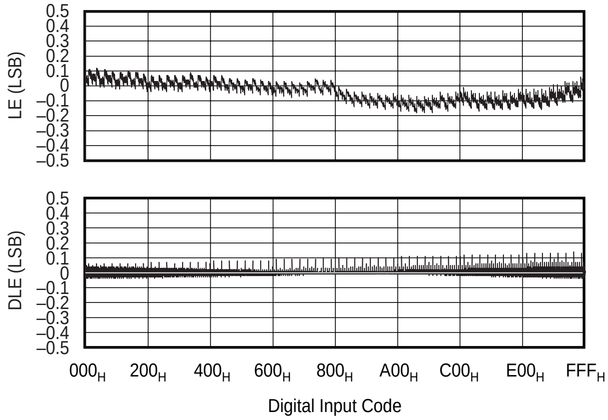
POWER SUPPLY REJECTION RATIO vs FREQUENCY



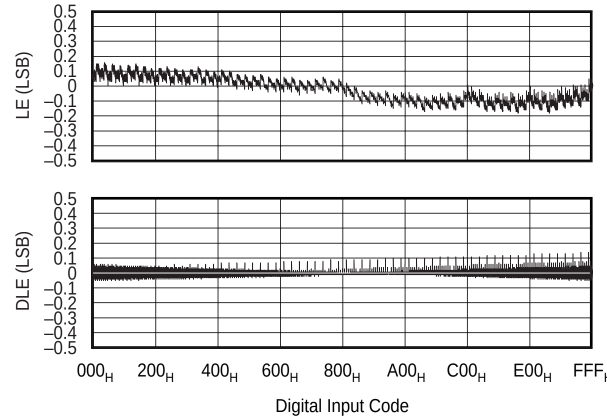
TYPICAL PERFORMANCE CURVES: V_{SS} = –15V

At T_A = +25°C, V_{CC} = +15V, V_{DD} = +5V, V_{SS} = –15V, V_{REFH} = +10V, V_{REFL} = –10V, representative unit, unless otherwise specified.

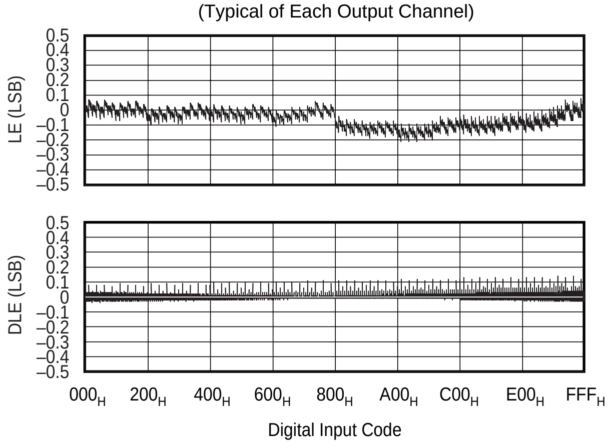
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel 25°C
(Typical of Each Output Channel)



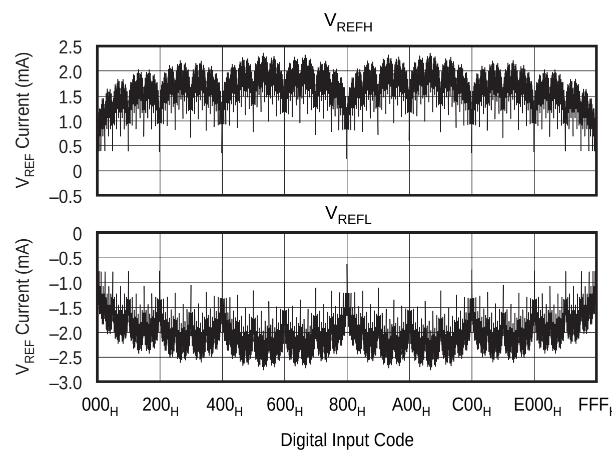
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel 85°C
(Typical of Each Output Channel)



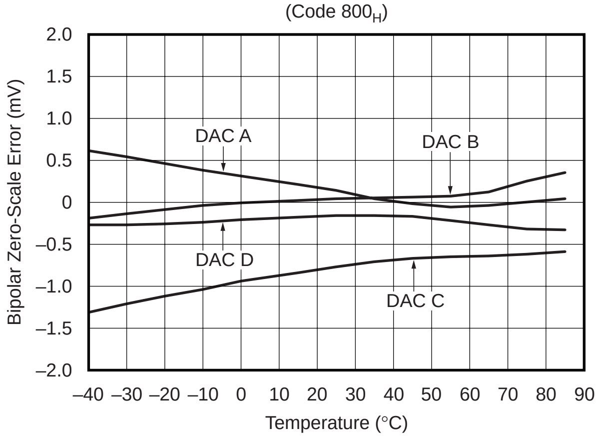
LINEARITY ERROR AND
DIFFERENTIAL LINEARITY ERROR vs CODE
Single Channel –40°C
(Typical of Each Output Channel)



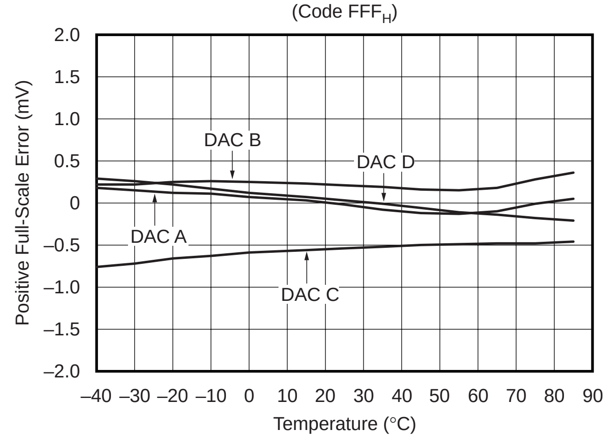
CURRENT vs CODE
All DACs Sent to Indicated Code



BIPOLAR ZERO-SCALE ERROR vs TEMPERATURE
(Code 800_H)



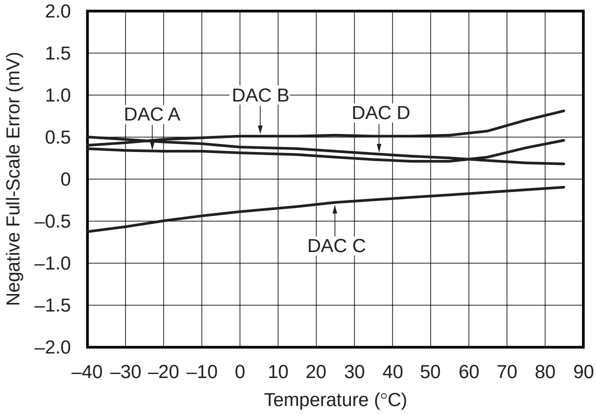
POSITIVE FULL-SCALE ERROR vs TEMPERATURE
(Code FFF_H)



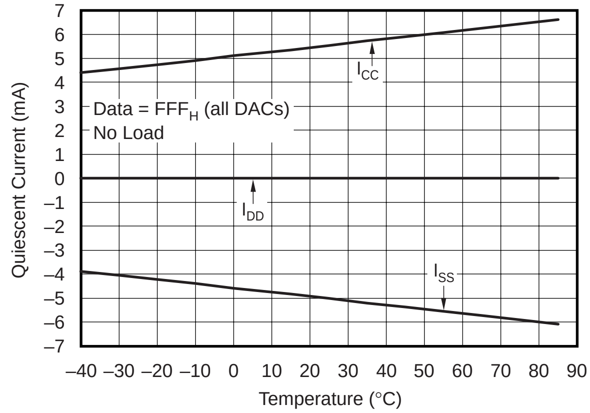
TYPICAL PERFORMANCE CURVES: V_{SS} = –15V (Cont.)

At T_A = +25°C, V_{CC} = +15V, V_{DD} = +5V, V_{SS} = –15V, V_{REFH} = +10V, V_{REFL} = –10V, representative unit, unless otherwise specified.

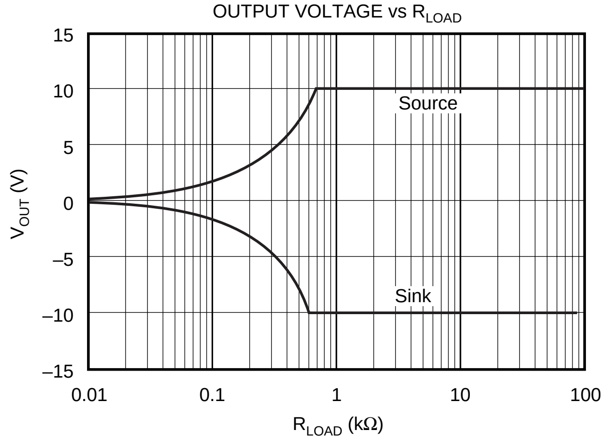
NEGATIVE FULL-SCALE ERROR vs TEMPERATURE
(Code 000_H)



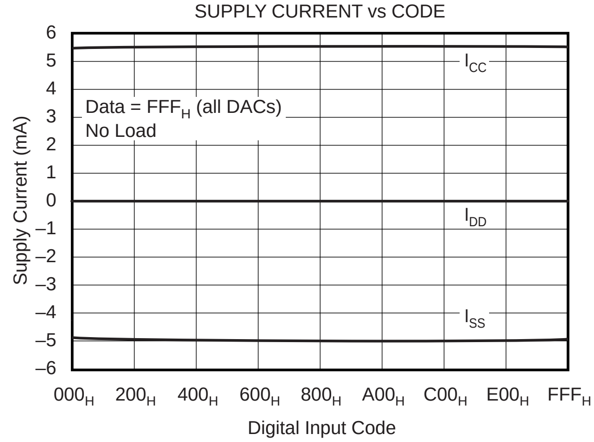
POWER SUPPLY CURRENT vs TEMPERATURE



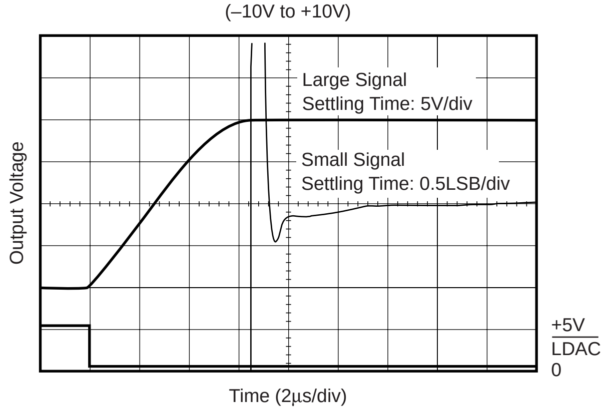
OUTPUT VOLTAGE vs R_{LOAD}



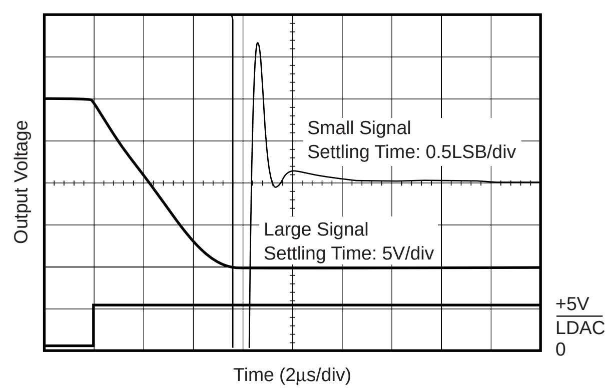
SUPPLY CURRENT vs CODE



OUTPUT VOLTAGE vs SETTLING TIME
(–10V to +10V)



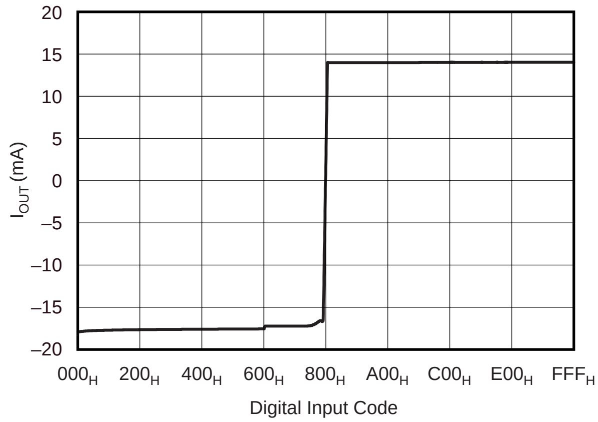
OUTPUT VOLTAGE vs SETTLING TIME
(+10V to –10V)



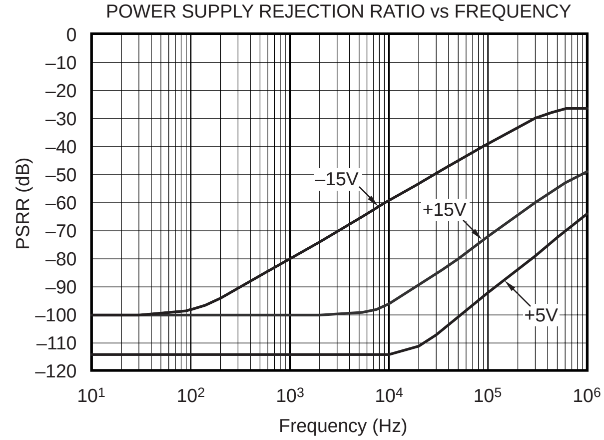
TYPICAL PERFORMANCE CURVES: V_{SS} = –15V (Cont.)

At T_A = +25°C, V_{CC} = +15V, V_{DD} = +5V, V_{SS} = –15V, V_{REFH} = +10V, V_{REFL} = –10V, representative unit, unless otherwise specified.

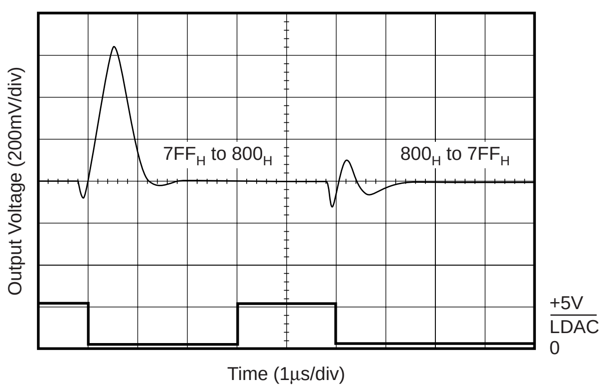
DUAL SUPPLY CURRENT LIMIT vs INPUT CODE
SHORT TO GROUND



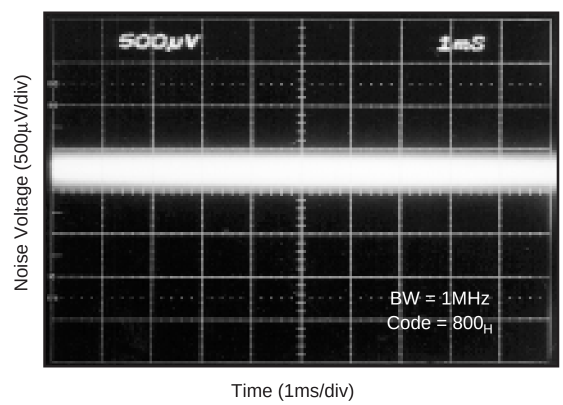
POWER SUPPLY REJECTION RATIO vs FREQUENCY



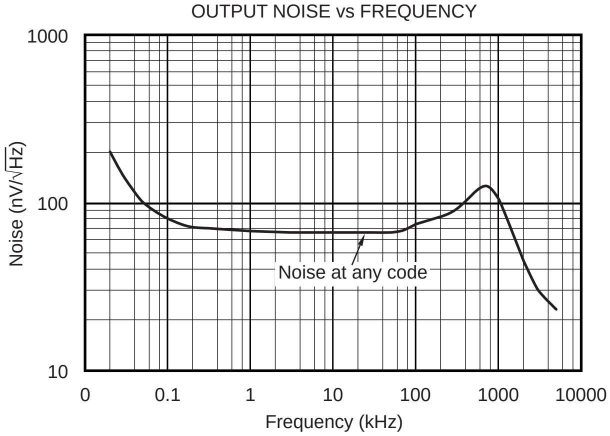
OUTPUT VOLTAGE
MID-SCALE GLITCH PERFORMANCE



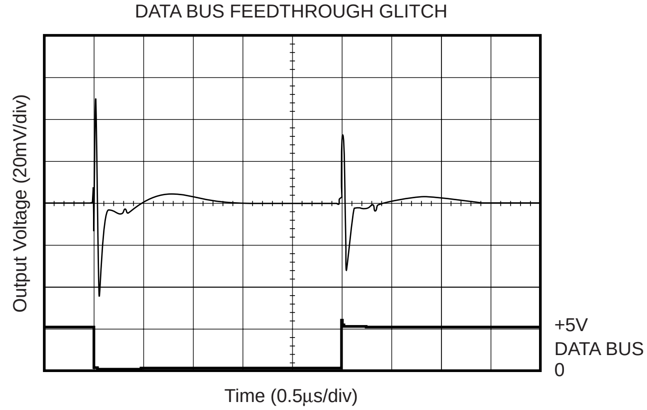
BROADBAND NOISE



OUTPUT NOISE vs FREQUENCY



DATA BUS FEEDTHROUGH GLITCH



THEORY OF OPERATION

The DAC7724 and DAC7725 are quad voltage output, 12-bit digital-to-analog converters (DACs). The architecture is a classic R-2R ladder configuration followed by an operational amplifier that serves as a buffer, as shown in Figure 1. Each DAC has its own R-2R ladder network and output op-amp, but all share the reference voltage inputs. The minimum voltage output ("zero-scale") and maximum voltage output ("full-scale") are set by the external voltage references (V_{REFL} and V_{REFH}, respectively). The digital input is a 12-bit parallel word and the DAC input registers offer a readback capability. The converters can be powered from a single +15V supply or a dual ±15V supply. Each device offers a reset function which immediately sets all DAC registers and DAC output voltages to mid-scale (DAC7724, code 800_H) or to zero-scale (DAC7725, code 000_H). See Figures 2 and 3 for the basic operation of the DAC7724/25.

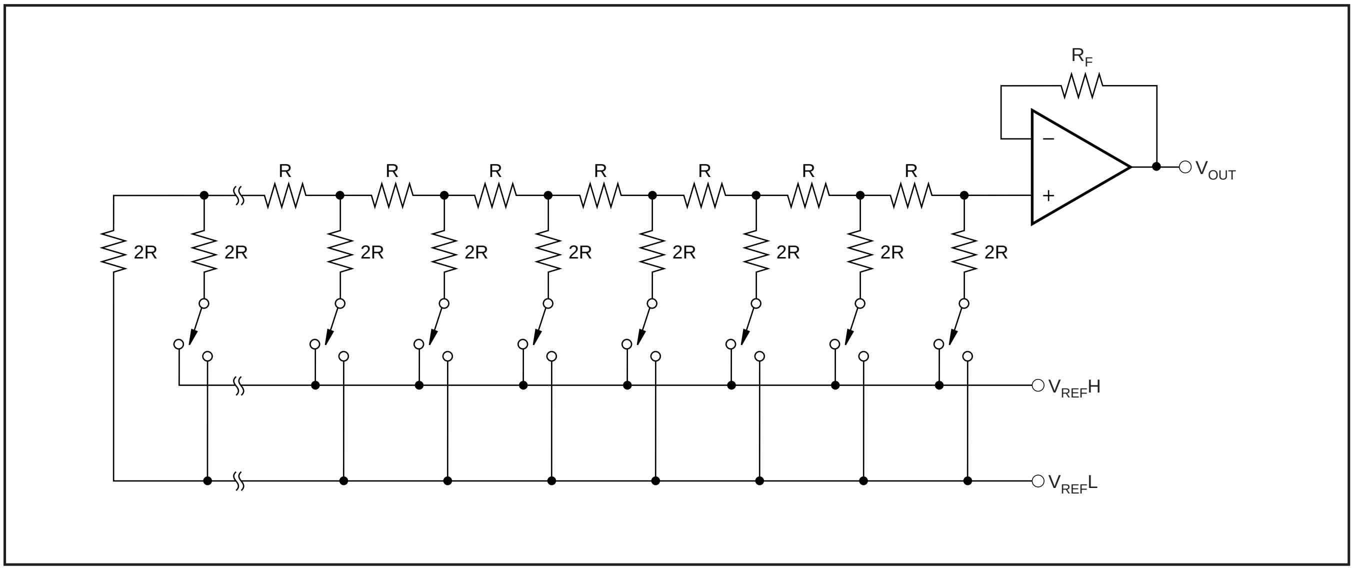


FIGURE 1. DAC7724/25 Architecture.

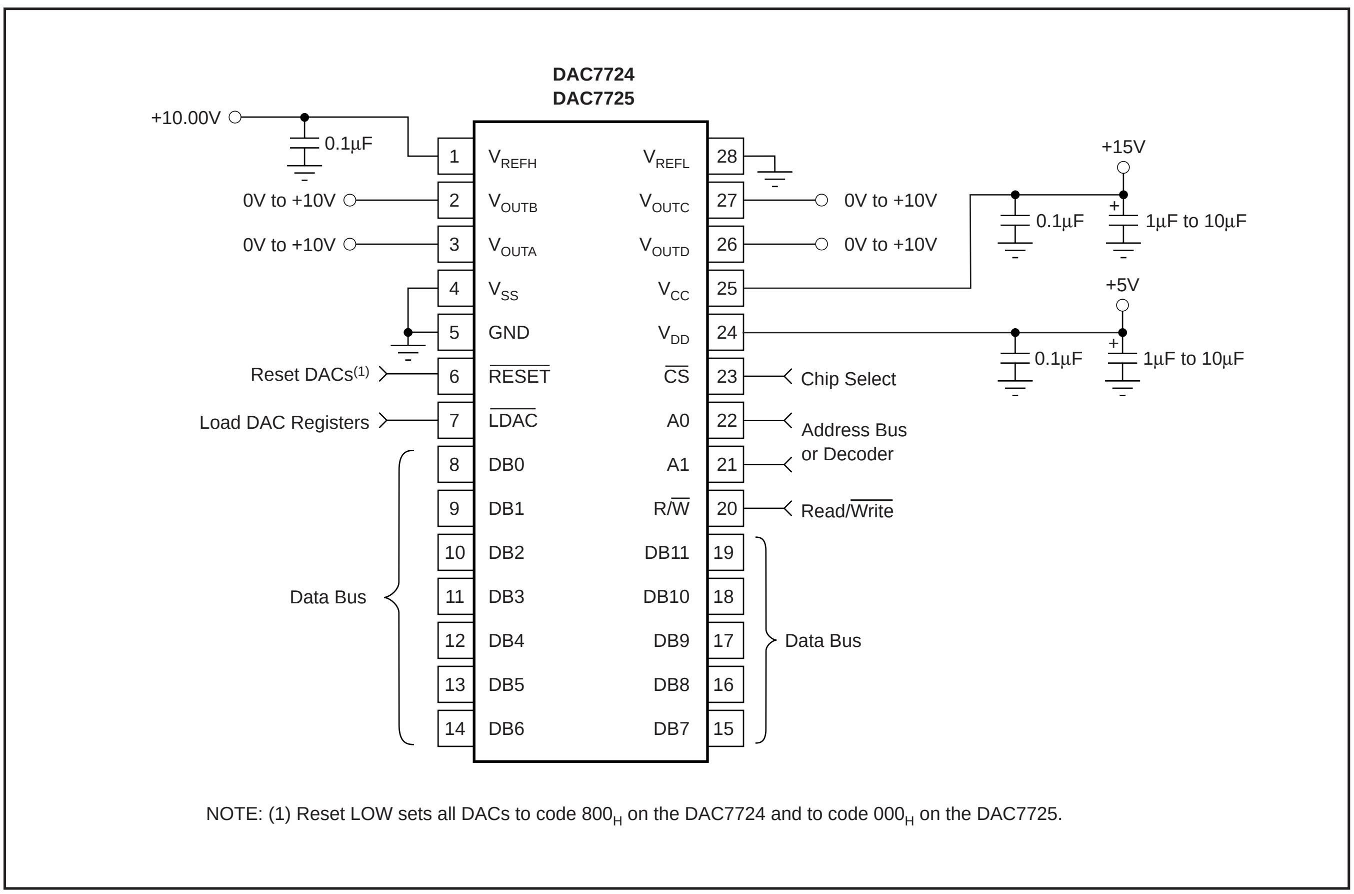


FIGURE 2. Basic Single-Supply Operation of the DAC7724/25.

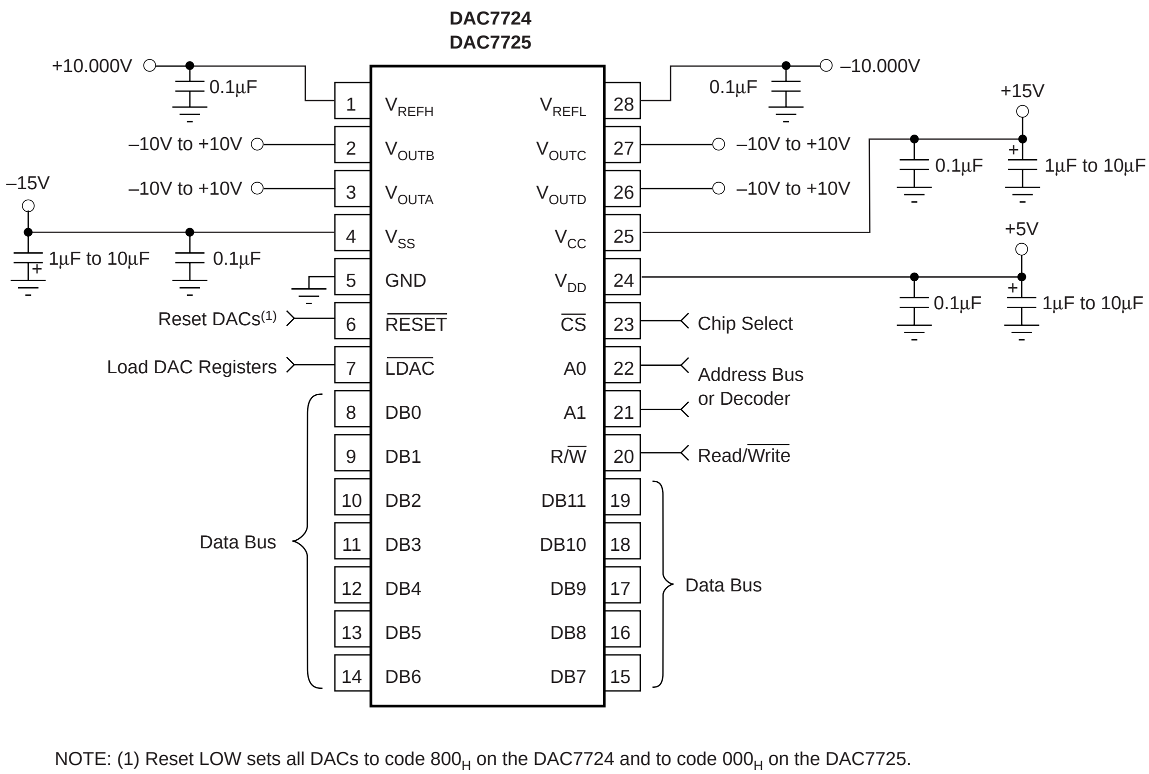


FIGURE 3. Basic Dual-Supply Operation of the DAC7724/25.

ANALOG OUTPUTS

When V_{SS} = –15V (dual supply operation), the output amplifier can swing to within 4V of the supply rails, guaranteed over the –40°C to +85°C temperature range. With V_{SS} = 0V (single-supply operation) and R_{LOAD} connected to ground, the output can swing to ground. Note that the settling time of the output op-amp will be longer with voltages very near ground. Additionally, care must be taken when measuring the zero-scale error when V_{SS} = 0V. Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (000_H, 001_H, 002_H, etc.) if the output amplifier has a negative offset. At the negative offset limit of –4 LSB (-9.76mV), for the single-supply case, the first specified output starts at code 004_H.

REFERENCE INPUTS

For dual-supply operation, the reference inputs, V_{REFL} and V_{REFH}, can be any voltage between V_{SS} + 4V and V_{CC} – 4V provided that V_{REFH} is at least 1.25V greater than V_{REFL}. For single-supply operation (V_{SS} = 0V), V_{REFL} value can be above 0V, with the same provision that V_{REFH} is at least 1.25V greater than V_{REFL}. The minimum output of each DAC is equal to V_{REFL} plus a small offset voltage (essentially, the offset of the output op-amp). The maximum output is equal to V_{REFH} plus a similar offset voltage. Note that V_{SS} (the negative power supply) must either be connected to ground or must be in the range of –14.25V to –15.75V. The voltage on V_{SS} sets several bias points within the converter, if V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not guaranteed.

The current into the V_{REF}H input and out of V_{REF}L depends on the DAC output voltages and can vary from a few microamps to approximately 0.3mA. The reference input appears as a varying load to the reference. If the reference can sink or source the required current, a reference buffer is not required. See "Reference Current vs Code" in the Typical Performance Curves.

The analog supplies (or the analog supplies and the reference power supplies) have to come up first. If the power supplies for the references come up first, then the V_{CC} and V_{SS} supplies will be "powered from the reference via the ESD protection diodes" (see page 4).

Bypassing the reference voltage or voltages with at least a 0.1uF capacitor placed as close to the DAC7724/25 package is strongly recommended.

DIGITAL INTERFACE

Table I shows the basic control logic for the DAC7724/25. Note that each internal register is level triggered and not edge triggered. When the appropriate signal is LOW, the register becomes transparent. When this signal is returned HIGH, the digital word currently in the register is latched. The first set of registers (the Input Registers) are triggered via the A0, A1, R/$\overline{\text{W}}$, and $\overline{\text{CS}}$ inputs. Only one of these registers is transparent at any given time. The second set of registers (the DAC Registers) are all transparent when $\overline{\text{LDAC}}$ input is pulled LOW.

Each DAC can be updated independently by writing to the appropriate Input Register and then updating the DAC Register. Alternatively, the entire DAC Register set can be configured as always transparent by keeping $\overline{\text{LDAC}}$ LOW—the DAC update will occur when the Input Register is written.

The double buffered architecture is mainly designed so that each DAC Input Register can be written at any time and then all DAC output voltages updated simultaneously by pulling $\overline{\text{LDAC}}$ LOW. It also allows a DAC Input Register to be written to at any point and the DAC voltage to be synchronously changed via a trigger signal connected to $\overline{\text{LDAC}}$.

DIGITAL TIMING

Figure 4 and Table II provide detailed timing for the digital interface of the DAC7724 and DAC7725.

DIGITAL INPUT CODING

The DAC7724 and DAC7725 input data is in straight binary format. The output voltage is given by the following equation:

$$V_{OUT} = V_{REFL} + \frac{\left(V_{REFH} - V_{REFL}\right) \cdot N}{4096}$$

where N is the digital input code. This equation does not include the effects of offset (zero-scale) errors.

A1	A0	R/$\overline{\text{W}}$	$\overline{\text{CS}}$	$\overline{\text{RESET}}$	$\overline{\text{LDAC}}$	SELECTED INPUT REGISTER	STATE OF SELECTED INPUT REGISTER	STATE OF ALL DAC REGISTERS
L(1)	L	L	L	H(2)	L	A	Transparent	Transparent
L	H	L	L	H	L	B	Transparent	Transparent
H	L	L	L	H	L	C	Transparent	Transparent
H	H	L	L	H	L	D	Transparent	Transparent
L	L	L	L	H	H	A	Transparent	Latched
L	H	L	L	H	H	B	Transparent	Latched
H	L	L	L	H	H	C	Transparent	Latched
H	H	L	L	H	H	D	Transparent	Latched
L	L	H	L	H	H	A	Readback	Latched
L	H	H	L	H	H	B	Readback	Latched
H	L	H	L	H	H	C	Readback	Latched
H	H	H	L	H	H	D	Readback	Latched
X(3)	X	X	H	H	L	NONE	(All Latched)	Transparent
X	X	X	H	H	H	NONE	(All Latched)	Latched
X	X	X	X	L	X	ALL	Reset(4)	Reset(4)

NOTES: (1) L = Logic LOW. (2) H= Logic HIGH. (3) X = Don't Care. (4) DAC7724 resets to 800_H, DAC7725 resets to 000_H. When $\overline{\text{RESET}}$ rises, all registers that are in their latched state retain the reset value.

TABLE I. DAC7724 and DAC7725 Control Logic Truth Table.

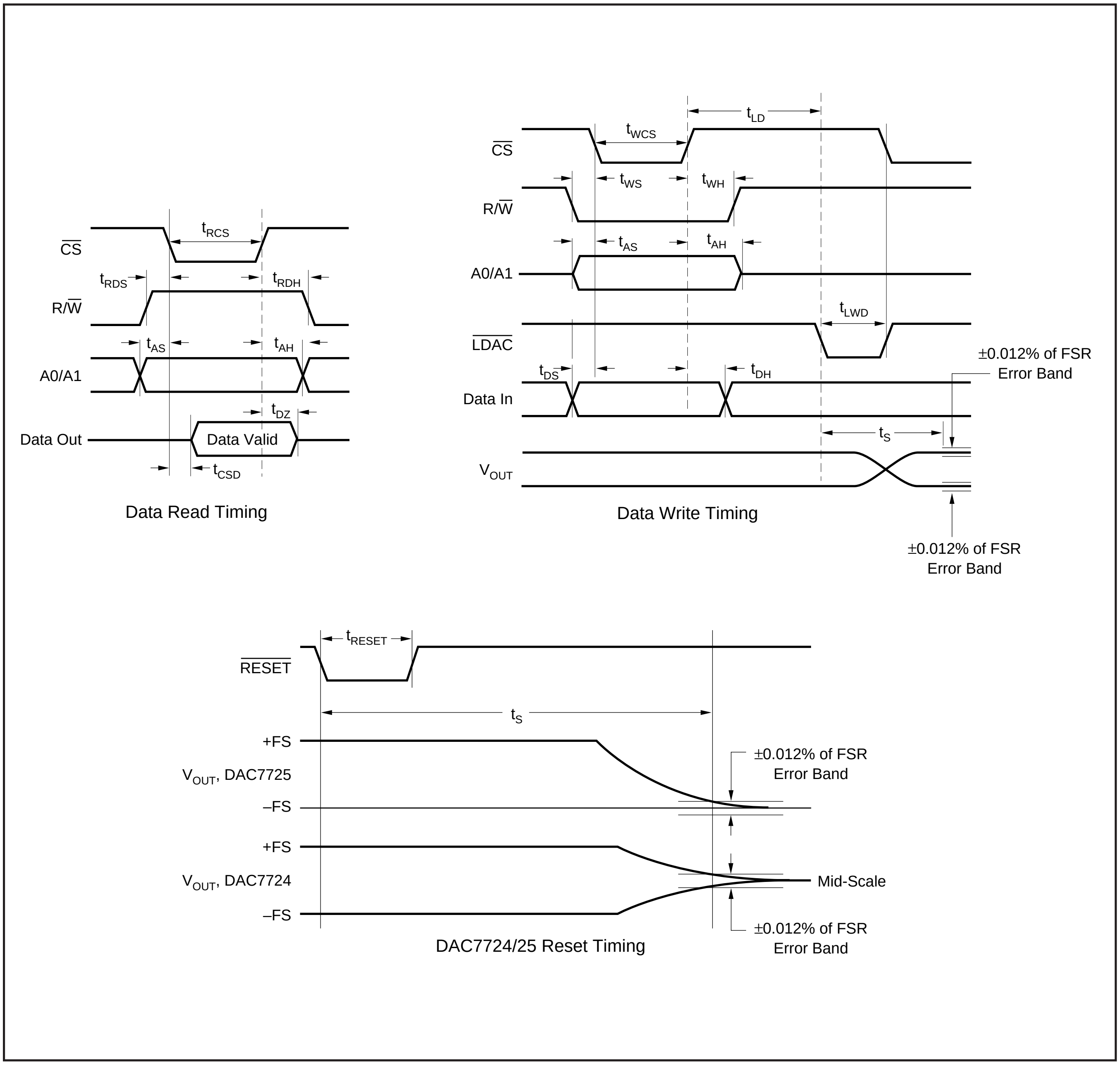


FIGURE 4. Digital Input and Output Timing.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{RCS}	$\overline{CS}$ LOW for Read	200			ns
t_{RDS}	R/$\overline{W}$ HIGH to $\overline{CS}$ LOW	10			ns
t_{RDH}	R/$\overline{W}$ HIGH after $\overline{CS}$ HIGH	10			ns
t_{DZ}	$\overline{CS}$ HIGH to Data Bus in High Impedance		100		ns
t_{CSD}	$\overline{CS}$ LOW to Data Bus Valid		100	160	ns
t_{WCS}	$\overline{CS}$ LOW for Write	50			ns
t_{WS}	R/$\overline{W}$ LOW to $\overline{CS}$ LOW	0			ns
t_{WH}	R/$\overline{W}$ LOW after $\overline{CS}$ HIGH	0			ns
t_{AS}	Address Valid to $\overline{CS}$ LOW	0			ns
t_{AH}	Address Valid after $\overline{CS}$ HIGH	0			ns
t_{LD}	$\overline{LDAC}$ Delay from $\overline{CS}$ HIGH	10			ns
t_{DS}	Data Valid to $\overline{CS}$ LOW	0			ns
t_{DH}	Data Valid after $\overline{CS}$ HIGH	0			ns
t_{LWD}	$\overline{LDAC}$ LOW	50			ns
t_{RESET}	RESET LOW Time	50			ns
t_S	Settling Time			10	µs

TABLE II. Timing Specifications (T_A = –40°C to +85°C).