QUAD, 16-BIT, RAIL-TO-RAIL VOLTAGE OUTPUT, PARALLEL INTERFACE, DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **Single Supply: +2.7 V to +5.5 V**
- **Micropower Operation: 950 µA @ 5 V**
- **Rail-To-Rail Voltage Output**
- **Ultralow Crosstalk: –110 dB**
- **Settling Time: 10 µs To ±0.003% FSR**
- **16-Bit Monotonic**
- **Offset Error: ±0.3 mV**
- **Gain Error: ±1 mV**
- **Total Error: ±3 mV**
- **Per-Channel V_{REF+}, $V_{REF–}$, V_{FB} Pins**
- **Logic Compatible: +1.8 V to +5.5 V**
- **Readback Capability**
- **Double Buffered Inputs**
- **Simultaneous or Sequential Update**
- **Schmitt-Triggered Digital Inputs**
- **Hardware Reset**
- **48-Lead TQFP Package**

APPLICATIONS

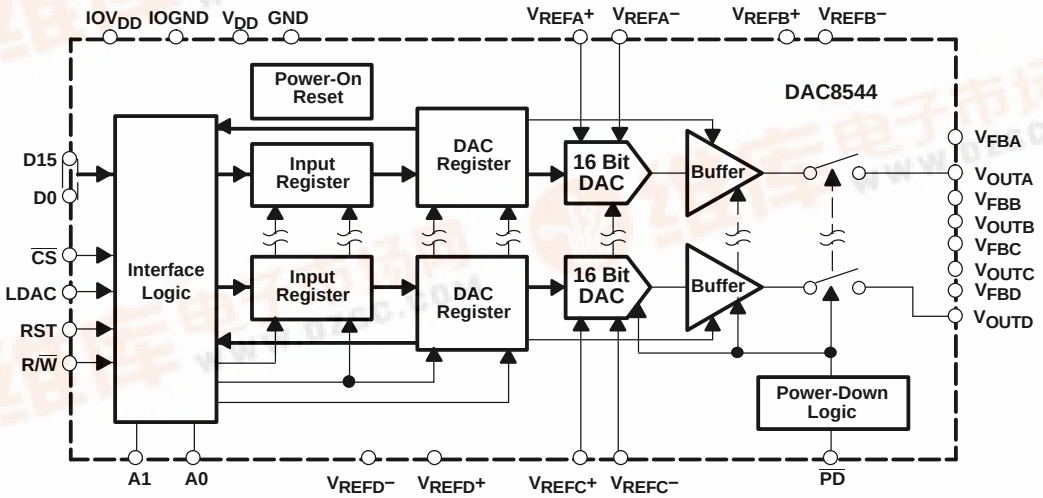
- **Process Control**
- **Data Acquisition Systems**
- **Closed-Loop Servo Control**
- **PC Peripherals**
- **Optical Networking**

DESCRIPTION

The DAC8544 is a low-power, quad-channel, 16-bit, voltage output DAC. Its on-chip precision output amplifier allows rail-to-rail voltage swing to be achieved at the output. The DAC8544 is 16-bit monotonic and offers exceptional absolute accuracy with ultralow crosstalk. The DAC8544 uses a 16-bit parallel interface and features additional power-down function pins as well as hardware-enabled, synchronous DAC updating and reset capability.

The DAC8544 requires an external reference voltage to set the output range of the DAC. The device incorporates a power-on-reset circuit that ensures that the DAC outputs power up at zero volt and remains there until a valid write takes place. In addition, the DAC8544 contains a power-down feature, accessed via $\overline{PD}$ pin, that reduces the current consumption of the device to 400 nA at 5 V. The power consumption is typically under 5 mW at V_{DD} = 5 V.

The DAC8544 is available in a 48-lead TQFP package with an operating temperature range of –40°C to +105°C.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	TA	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
DAC8544	48 - TQFP	PFB	-40°C to 105°C	DAC8544I	DAC8544IPFB	Tray
					DAC8544IPFBR	Tape and Reel

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

V_{DD} to GND	–0.3 V to 6 V
IOV_{DD} to IOGND	–0.3 V to 6 V
Digital input voltage to IOGND	–0.3 V to IOV_{DD} + 0.3 V
V_{OUT} to GND	–0.3 V to V_{DD} + 0.3 V
Operating temperature range	–40°C to 105°C
Storage temperature range, Tstg	–65°C to 150°C
Junction temperature, TJ max	+150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

V_{DD} = + 2.7 V to + 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications –40°C to +105°C unless otherwise noted

		DAC8544			
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
STATIC PERFORMANCE(1)					
Resolution		16			Bits
Relative Accuracy			±0.025	±.098	%FSR
Differential Nonlinearity	16-Bit Monotonic		±0.25	±1	LSB
Zero-Code Offset Error	Measured at code 485, 25°C		0.3	±3	mV
	Measured at code 485, -40°C to 105°C		1.0	±5.0	
Zero-Code Error Drift	All zeroes loaded to DAC register		-20		µV/°C
DC Crosstalk			0.1		LSB
AC Crosstalk	1-kHz sine wave		-110		dB
Gain Error	Measured at code 64714, 25°C		1.0	±3.0	mV
	Measured at code 64714, -40°C to 105°C		2.0	±5.0	
Gain Error Drift			-5		ppm of FSR/°C
Full-Scale Error	Measured at code 64714, 25°C		0.5	±3.0	mV
	Measured at code 64714, -40°C to 105°C		1.0	±5.0	
OUTPUT CHARACTERISTICS(2)					
Output Voltage Range		0		V_{REF}	V
Output Voltage Settling Time	R_L = 2 kΩ; C_L <200 pF		8	10	µs
	R_L = 2 kΩ; C_L <500 pF		12		
Slew Rate	R_L = 2 kΩ; C_L <200 pF		1		V/µs

(1) Linearity calculated using a reduced code range of 485 to 64714. Output unloaded.
(2) Assured by design and characterization, not production tested.

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = + 2.7 V to + 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications –40°C to +105°C unless otherwise noted

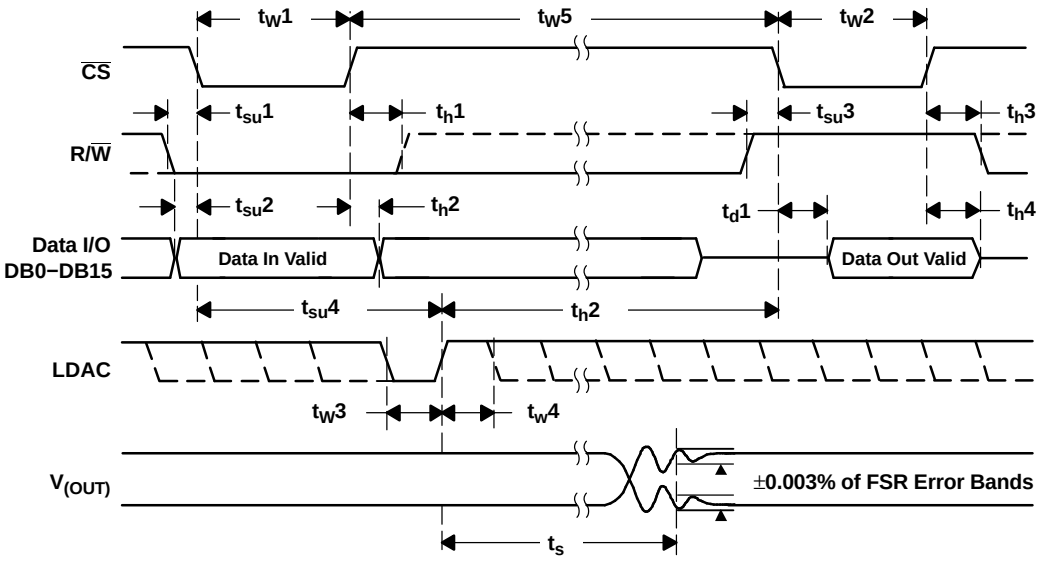
		DAC8544			
PARAMETER	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Capacitive Load Stability	$R_L = \infty$		470		pF
	R_L = 2 kΩ		1000		pF
Digital-to-Analog Glitch Impulse			20		nV-s
Digital Feedthrough			0.5		nV-s
DC Output Impedance			1		Ω
Short-Circuit Current	V_{DD} = +5 V		50		mA
	V_{DD} = +3 V		20		
Power-Up Time	Coming out of power-down mode, V_{DD} = +5 V		2.5		µs
	Coming out of power-down mode, V_{DD} = +3 V		5		
REFERENCE INPUT					
V_{REF+} Input Range		0		V_{DD}	V
$V_{REF–}$ Input Range		–0.1	0.0	$V_{DD}/2$	V
Reference Input Impedance			140		kΩ
LOGIC INPUTS					
Input Current				±1	µA
$V_{IN}L$, Input Low Voltage	IOV_{DD} = +1.8 V – +5.5 V			0.3 x IOV_{DD}	V
$V_{IN}H$, Input High Voltage	IOV_{DD} = +1.8 V – +5.5 V	0.7 x IOV_{DD}			V
Pin Capacitance				3	pF
POWER REQUIREMENTS					
V_{DD}		2.7		5.5	V
IOV_{DD}		1.8		5.5	V
I_{DD} (Normal Mode)	DAC active and excluding load current				
V_{DD} = +3.6 V to +5.5 V	$VI_H = IOV_{DD}$ and VI_L = IOGND		1.0	1.6	mA
V_{DD} = +2.7 V to +3.6 V	$VI_H = IOV_{DD}$ and VI_L = IOGND		0.96	1.52	
I_{DD} (All Power-Down Modes)					
V_{DD} = +3.6 V to +5.5 V	$VI_H = IOV_{DD}$ and VI_L = IOGND		0.2	1	µA
V_{DD} = +2.7 V to +3.6 V	$VI_H = IOV_{DD}$ and VI_L = IOGND		0.05	1	
POWER EFFICIENCY					
I_{OUT}/I_{DD}	I_{LOAD} = 2 mA, V_{DD} = +5 V		93		%

TIMING CHARACTERISTICS

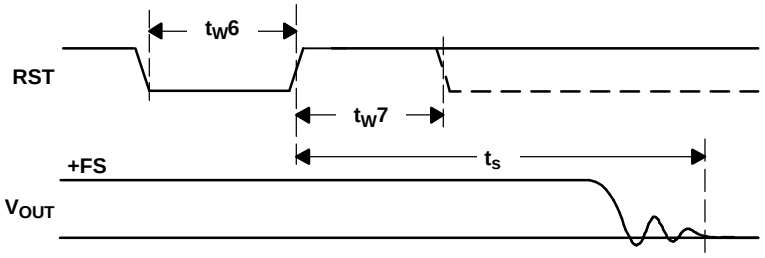
IOV_{DD} = 1.8 V to 5.5 V; V_{DD} = 2.7 V to 5.5 V; R_L = 2 kΩ to GND; C_L = 200 pF to GND; all specifications –40°C to 85°C (unless otherwise noted)

		MIN	TYP	MAX	UNIT
t_w1	Pulse width: $\overline{CS}$ low for valid write	20			ns
$t_{su}1$	Setup time: R/$\overline{W}$ low before $\overline{CS}$ falling	0			ns
$t_{su}2$	Setup time: data in valid before $\overline{CS}$ falling	0			ns
t_h1	Hold time: R/$\overline{W}$ low after $\overline{CS}$ rising	10			ns
t_h2	Hold time: data in valid after $\overline{CS}$ rising	15			ns
t_w2	Pulse width: $\overline{CS}$ low for valid read	40			ns
$t_{su}3$	Setup time: R/$\overline{W}$ high before $\overline{CS}$ falling	30			ns
t_d1	Delay time: data out valid after $\overline{CS}$ falling		60	80	ns
t_h3	Hold time: R/$\overline{W}$ high after $\overline{CS}$ rising	10			ns
t_h4	Hold time: data out valid after $\overline{CS}$ rising	5		20	ns
$t_{su}4$	Setup time: LDAC rising after $\overline{CS}$ falling	10			ns
t_d2	Delay time: $\overline{CS}$ low after LDAC rising	50			ns
t_w3	Pulse width: LDAC low	40			ns
t_w4	Pulse width: LDAC high	40			ns
t_w5	Pulse width: $\overline{CS}$ high	80			ns
t_w6	Pulse width: RST low	40			ns
t_w7	Pulse width: RST high	40			ns
t_S	V$\overline{OUT}$ Settling time (settling time for a full-scale code change)			10	µs

Data Read/Write Timing

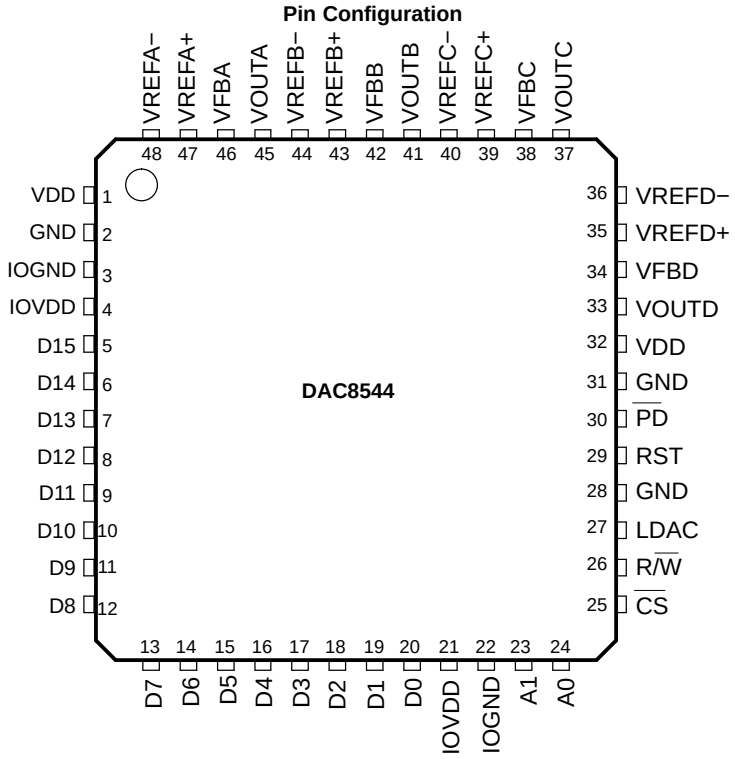


Reset Timing



DEVICE INFORMATION

Pin Configuration



DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS

DAC8544		
Pin	**Mnemonic**	**Function**
1	VDD	Analog supply voltage, +2.7 V to +5.5 V
2	GND	Analog supply ground
3	IOGND	Digital supply ground
4	IOVDD	Digital supply +1.8 V to +5.5 V
5	D15	Digital input, MSB
6	D14	Digital input
7	D13	Digital input
8	D12	Digital input
9	D11	Digital input
10	D10	Digital input
11	D9	Digital input
12	D8	Digital input
13	D7	Digital input
14	D6	Digital input
15	D5	Digital input
16	D4	Digital input
17	D3	Digital input
18	D2	Digital input
19	D1	Digital input
20	D0	Digital input, LSB
21	IOVDD	Digital supply +1.8 V to +5.5 V
22	IOGND	Digital supply ground
23	A1	Address pin for selecting between DAC channels
24	A0	Address pin for selecting between DAC channels
25	$\overline{CS}$	Active-low chip select. Used with R/$\overline{W}$_ to write/read data to/from device
26	R/$\overline{W}$	Read/Write select used to write data to input register or read data from DAC register
27	LDAC	Load DACs, rising edge triggered loads all DAC registers
28	GND	Analog ground
29	RST	Asynchronously resets contents of all DAC Registers to zero-scale, but does not affect input register
30	$\overline{PD}$	Active-low power-down pin puts entire device into power-down mode with DAC outputs in 3-state condition
31	GND	Analog supply ground
32	VDD	Analog supply voltage, +2.7 V to +5.5 V
33	VOUTD	Analog output voltage from DAC-D
34	VFBD	Analog output sense for DAC-D
35	VREFD+	High reference voltage input for DAC-D
36	VREFD–	Low reference voltage input for DAC-D, normally VREFD– = GND
37	VOUTC	Analog output voltage from DAC-C
38	VFBC	Analog output sense for DAC-C
39	VREFC+	High reference voltage input for DAC-C
40	VREFC–	Low reference voltage input for DAC-C, normally VREFC– = GND
41	VOUTB	Analog output voltage from DAC-B
42	VFBB	Analog output sense for DAC-B
43	VREFB+	High reference voltage input for DAC-B
44	VREFB–	Low reference voltage input for DAC-B, normally VREFB– = GND
45	VOUTA	Analog output voltage from DAC-A

DEVICE INFORMATION (continued)

TERMINAL FUNCTIONS (continued)

DAC8544		
Pin	**Mnemonic**	**Function**
46	VFBA	Analog output sense for DAC-A
47	VREFA+	High reference voltage input for DAC-A
48	VREFA–	Low reference voltage input for DAC-A, normally VREFA– = GND

TYPICAL CHARACTERISTICS

This condition applies to all typical characteristics: $V_{REF+} = V_{DD}$, V_{REF-} = GND, T_A = 25°C (unless otherwise noted)

TOTAL UNADJUSTED ERROR vs DIGITAL INPUT CODE

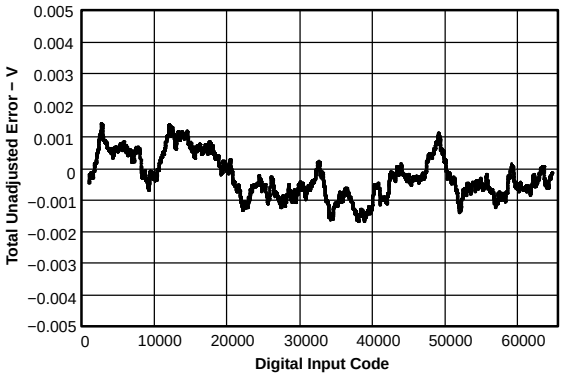


Figure 1.

ERROR vs TEMPERATURE

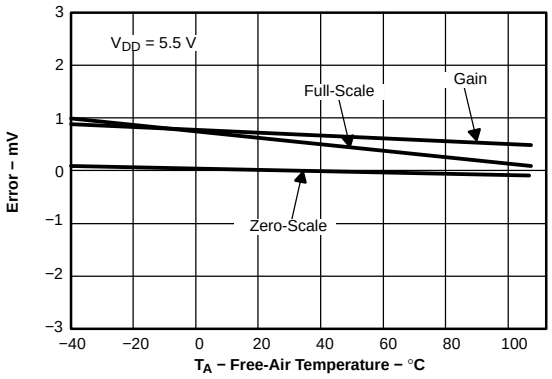


Figure 2.

ERROR vs TEMPERATURE

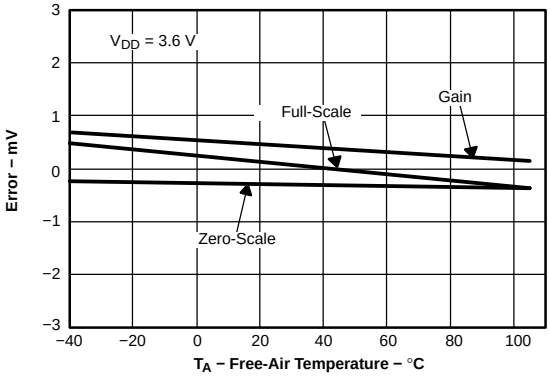


Figure 3.

OFFSET ERROR DISTRIBUTION (ACROSS MANY SAMPLES)

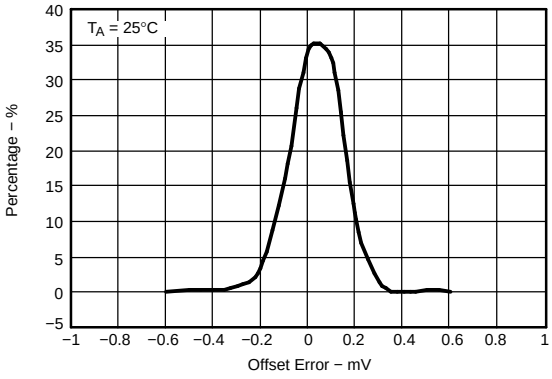


Figure 4.

GAIN ERROR DISTRIBUTION (ACROSS MANY SAMPLES)

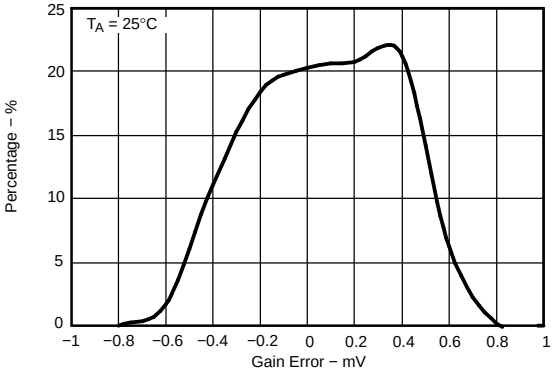


Figure 5.

FULL SCALE ERROR DISTRIBUTION (ACROSS MANY SAMPLES)

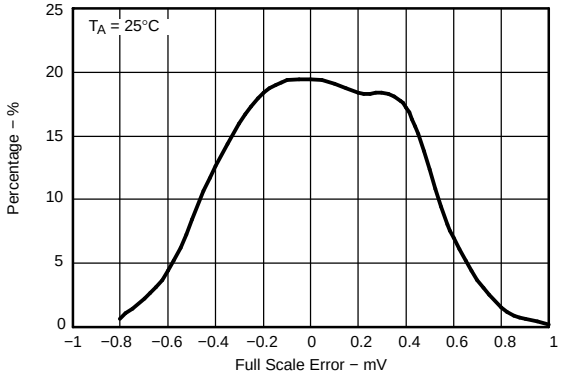


Figure 6.

TYPICAL CHARACTERISTICS (continued)

This condition applies to all typical characteristics: $V_{REF+} = V_{DD}$, V_{REF-} = GND, T_A = 25°C (unless otherwise noted)

LINEARITY ERROR vs DIGITAL INPUT CODE

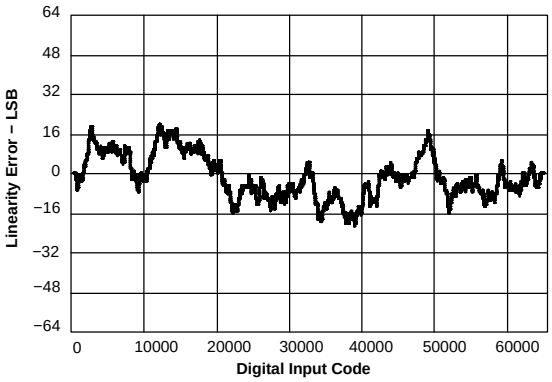


Figure 7.

DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE

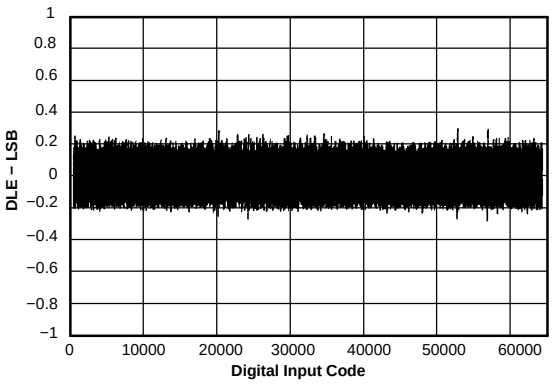


Figure 8.

LINEARITY ERROR vs TEMPERATURE

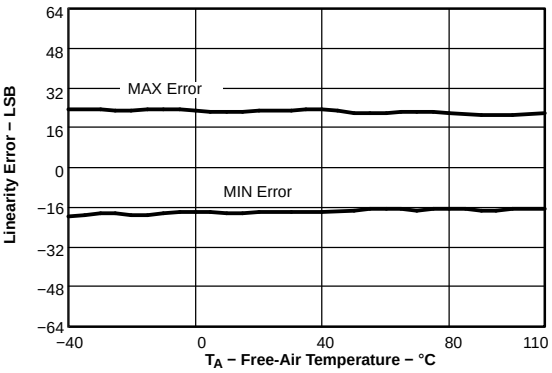


Figure 9.

DIFFERENTIAL LINEARITY ERROR vs TEMPERATURE

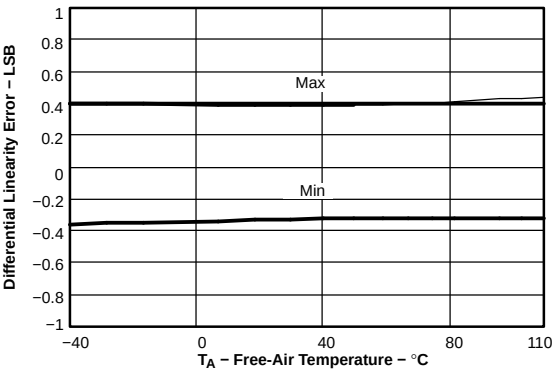


Figure 10.

SINK CURRENT AT NEGATIVE RAIL

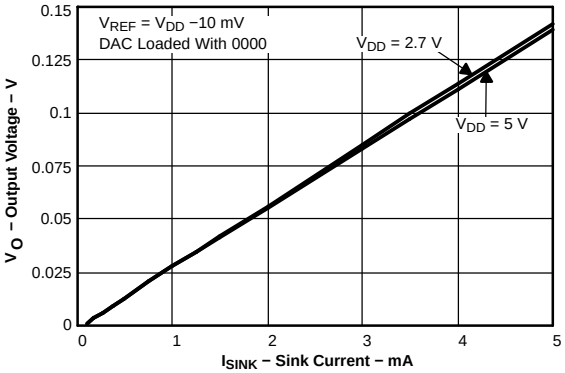


Figure 11.

SOURCE CURRENT AT POSITIVE RAIL

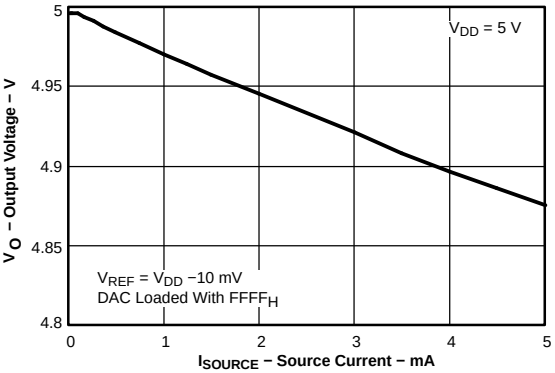


Figure 12.

TYPICAL CHARACTERISTICS (continued)

This condition applies to all typical characteristics: $V_{REF+} = V_{DD}$, V_{REF-} = GND, T_A = 25°C (unless otherwise noted)

SOURCE CURRENT AT POSITIVE RAIL

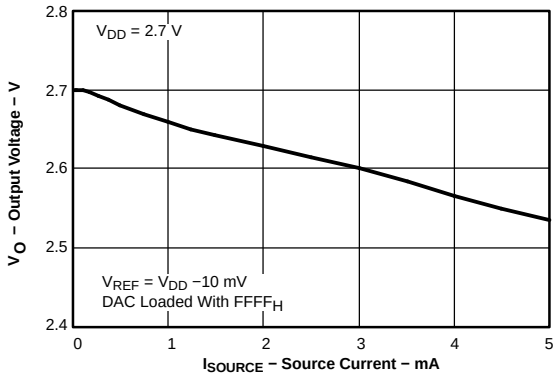


Figure 13.

SUPPLY CURRENT vs DIGITAL INPUT CODE

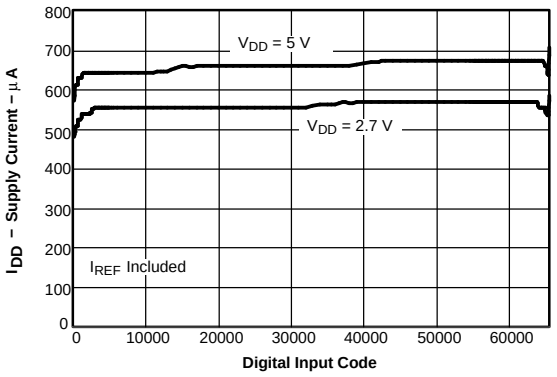


Figure 14.

SUPPLY CURRENT vs TEMPERATURE

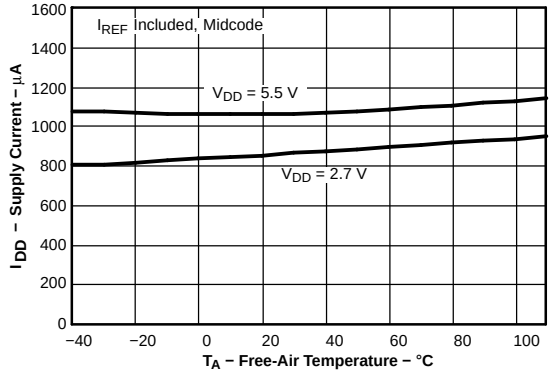


Figure 15.

SUPPLY CURRENT vs SUPPLY VOLTAGE

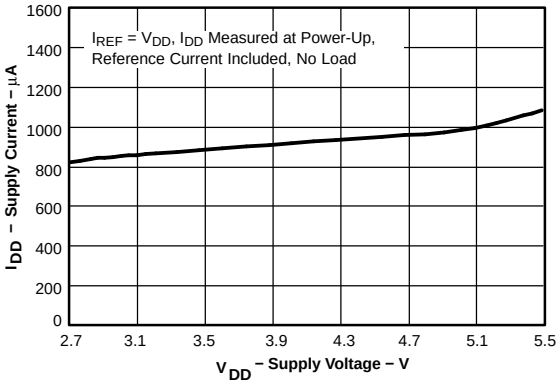


Figure 16.

SUPPLY CURRENT vs LOGIC INPUT VOLTAGE

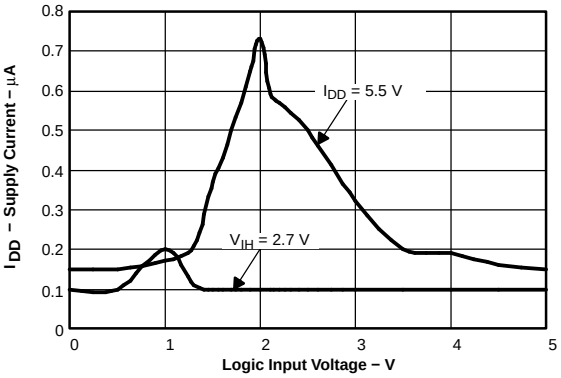


Figure 17.

HISTOGRAM OF CURRENT CONSUMPTION

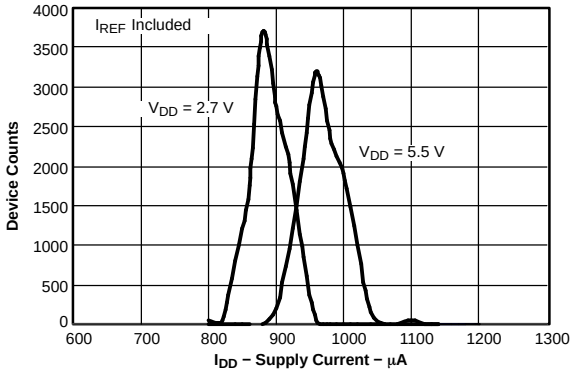


Figure 18.

TYPICAL CHARACTERISTICS (continued)

This condition applies to all typical characteristics: $V_{REF+} = V_{DD}$, V_{REF-} = GND, T_A = 25°C (unless otherwise noted)

EXITING POWER-DOWN MODE

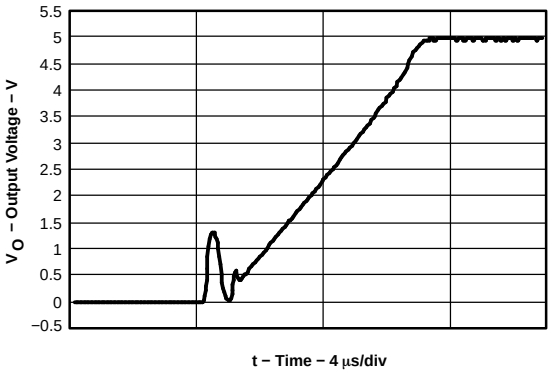


Figure 19.

OUTPUT GLITCH (MID-SCALE)

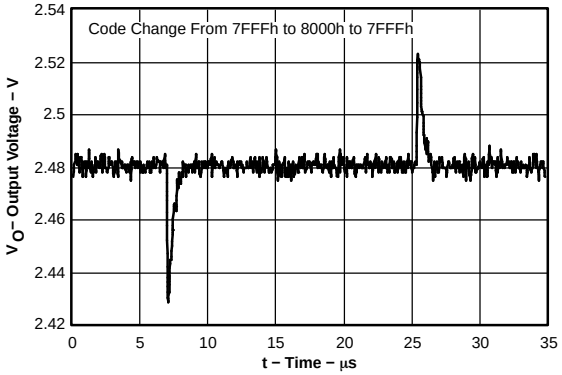


Figure 20.

FULL-SCALE SETTLING TIME

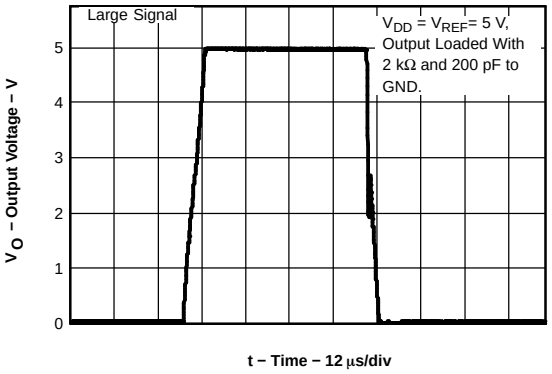


Figure 21.

HALF-SCALE SETTLING TIME

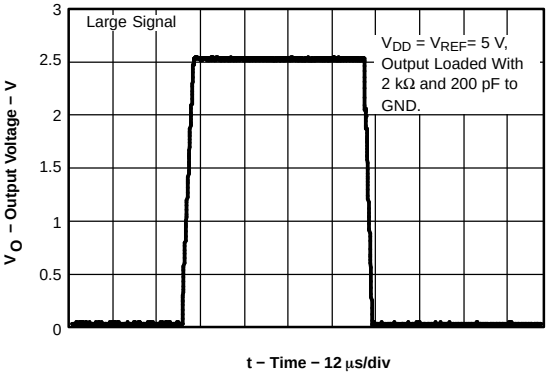


Figure 22.

FULL-SCALE SETTLING TIME

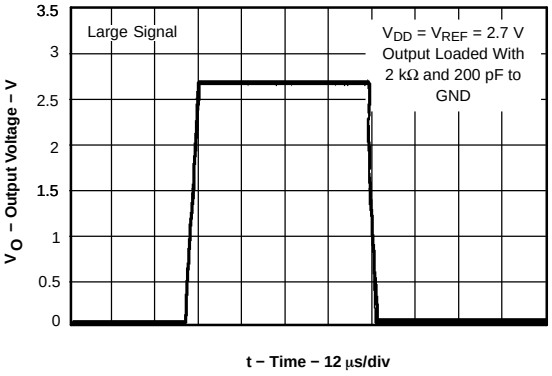


Figure 23.

HALF-SCALE SETTLING TIME

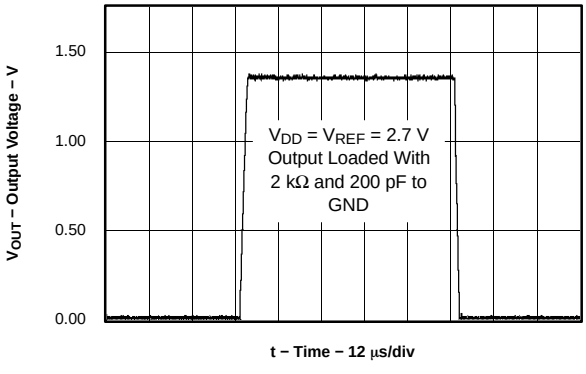


Figure 24.

TYPICAL CHARACTERISTICS (continued)

This condition applies to all typical characteristics: $V_{REF+} = V_{DD}$, $V_{REF-} = GND$, $T_A = 25°C$ (unless otherwise noted)

SIGNAL-TO-NOISE vs OUTPUT FREQUENCY

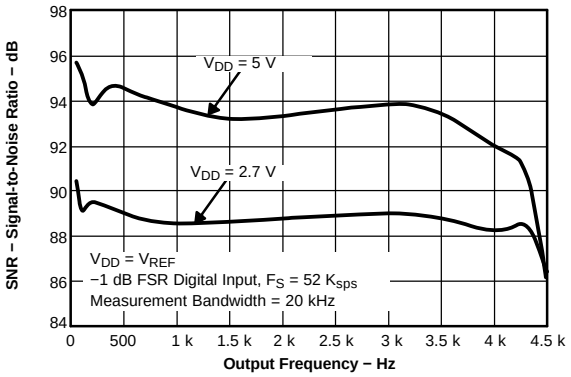


Figure 25.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

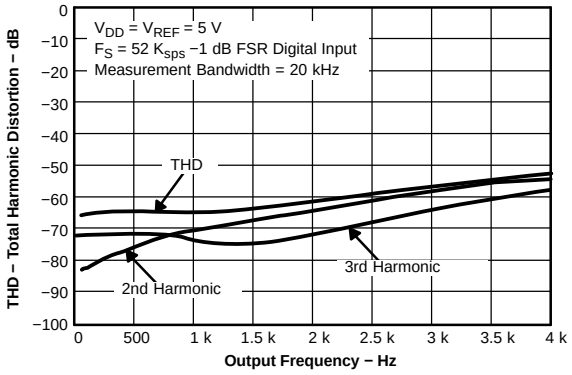


Figure 26.

TOTAL HARMONIC DISTORTION vs OUTPUT FREQUENCY

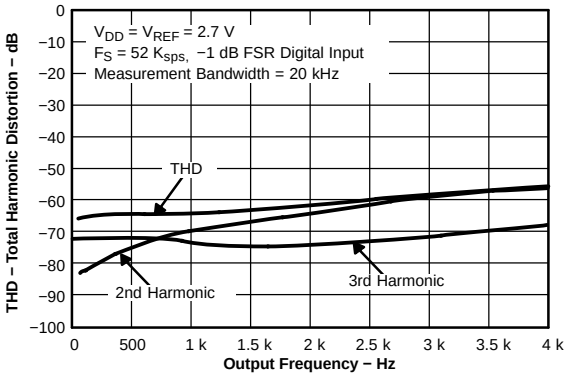


Figure 27.

FULL-SCALE SETTLING TIME (SMALL-SIGNAL POSITIVE-GOING STEP)

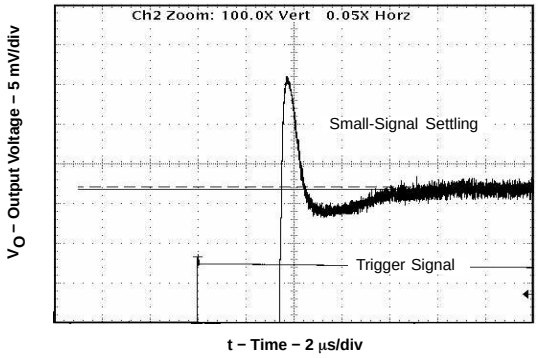


Figure 28.

FULL-SCALE SETTLING TIME (SMALL-SIGNAL NEGATIVE-GOING STEP)

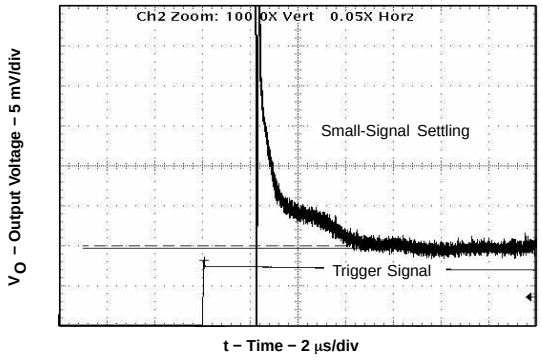


Figure 29.

THEORY OF OPERATION

D/A SECTION

The architecture of the DAC8544 consists of four string DACs followed by an output buffer amplifier. Figure 30 shows a block diagram of the DAC architecture.

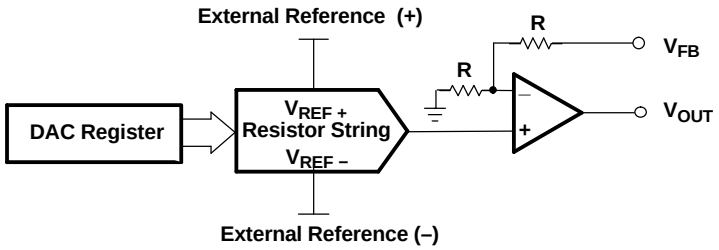


Figure 30. DAC8544 Architecture

The input coding to the DAC8544 is unsigned binary, which gives the ideal output voltage as:

$$V_{OUT} = 2 \times V_{REF-} + (V_{REF+} - V_{REF-}) \times \frac{D}{65536} \quad (1)$$

where

- D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 65535.

RESISTOR STRING

The resistor string section is shown in Figure 31. It is simply a divide-by-two resistor, followed by a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off, to be fed into the output amplifier, by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is assured monotonic.

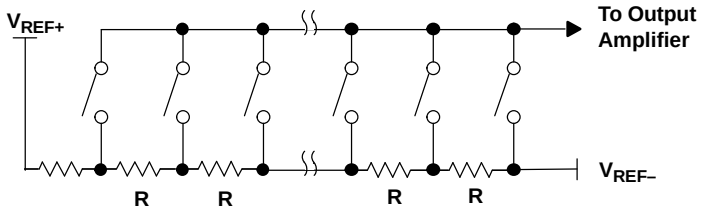


Figure 31. Resistor String

OUTPUT AMPLIFIER

The output buffer is capable of generating rail-to-rail voltages at its output, which gives an output range of 0 V to V_{REF+}. It is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in the typical curves. The slew rate is 1 V/μs with a full-scale settling time of 10 μs with the output loaded. The feedback and gain setting resistors of the amplifier are in the order of 50 kΩ. Their absolute value can be off significantly, but they are matched to within 0.1%.

The inverting input of the output amplifier is brought out to the V_{FB} pin, through the feedback resistor. This allows for better accuracy in critical applications by tying the V_{FB} point and the amplifier output together at the load. Other signal conditioning circuitry may also be connected between these points for specific applications including current sourcing.

THEORY OF OPERATION (continued)

PARALLEL INTERFACE

The DAC8544 provides a 16-bit parallel interface and supports both writing to and reading from the DAC input register. (See the timing characteristics section for detailed information for a typical write or read operation.) In addition to the data, $\overline{CS}$, and R/$\overline{W}$ inputs, the DAC8544's interface also provides power down, LDAC, and reset/reset-select control. Table 1 and Table 2 show the control signal actions and data format, respectively. These features are discussed in more detail in the remaining sections.

Table 1. DAC8544 CONTROL SIGNAL SUMMARY

$\overline{CS}$	R/$\overline{W}$	LDAC	RST	$\overline{PD}$	ACTION
H	X	X	X	X	Device data I/O is disabled on the bus.(1)
↓	L	X	H,L	H	Write initiated, present input data to the bus.
↓	H	X	H,L	H	Read initiated, data from input register is presented to data bus.
↑	X	X	H,L	H	Input data is latched when writing to the device.
X	X	↑	H,L	H	Data from input register is transferred to DAC register and V_{OUT} is updated.
X	X	X	↑	H	DAC register and V_{OUT} reset to min-scale. (If DAC is powered down during reset, DAC register resets and V_{OUT} settles to min-scale on power up.)
X	X	X	X	L	Power down device, V_{OUT} impedance equals high impedance

(1) Only disables 16-bit data I/O interface. Other control lines remain active.

LDAC FUNCTION

The DAC8544 is designed using a double-buffered architecture. A write operation (rising edge of $\overline{CS}$ while R/$\overline{W}$ is low) transfers data from the data input pins into the input register. The data is held in the input register until a rising-edge is detected on the LDAC input. This rising-edge signal transfers the data from the input register to the DAC register. On issuance of the rising LDAC edge, the output of the DAC8544 begins settling to the newly written data value presented to the DAC register. Data in the input register is not changed when an LDAC rising edge occurs.

UPDATE SEQUENCE

For regular operation, R/$\overline{W}$ pin should be kept low while $\overline{CS}$ is kept high. Then, the 16-bit digital data should be applied to the input bus. The channel selection should then be asserted by setting the A0 and A1 pins. The falling edge of $\overline{CS}$ enables the device. Once the data is stable and the channels are selected, the first rising edge of the $\overline{CS}$ signal latches the data to the input register of the selected channel. After the data is latched to the input register, the rising edge of the LDAC signal updates all four channels simultaneously with existing data from their corresponding input register.

READBACK

For read-back operation, the user first releases the 16-bit bus, while $\overline{CS}$ is high. Then, the DAC channel should be selected using the A0 and A1 pins. R/$\overline{W}$ pin is then brought high to enable read-back operation. Following the falling edge of $\overline{CS}$, the data from the selected channel (buffer data) is output on the bus.

RST

The RST input controls the reset of the DAC register and, consequently, the DAC output, but does not change the input register. The reset operation is edge-triggered by a low-to-high transition on the RST pin. Once a rising edge on RST is detected, the DAC output settles to the zero code. Application of a valid reset signal to the DAC does not overwrite existing data in the input register.

POWER-ON RESET

The DAC8544 contains a power-on reset circuit that controls the output voltage after power up. On power up, the DAC register (and DAC output) is set to zero (plus a small offset error produced by the output buffer). It remains at zero until a valid write sequence is made to the DAC, changing the DAC register data. This is useful in applications where it is important to know the state of the output of the DAC after power up. All digital inputs must be logic low until the digital and analog supplies are applied. Logic high voltages, applied to the input pins when power is not applied to IOV_{DD} and V_{DD}, may power the device through the ESD input structures causing undesired operation.

POWER-DOWN MODES

The DAC8544 uses two modes of operation. These modes are programmable via pin $\overline{PD}$.

Table 2 shows how the state of the pin correspond to the mode of operation of the DAC8544.

Table 2. Modes of Operation for the DAC8544

$\overline{PD}$	OPERATING MODE
High	Normal operation
Low	Power down, high impedance

When pin $\overline{PD}$ is high, the device works normally with its typical power consumption of 950 µA at V_{DD} = 5 V. However, when $\overline{PD}$ pin is in low state, the device is in power-down mode, the supply current falls to 200 nA at V_{DD} = 5 V (50 nA at V_{DD} = 3 V), and the output is open circuit (high impedance).

All analog circuitry is shut down when a power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down mode. This allows the DAC output voltage to return to the previous level when power up resumes. The delay time required to exit power-down is typically 2.5 µs for V_{DD} = 5 V, and 5 µs for V_{DD} = 3 V. (See the typical characteristics section for additional information.)

VOLTAGE REFERENCE INPUTS

Two voltage inputs provide the reference set points for the DAC architecture. These are V_{REF+} and V_{REF-}. For typical rail-to-rail operation, V_{REF+} should be equivalent to V_{DD} and V_{REF-} tied to GND. The output voltage is given by:

$$V_{OUT} = 2 \times V_{REF-} + (V_{REF+} - V_{REF-}) \times \frac{D}{65536} \quad (2)$$

The use of the V_{REF-} input allows minor adjustments to be made to the offset of the DAC output by applying a small voltage to the V_{REF-} input. A low output impedance source is needed, so that the accuracy of the DAC over its operating range is not affected.

ANALOG AND DIGITAL SUPPLIES

The analog supply (V_{DD}) powers the output buffer and DAC while the digital supply (IOV_{DD}) powers the digital interface. V_{DD} can operate from 2.7 V to 5.5 V while IOV_{DD} can independently function from 1.8 V to 5.5 V. IOV_{DD} determines the interface logic level. See the device specification table for details.

EXTERNAL REFERENCE VOLTAGE

To take advantage of the absolute accuracy of DAC8544, a high-performance reference voltage generator must be used. DAC8544 has a typical absolute accuracy error of 2 millivolts, and a typical voltage drift of 3 ppm/°C. This level of performance requires an accurate external reference voltage generator with good temperature drift characteristics. Accuracy, drift, supply voltage, power consumption, and cost are important factors in choosing a voltage reference. TI's REF02 is recommended. TI's REF3140 and REF3040 are small and low-cost alternatives.

FEEDBACK PINS

For regular operation, the feedback pins (V_{FBA} through V_{FBD}) must be tied to their corresponding output pins (V_{OUTA} through V_{OUTD}) at the load. For higher current applications sensitive to gain error, the feedback pin should be routed to the target node, to sense the node voltage accurately (DAC8544 gain error is typically low, around 1 mV).

HOST PROCESSOR INTERFACING

DAC8544 to MSP430 Microcontroller

Figure 32 shows a typical parallel interface connection between the DAC8544 and a MSP430 microcontroller. The setup for the interface shown uses ports 4 and 5 of the MSP430 to send or receive the 16-bit data while bits 0-7 of port 2 provides the control signals for the DAC. When data is to be transmitted to the DAC8544, the data is made available to the DAC via P4 and P5, and P2.1 is taken low. The MSP430 then toggles P2.0 from high-to-low and back to high, transferring the 16-bit data to the DAC. This data is loaded into the DAC register by applying a rising edge to P2.4. The remaining five I/O signals of P2 shown in the figure control the reset, power-down, and data format functions of the DAC. Depending on the specific requirements of a given application, these pins may be tied to IOGND or IOV_{DD}, enabling the desired mode of operation.

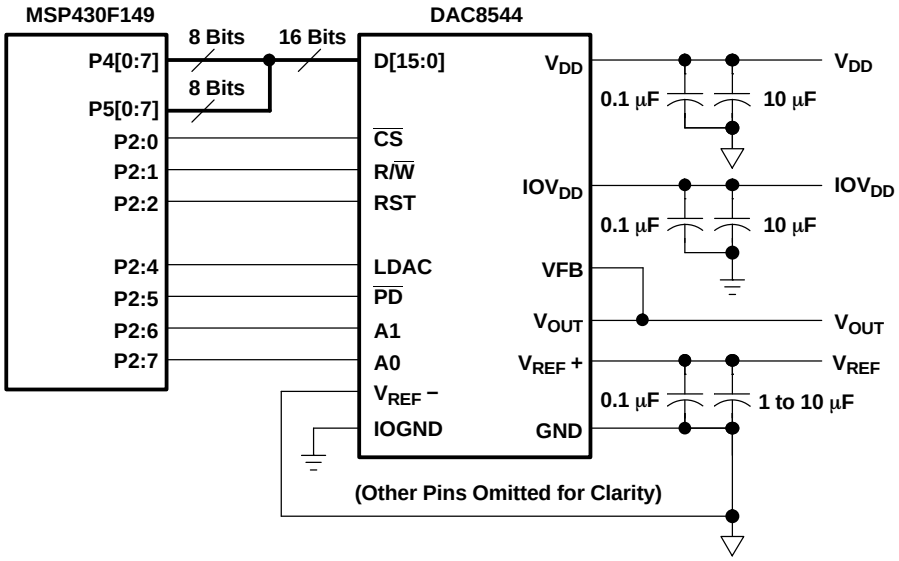


Figure 32. DAC8544 to MSP430 Microcontroller

DAC8544 to TMS320C5402 DSP

Figure 33 shows the connections between the DAC8544 and the TMS320C5402 digital signal processor. Data is provided via the parallel data bus of the DSP while the DAC $\overline{CS}$ control input is derived from the decoded I/O strobe signal. The IOSTRB in addition to the R/$\overline{W}$ and XF(I/O) signals control the data transmission to and from the DAC as well as the LDAC control. With additional decoding, multiple DAC8544s can be connected to the same parallel data bus of the DSP.

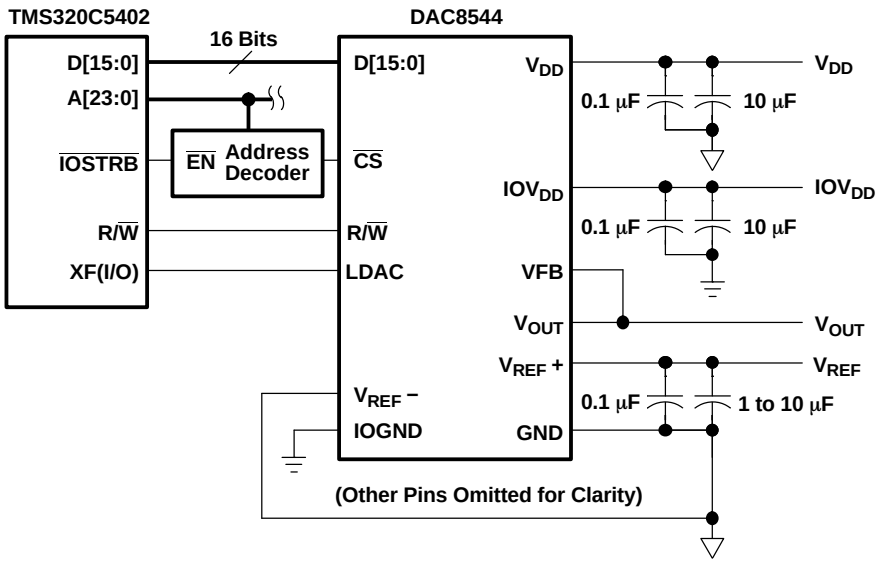


Figure 33. DAC8544 to TMS320 DSP

BIPOLAR OPERATION USING THE DAC8544

The DAC8544 has been designed for single-supply operation but a bipolar output range is also possible using the circuit shown in Figure 34. The circuit allows the DAC8544 to achieve an analog output range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an OPA703 as the output amplifier.

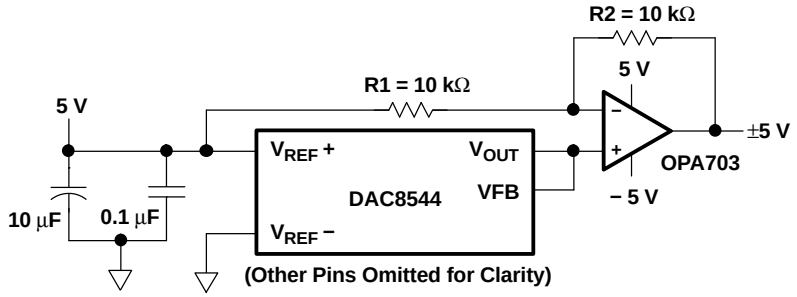


Figure 34. Bipolar Operation With the DAC8544

With V_{REF+} = 5 V, R1 = R2 = 10 kΩ:

$$V_{OUT} = \left(\frac{10 \times D}{65536}\right) - 5V \quad (3)$$

LAYOUT

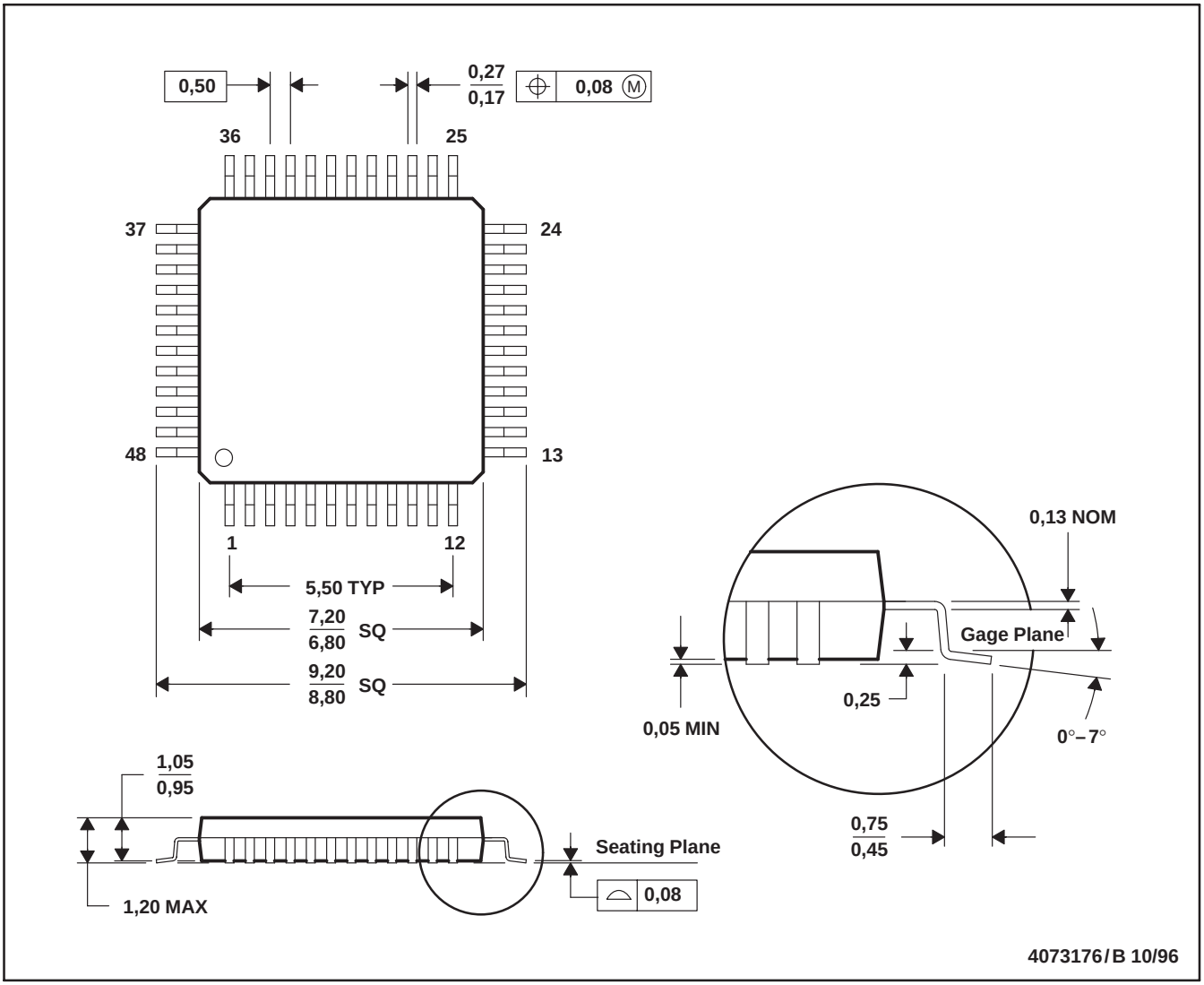
A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The following measures should be taken to assure optimum performance of the DAC8544. The DAC8544 offers dual-supply operation, as it can often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more important it becomes to separate the analog and digital ground and supply planes at the DAC.

Because the DAC8544 has both analog and digital ground pins, return currents can be better controlled and have less effect on the DAC output error. Ideally, GND would be connected directly to an analog ground plane and GND to the digital ground plane. The analog ground plane would be separate from the ground connection for the digital components until they were connected at the power entry point of the system. The power applied to V_{DD} and V_{REF+} (this also applies to V_{REF-} if not tied to GND) should be well-regulated and low-noise. Switching power supplies and dc/dc converters often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

As with the GND connection, V_{DD} should be connected to a 5-V power supply plane or trace that is separate from the connection for digital logic until they are connected at the power entry point. In addition, the 1-µF to 10-µF and 0.1-µF bypass capacitors are strongly recommended. In some situations, additional bypassing may be required, such as a 100-µF electrolytic capacitor or even a Pi filter made up of inductors and capacitors—all designed to essentially lowpass-filter the V_{DD} supply, removing the high-frequency noise.

MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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