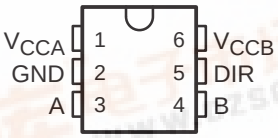
SINGLE-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

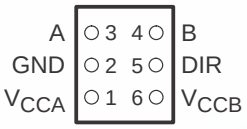
SCES598C – JULY 2004 – REVISED OCTOBER 2004

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Control Inputs V_{IH}/V_{IL} Levels Are Referenced to V_{CCA} Voltage
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range
- I/Os Are 4.6-V Tolerant
- I_{off} Supports Partial-Power-Down Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

DBV OR DCK PACKAGE
(TOP VIEW)



YEP OR YZP PACKAGE
(BOTTOM VIEW)



description/ordering information

This single-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}. V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB}. V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

The SN74AVCH1T45 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input.

The SN74AVCH1T45 is designed so that the DIR input is powered by V_{CCA}.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
−40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Tape and reel	SN74AVCH1T45YEPR	_ _ _TF_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Tape and reel	SN74AVCH1T45YZPR	
	SOT (SOT-23) – DBV	Tape and reel	SN74AVCH1T45DBVR	ET1_
	SOT (SC-70) – DCK	Tape and reel	SN74AVCH1T45DCKR	TF_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

description/ordering information (continued)

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both outputs are in the high-impedance state. The bus-hold circuitry on the powered-up side always stays active.

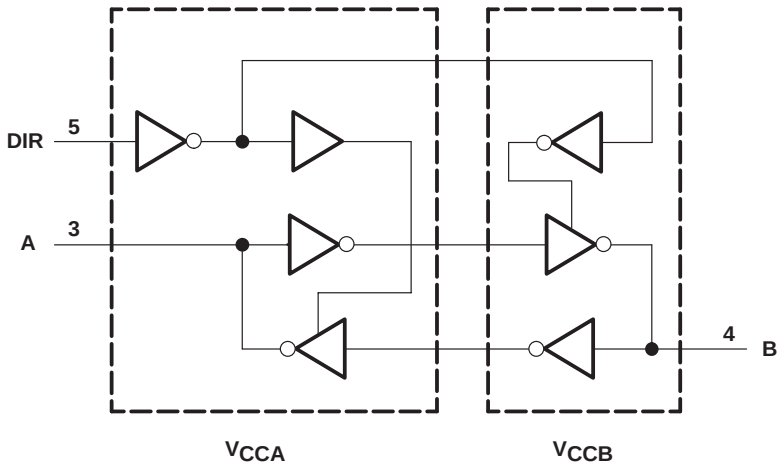
Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

FUNCTION TABLE

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CCA} and V_{CCB}	−0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): I/O ports (A port)	−0.5 V to 4.6 V
I/O ports (B port)	−0.5 V to 4.6 V
Control inputs	−0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1): A port	−0.5 V to 4.6 V
B port	−0.5 V to 4.6 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2): A port	−0.5 V to V_{CCA} + 0.5 V
B port	−0.5 V to V_{CCB} + 0.5 V
Input clamp current, I_{IK} (V_I < 0)	−50 mA
Output clamp current, I_{OK} (V_O < 0)	−50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CCA}, V_{CCB}, or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DBV package	165°C/W
DCK package	259°C/W
YEP/YZP package	123°C/W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Notes 4 through 8)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs (see Note 7)	1.2 V to 1.95 V		$V_{CCI} \times 0.65$		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs (see Note 7)	1.2 V to 1.95 V			$V_{CCI} \times 0.35$	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA}) (see Note 8)	1.2 V to 1.95 V		$V_{CCA} \times 0.65$		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA}) (see Note 8)	1.2 V to 1.95 V			$V_{CCA} \times 0.35$	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2 V		−3	mA
				1.4 V to 1.6 V		−6	
				1.65 V to 1.95 V		−8	
				2.3 V to 2.7 V		−9	
				3 V to 3.6 V		−12	
I_{OL}	Low-level output current			1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				−40	85	°C

NOTES: 4. V_{CCI} is the V_{CC} associated with the data input port.
5. V_{CCO} is the V_{CC} associated with the output port.
6. All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
7. For V_{CCI} values not specified in the data sheet, V_{IH} min = $V_{CCI} \times 0.7$ V, V_{IL} max = $V_{CCI} \times 0.3$ V.
8. For V_{CCI} values not specified in the data sheet, V_{IH} min = $V_{CCA} \times 0.7$ V, V_{IL} max = $V_{CCA} \times 0.3$ V.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 9 and 10)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A = 25°C			−40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = −100 µA	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V				V_{CCO} − 0.2 V		V
		I_{OH} = −3 mA		1.2 V	1.2 V		0.95				
		I_{OH} = −6 mA		1.4 V	1.4 V				1.05		
		I_{OH} = −8 mA		1.65 V	1.65 V				1.2		
		I_{OH} = −9 mA		2.3 V	2.3 V				1.75		
		I_{OH} = −12 mA		3 V	3 V				2.3		
V_{OL}		I_{OL} = 100 µA	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V					0.2	V
		I_{OL} = 3 mA		1.2 V	1.2 V		0.15				
		I_{OL} = 6 mA		1.4 V	1.4 V					0.35	
		I_{OL} = 8 mA		1.65 V	1.65 V					0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V					0.55	
		I_{OL} = 12 mA		3 V	3 V					0.7	
I_I	DIR input	$V_I = V_{CCA}$ or GND		1.2 V to 3.6 V	1.2 V to 3.6 V		±0.025	±0.25		±1	µA
I_{BHL}†		V_I = 0.42 V		1.2 V	1.2 V		25				µA
		V_I = 0.49 V		1.4 V	1.4 V				15		
		V_I = 0.58 V		1.65 V	1.65 V				25		
		V_I = 0.7 V		2.3 V	2.3 V				45		
		V_I = 0.8 V		3.3 V	3.3 V				100		
I_{BHH}‡		V_I = 0.78 V		1.2 V	1.2 V		−25				µA
		V_I = 0.91 V		1.4 V	1.4 V				−15		
		V_I = 1.07 V		1.65 V	1.65 V				−25		
		V_I = 1.6 V		2.3 V	2.3 V				−45		
		V_I = 2 V		3.3 V	3.3 V				−100		
I_{BHLO}§		V_I = 0 to V_{CC}		1.2 V	1.2 V		50				µA
				1.6 V	1.6 V				125		
				1.95 V	1.95 V				200		
				2.7 V	2.7 V				300		
				3.6 V	3.6 V				500		
I_{BHHO}¶		V_I = 0 to V_{CC}		1.2 V	1.2 V		−50				µA
				1.6 V	1.6 V				−125		
				1.95 V	1.95 V				−200		
				2.7 V	2.7 V				−300		
				3.6 V	3.6 V				−500		

† The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.
‡ The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
§ An external driver must source at least I_{BHLO} to switch this node from low to high.
¶ An external driver must sink at least I_{BHHO} to switch this node from high to low.
NOTES: 9. V_{CCO} is the V_{CC} associated with the output port.
10. V_{CCI} is the V_{CC} associated with the input port.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 9 and 10) (continued)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A = 25°C			−40°C to 85°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
I_{off}	A port	V_I or V_O = 0 to 3.6 V	0 V	0 to 3.6 V		±0.1	±1		±5	µA
	B port		0 to 3.6 V	0 V		±0.1	±1		±5	
I_{OZ}	A or B ports	V_O = V_{CCO} or GND	1.2 V to 3.6 V	1.2 V to 3.6 V		±0.5	±2.5		±5	µA
I_{CCA}		V_I = V_{CCI} or GND, I_O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V					10	µA
			0 V	3.6 V					−2	
			3.6 V	0 V					10	
I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V					10	µA
			0 V	3.6 V					10	
			3.6 V	0 V					−2	
I_{CCA} + I_{CCB}		V_I = V_{CCI} or GND, I_O = 0	1.2 V to 3.6 V	1.2 V to 3.6 V					20	µA
C_i	Control inputs	V_I = 3.3 V or GND	3.3 V	3.3 V		2.5				pF
C_{io}	A or B ports	V_O = 3.3 V or GND	3.3 V	3.3 V		6				pF

NOTES: 9. V_{CCO} is the V_{CC} associated with the output port.
10. V_{CCI} is the V_{CC} associated with the input port.

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 1.2 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V	V_{CCB} = 1.8 V	V_{CCB} = 2.5 V	V_{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH}	A	B	3.3	2.7	2.4	2.3	2.4	ns
t_{PHL}			3.3	2.7	2.4	2.3	2.4	
t_{PLH}	B	A	3.3	3.1	2.9	2.8	2.7	ns
t_{PHL}			3.3	3.1	2.9	2.8	2.7	
t_{PHZ}	DIR	A	5.1	5.2	5.3	5.2	3.7	ns
t_{PLZ}			5.1	5.2	5.3	5.2	3.7	
t_{PHZ}	DIR	B	5.3	4.3	4	3.3	3.7	ns
t_{PLZ}			5.3	4.3	4	3.3	3.7	
t_{PZH}†	DIR	A	8.5	6.9	6.4	5.5	6.1	ns
t_{PZL}†			8.5	6.9	6.4	5.5	6.1	
t_{PZH}†	DIR	B	8.3	7.8	7.7	7.5	5.9	ns
t_{PZL}†			8.3	7.8	7.7	7.5	5.9	

† The enable time is a calculated value, derived using the formula shown in the *enable times* section, page 16.

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 1.5 V ± 0.1 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.9	0.7	5.6	0.6	5.2	0.5	4.2	0.5	3.8	ns
t_{PHL}			2.9	0.7	5.6	0.6	5.2	0.5	4.2	0.5	3.8	
t_{PLH}	B	A	2.6	0.6	5.5	0.4	5.3	0.3	4.9	0.3	4.8	ns
t_{PHL}			2.6	0.6	5.5	0.4	5.3	0.3	4.9	0.3	4.8	
t_{PHZ}	DIR	A	3.8	1.6	6.7	1.5	6.8	0.3	6.9	0.9	6.9	ns
t_{PLZ}			3.8	1.6	6.7	1.5	6.8	0.3	6.9	0.9	6.9	
t_{PHZ}	DIR	B	5.1	1.8	8.1	1.6	7.1	1.1	4.7	1.4	4.5	ns
t_{PLZ}			5.1	1.8	8.1	1.6	7.1	1.1	4.7	1.4	4.5	
t_{PZH}†	DIR	A	7.7		13.6		12.4		9.6		9.3	ns
t_{PZL}†			7.7		13.6		12.4		9.6		9.3	
t_{PZH}†	DIR	B	6.7		12.3		12		11.1		10.7	ns
t_{PZL}†			6.7		12.3		12		11.1		10.7	

† The enable time is a calculated value, derived using the formula shown in the *enable times* section, page 16.

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.8	0.6	5.3	0.5	5	0.4	3.9	0.4	3.4	ns
t_{PHL}			2.8	0.6	5.3	0.5	5	0.4	3.9	0.4	3.4	
t_{PLH}	B	A	2.3	0.5	5.2	0.4	5	0.3	4.6	0.2	4.4	ns
t_{PHL}			2.3	0.5	5.2	0.4	5	0.3	4.6	0.2	4.4	
t_{PHZ}	DIR	A	3.8	1.6	5.9	1.6	5.9	1.6	5.9	0.5	6	ns
t_{PLZ}			3.8	1.6	5.9	1.6	5.9	1.6	5.9	0.5	6	
t_{PHZ}	DIR	B	5	1.8	7.7	1.4	6.8	1	4.4	1.4	4.3	ns
t_{PLZ}			5	1.89	7.7	1.4	6.8	1	4.4	1.4	4.3	
t_{PZH}†	DIR	A	7.3		12.9		11.8		9		8.7	ns
t_{PZL}†			7.3		12.9		11.8		9		8.7	
t_{PZH}†	DIR	B	6.5		11.2		10.9		9.8		9.4	ns
t_{PZL}†			6.5		11.2		10.9		9.8		9.4	

† The enable time is a calculated value, derived using the formula shown in the *enable times* section, page 16.

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.6	0.5	4.9	0.4	4.6	0.3	3.4	0.3	3	ns
t_{PHL}			2.6	0.5	4.9	0.4	4.6	0.3	3.4	0.3	3	
t_{PLH}	B	A	2.2	0.4	4.2	0.3	3.8	0.2	3.4	0.2	3.3	ns
t_{PHL}			2.2	0.4	4.2	0.3	3.8	0.2	3.4	0.2	3.3	
t_{PHZ}	DIR	A	2.8	0.3	3.8	0.8	3.8	0.4	3.8	0.5	3.8	ns
t_{PLZ}			2.8	0.3	3.8	0.8	3.8	0.4	3.8	0.5	3.8	
t_{PHZ}	DIR	B	4.9	2	7.6	1.5	6.5	0.6	4.1	1	4	ns
t_{PLZ}			4.9	2	7.6	1.5	6.5	0.6	4.1	1	4	
t_{PZH}†	DIR	A	7.1		11.8		10.3		7.5		7.3	ns
t_{PZL}†			7.1		11.8		10.3		7.5		7.3	
t_{PZH}†	DIR	B	5.4		8.6		8.1		7		6.6	ns
t_{PZL}†			5.4		8.6		8.1		7		6.6	

† The enable time is a calculated value, derived using the formula shown in the *enable times* section, page 16.

switching characteristics over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (see Figure 11)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB} = 1.2 V	V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	2.6	0.4	4.7	0.3	4.4	0.2	3.3	0.2	2.8	ns
t_{PHL}			2.6	0.4	4.7	0.3	4.4	0.2	3.3	0.2	2.8	
t_{PLH}	B	A	2.2	0.4	3.8	0.3	3.4	0.2	3	0.1	2.8	ns
t_{PHL}			2.2	0.4	3.8	0.3	3.4	0.2	3	0.1	2.8	
t_{PHZ}	DIR	A	3.1	1.3	4.3	1.3	4.3	1.3	4.3	1.3	4.3	ns
t_{PLZ}			3.1	1.3	4.3	1.3	4.3	1.3	4.3	1.3	4.3	
t_{PHZ}	DIR	B	4	0.7	7.4	0.6	6.5	0.7	4	1.5	3.9	ns
t_{PLZ}			4	0.7	7.4	0.6	6.5	0.7	4	1.5	3.9	
t_{PZH}†	DIR	A	6.2		11.2		9.9		7		6.7	ns
t_{PZL}†			6.2		11.2		9.9		7		6.7	
t_{PZH}†	DIR	B	5.7		8.9		8.5		7.2		6.8	ns
t_{PZL}†			5.7		8.9		8.5		7.2		6.8	

† The enable time is a calculated value, derived using the formula shown in the *enable times* section, page 16.

operating characteristics, $T_A = 25°C$

PARAMETER		TEST CONDITIONS	V_{CCA} = V_{CCB} = 1.2 V	V_{CCA} = V_{CCB} = 1.5 V	V_{CCA} = V_{CCB} = 1.8 V	V_{CCA} = V_{CCB} = 2.5 V	V_{CCA} = V_{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
C_{pdA}†	A-port input, B-port output	C_L = 0 pF, f = 10 MHz, $t_r = t_f$ = 1 ns	3	3	3	3	4	pF
	B-port input, A-port output		14	14	14	15	16	
C_{pdB}†	A-port input, B-port output	C_L = 0 pF, f = 10 MHz, $t_r = t_f$ = 1 ns	14	14	14	15	16	pF
	B-port input, A-port output		3	3	3	3	4	

† Power-dissipation capacitance per transceiver

power-up considerations

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA}.
3. V_{CCB} can be ramped up along with or after V_{CCA}.

typical total static power consumption (I_{CCA} + I_{CCB})

Table 1

V_{CCB}	V_{CCA}						UNIT
	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	<0.5	<0.5	<0.5	<0.5	<0.5	μA
1.2 V	<0.5	<1	<1	<1	<1	1	
1.5 V	<0.5	<1	<1	<1	<1	1	
1.8 V	<0.5	<1	<1	<1	<1	<1	
2.5 V	<0.5	1	<1	<1	<1	<1	
3.3 V	<0.5	1	<1	<1	<1	<1	

TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, $T_A = 25°C$, $V_{CCA} = 1.2$ V

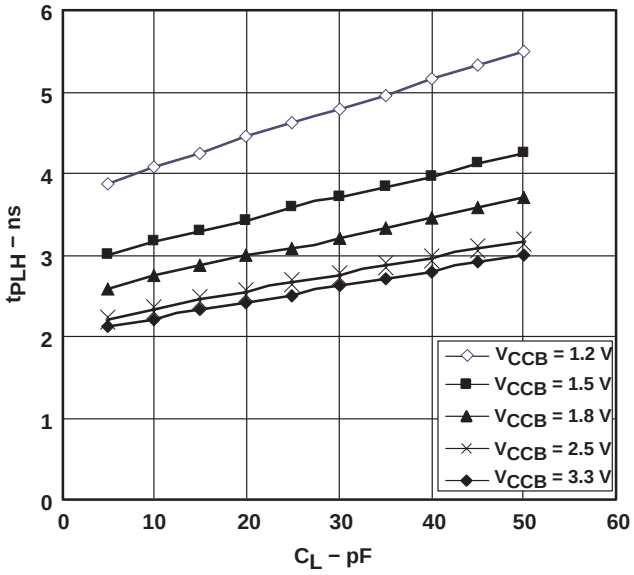


Figure 1

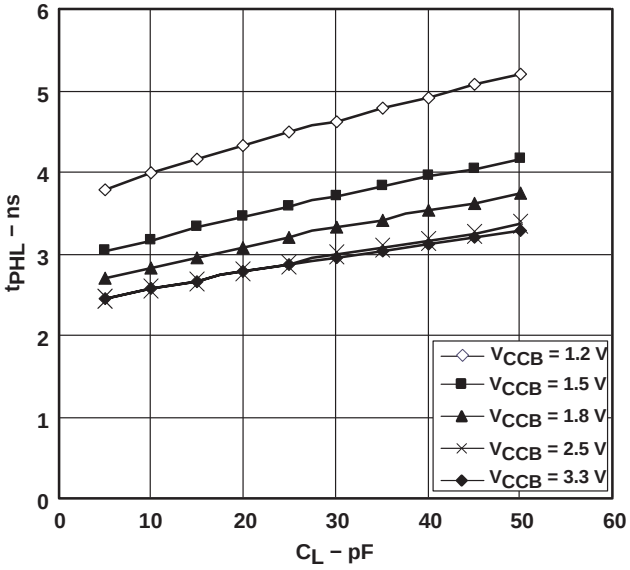


Figure 2

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE, $T_A = 25°C$, $V_{CCA} = 1.5$ V

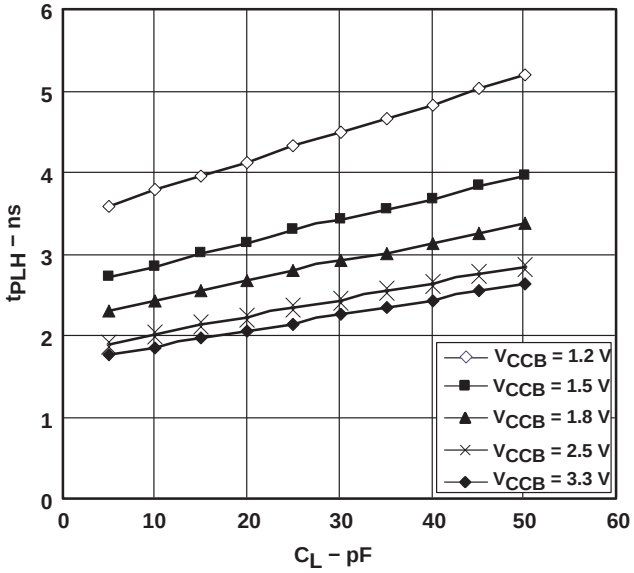


Figure 3

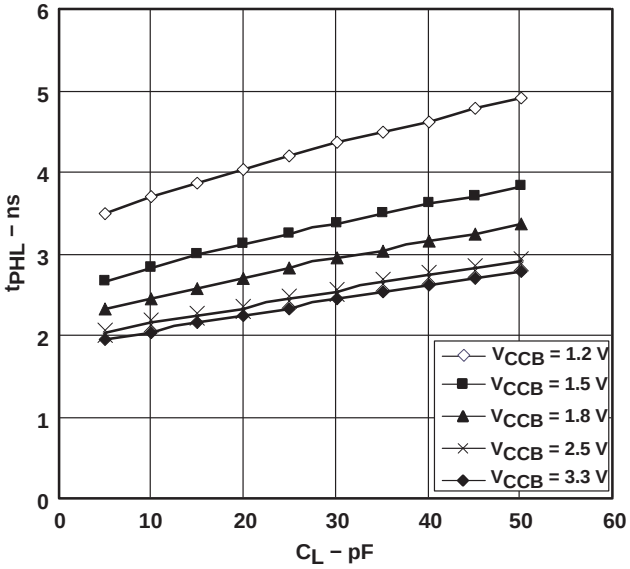


Figure 4

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE,
T_A = 25°C, V_{CCA} = 1.8 V

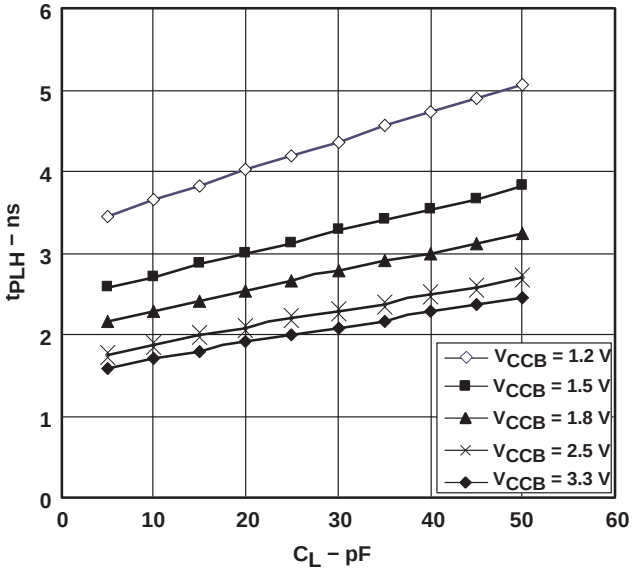


Figure 5

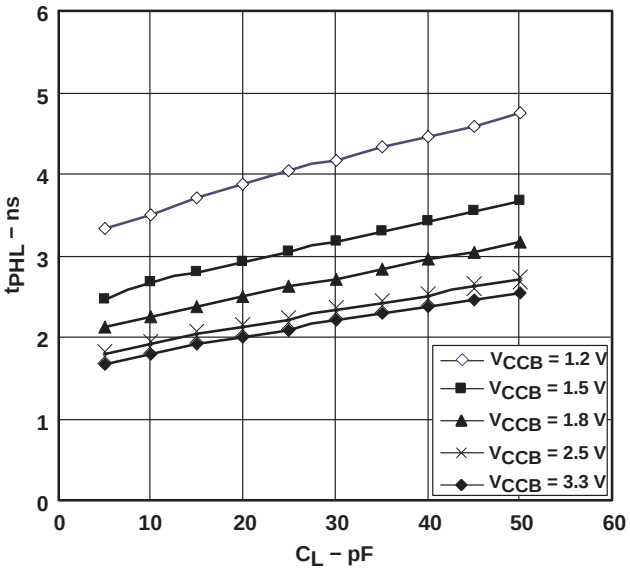


Figure 6

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE,
T_A = 25°C, V_{CCA} = 2.5 V

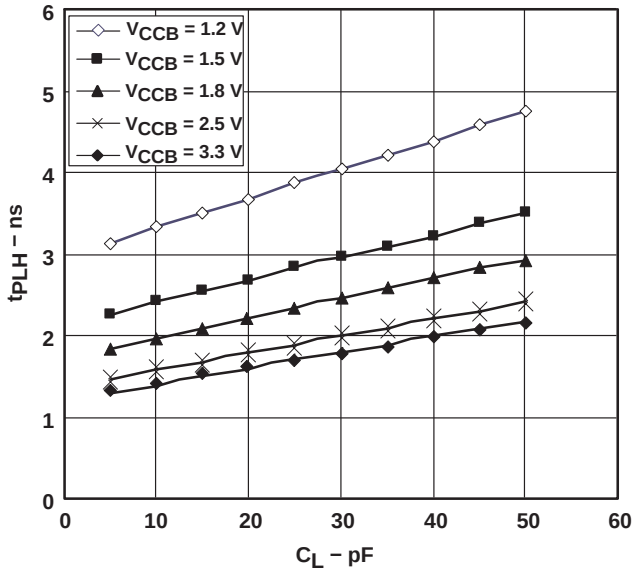


Figure 7

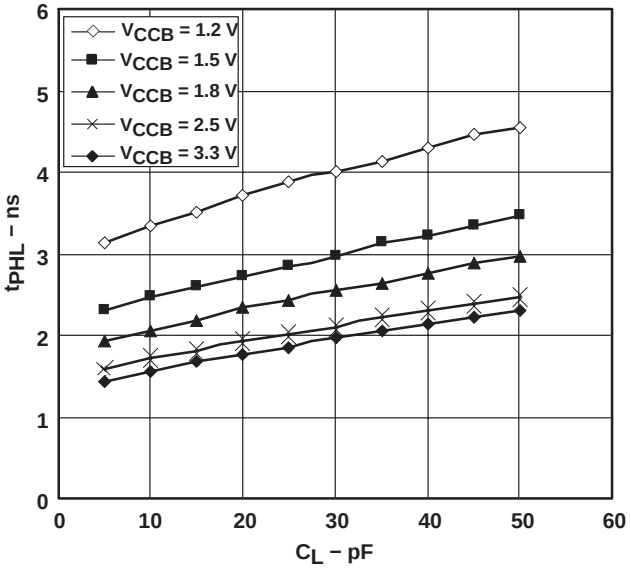


Figure 8

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE,
T_A = 25°C, V_{CCA} = 3.3 V

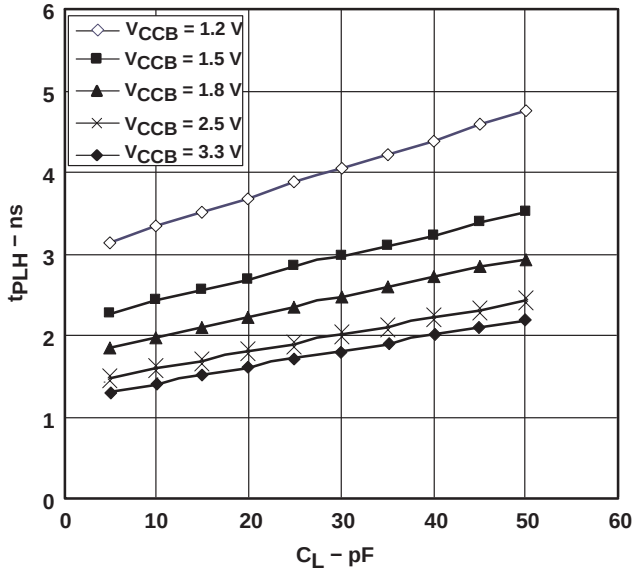


Figure 9

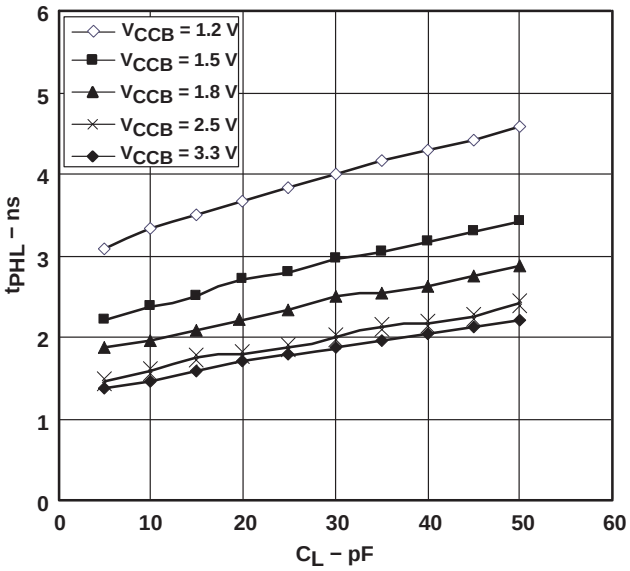
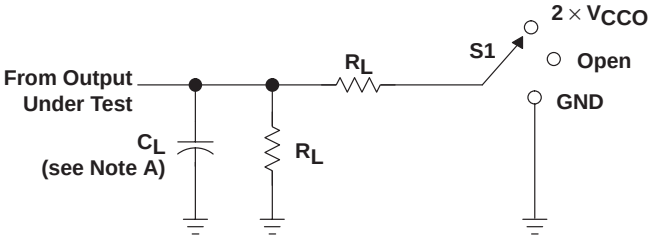


Figure 10

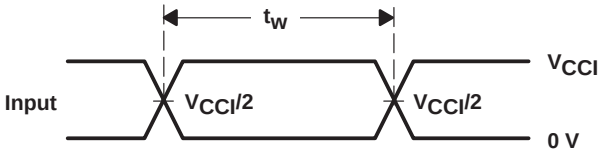
PARAMETER MEASUREMENT INFORMATION



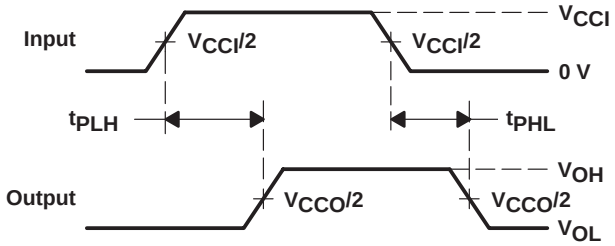
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

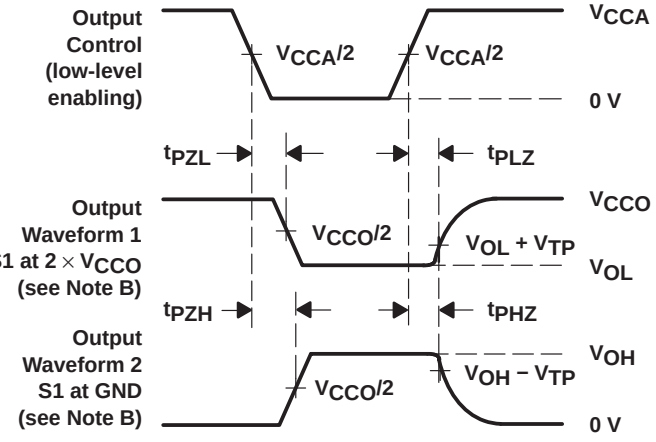
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



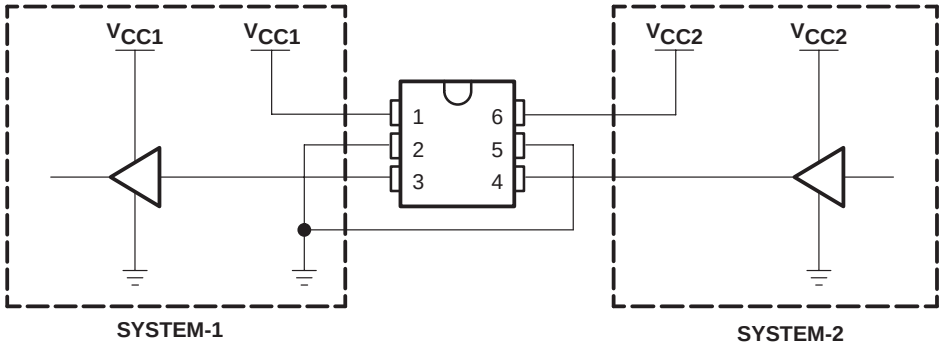
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns, dv/dt ≥1 V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

Figure 11. Load Circuit and Voltage Waveforms

APPLICATION INFORMATION

Figure 12 shows an example of the SN74AVCH1T45 being used in a unidirectional logic level-shifting application.

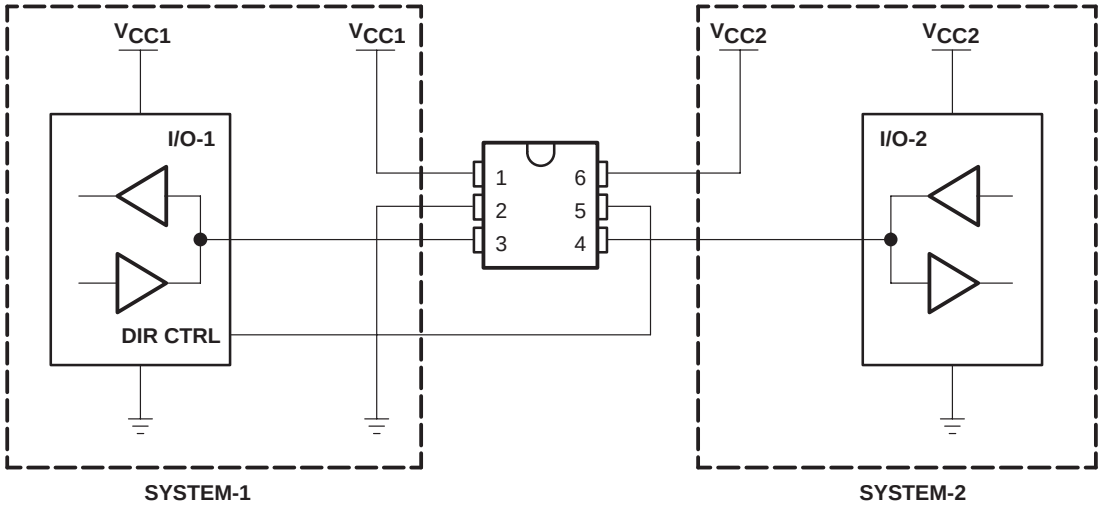


PIN	NAME	FUNCTION	DESCRIPTION
1	V_{CCA}	V_{CC1}	SYSTEM-1 supply voltage (1.2 V to 3.6 V)
2	GND	GND	Device GND
3	A	OUT	Output level depends on V_{CC1} voltage.
4	B	IN	Input threshold value depends on V_{CC2} voltage.
5	DIR	DIR	GND (low level) determines B-port to A-port direction.
6	V_{CCB}	V_{CC2}	SYSTEM-2 supply voltage (1.2 V to 3.6 V)

Figure 12. Unidirectional Logic Level-Shifting Application

APPLICATION INFORMATION

Figure 13 shows the SN74AVCH1T45 being used in a bidirectional logic level-shifting application. Since the SN74AVCH1T45 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.



Following is a sequence that illustrates data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on bus hold.
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 are still disabled. The bus-line state depends on bus hold.
4	L	Out	In	SYSTEM-2 data to SYSTEM-1

Figure 13. Bidirectional Logic Level-Shifting Application

enable times

Calculate the enable times for the SN74AVCH1T45 using the following formulas:

t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)

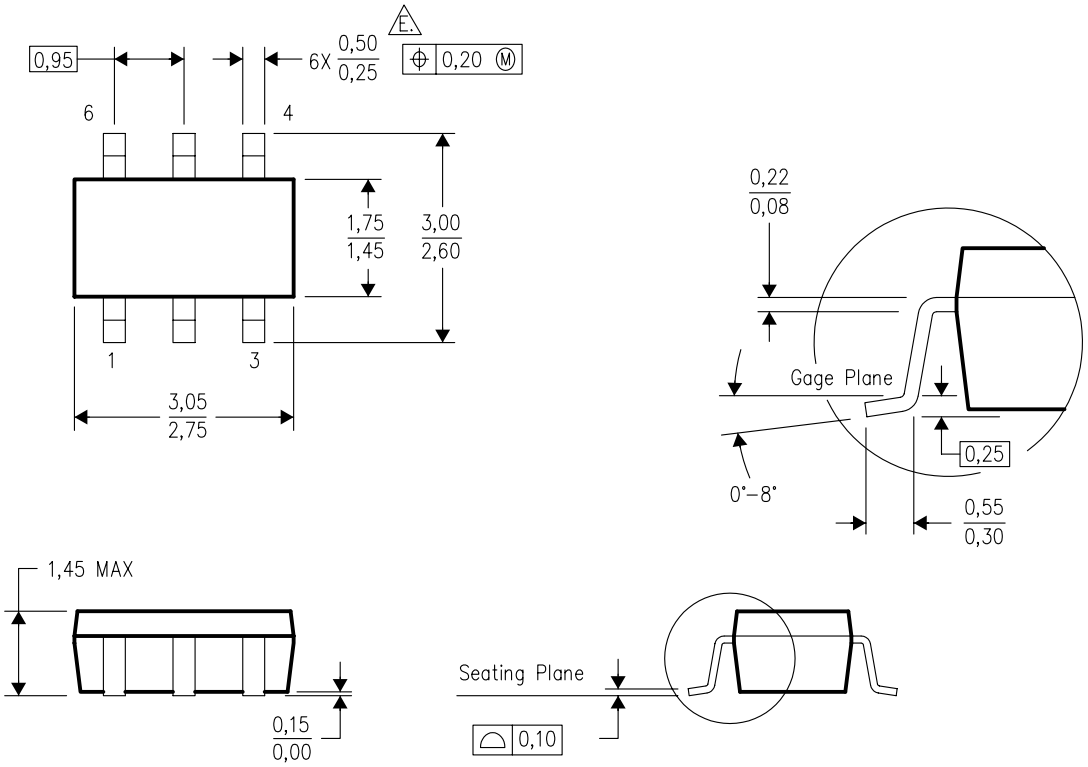
t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)

t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)

t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVCH1T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

DBV (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE

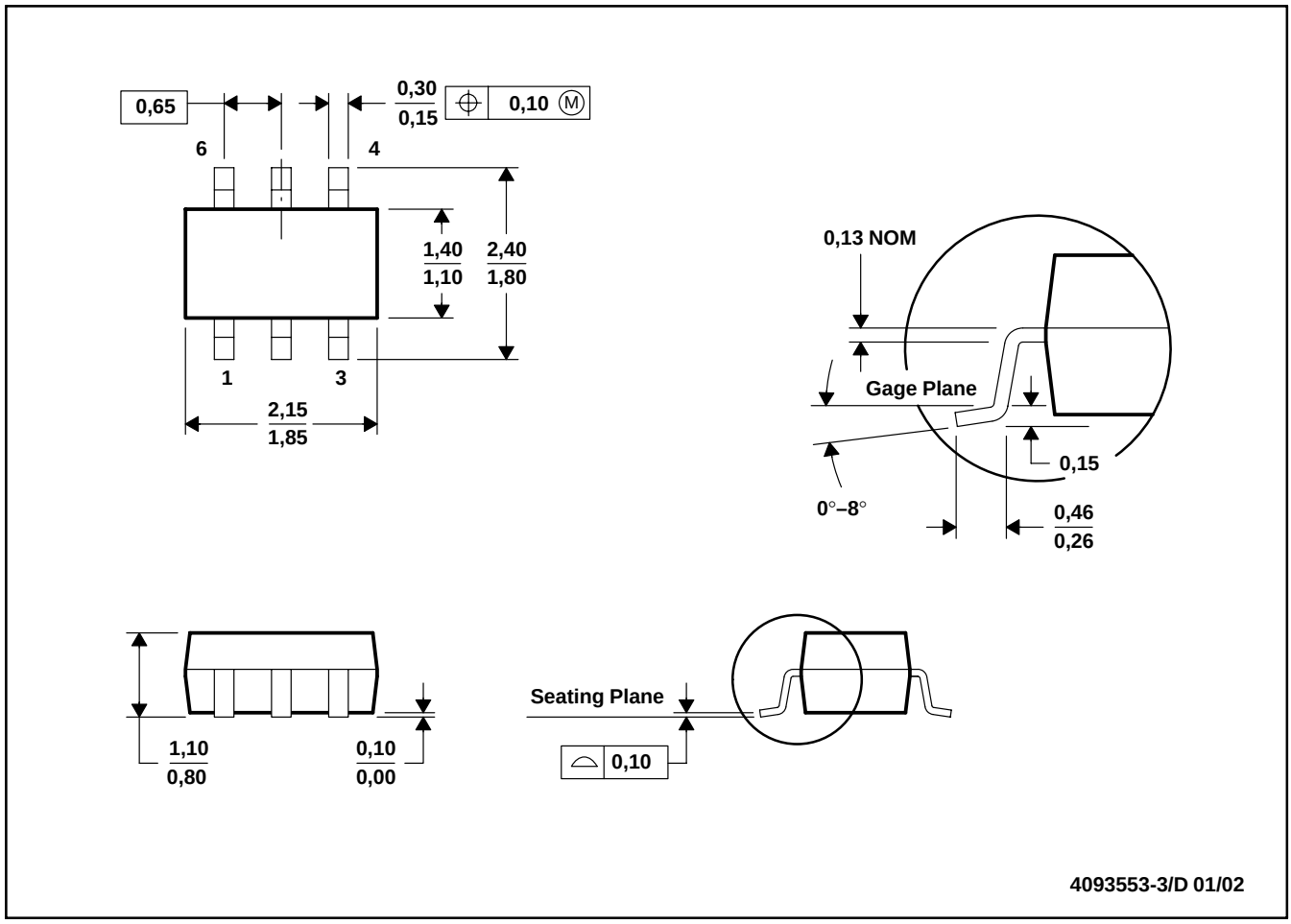


4073253–5/I 04/2005

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
E. Falls within JEDEC MO–178 Variation AB, except minimum lead width.

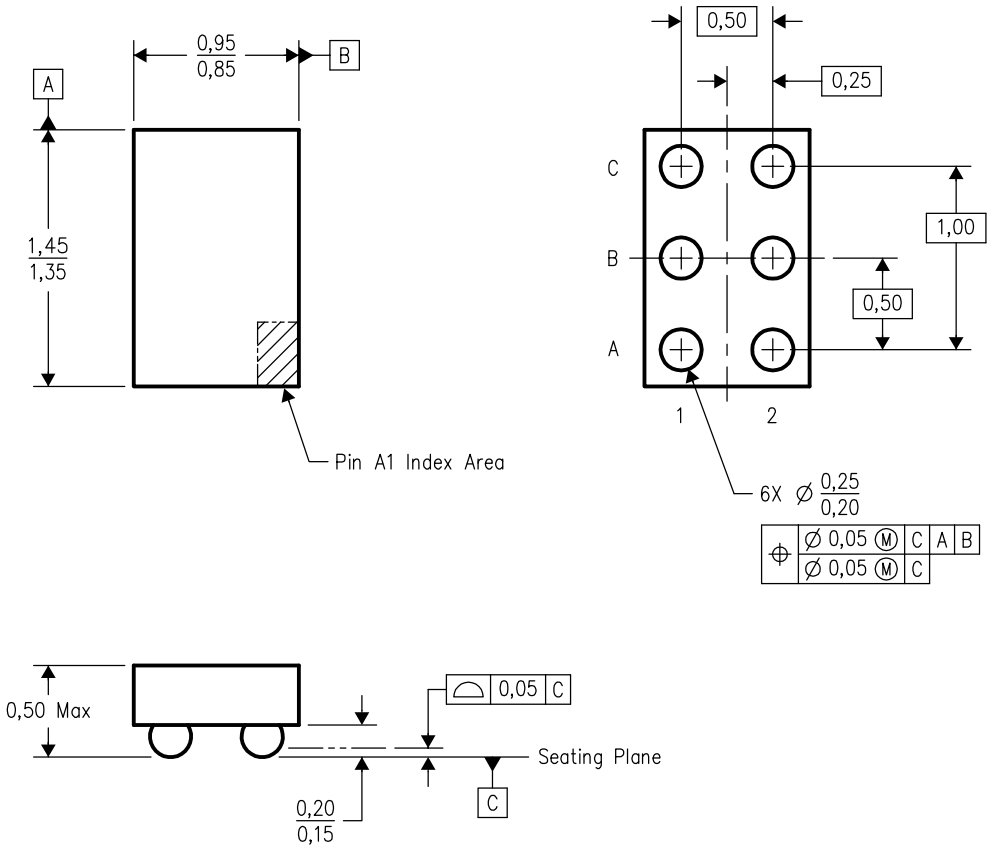
MPDS114 – FEBRUARY 2002

DCK (R-PDSO-G6) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-203

YZP (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY

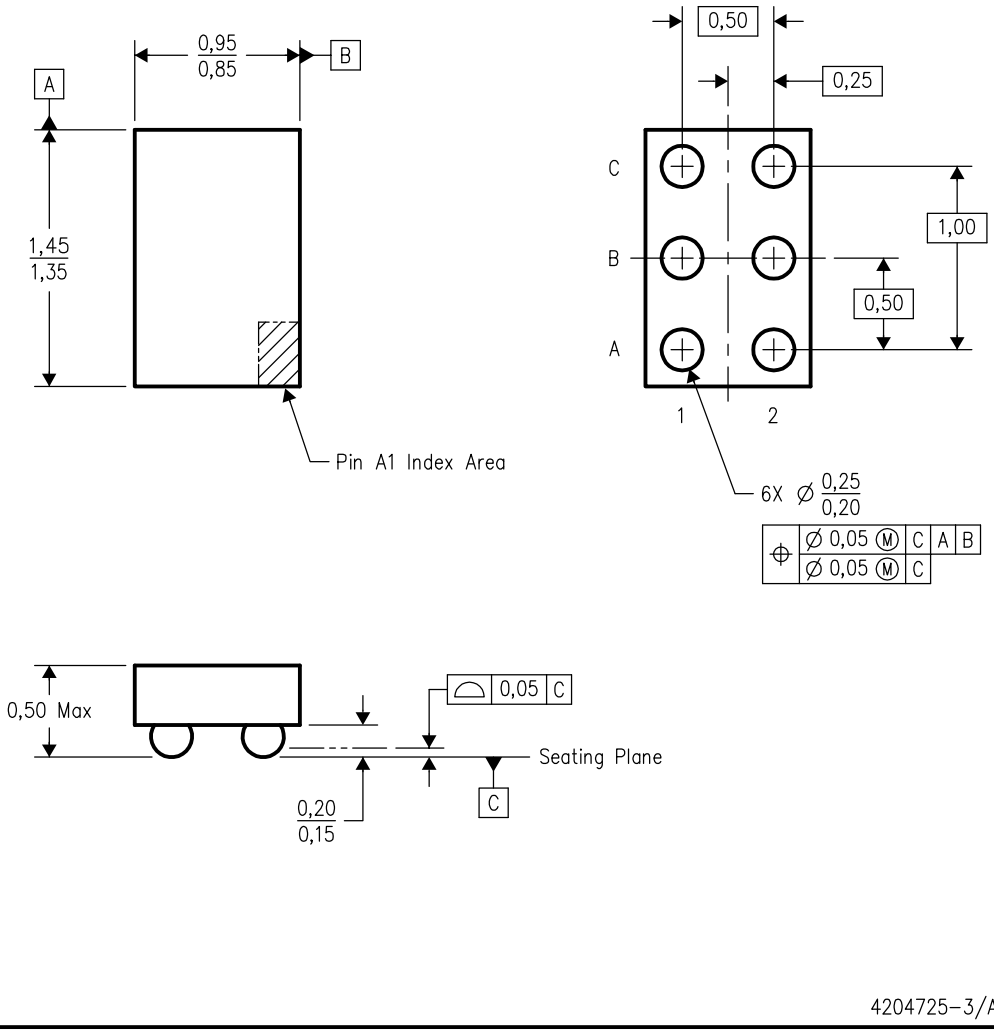


4204741–3/A 10/2002

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is lead–free. Refer to the 6 YEP package (drawing 4204725) for tin–lead (SnPb).

NanoFree is a trademark of Texas Instruments.

YEP (R–XBGA–N6) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. This package is tin–lead (SnPb). Refer to the 6 YZP package (drawing 4204741) for lead–free.

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