GPS Chip Set for Mobile, Navigation and Multimedia Applications

Atmel's chip set for highly optimized low-power GPS modules is highly integrated, thus enabling drastic board space reduction. Comprising an RF receiver IC, a baseband IC and an LNA, it performs a complete GPS receiver optimized for mobile applications, but can also be used for in-vehicle navigation systems. Chip set and GPS modules are a joint development of Atmel (providing the RF IC/digital IC design know-how) and u-blox, providing the GPS system/software know-how.
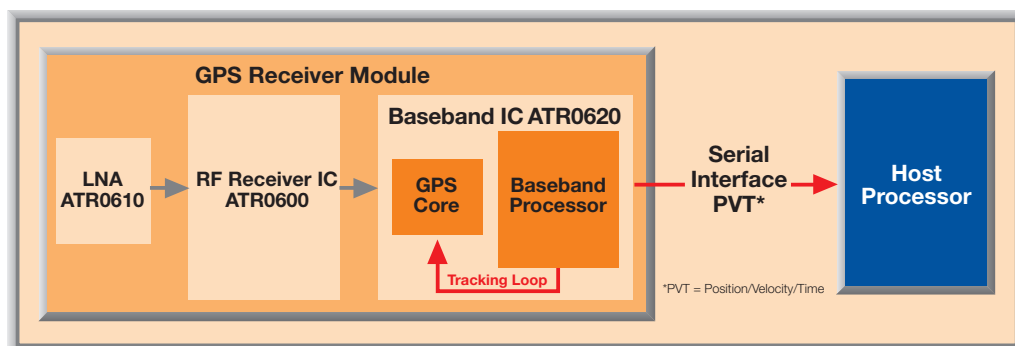
The GPS Chip Set

- Offers Excellent Navigation Accuracy
- Enables Fast Time-to-first-fix
- Is Optimized for Reliable Operation Under Mobile Phone Reception Conditions
- Guarantees Extremely Low Power Consumption (< 100 mW @ 1fix/s)
- Enables Small Form Factors (Required Board Size < 400 mm^2)
- Significantly Reduces BOM and System Costs
- Supports Network-assisted GPS (NA-GPS)

Portable Applications

- Mobile Tracking for All Mobile Phones
- Mobile Tracking for PDAs
- Sports and Recreation (i.e. Outdoor)
- Watches

Automotive Applications

- In-vehicle Navigation
- Fleet Management
- Freight Tracking

GPS Receiver Module

Baseband IC ATR0620

LNA ATR0610 → RF Receiver IC ATR0600 → GPS Core | Baseband Processor

Tracking Loop

Serial Interface PVT* → Host Processor

*PVT = Position/Velocity/Time

GPS RF Receiver IC ATR0600

- Extremely Low Power Consumption (50 mW typically) Due to Single IF Front End Concept
- Excellent Blocking Performance of Nearby GSM Frequencies
- High Integration Level (VCO Tank, Loop Filter and Gain-control Filter on Chip, only one External Low-cost LC Filter Necessary)
- RF LNA Noise Figure < 1.2 dB
- 1.5-Bit ADC on Chip
- UHF6 Technology
- 28 QFN Package (5 x 5 mm)

GPS Baseband IC ATR0620

- High-performance GPS Engine Using a 16-channel GPS Core Driven by an ARM7TDMI® Core on Chip
- Various Interfaces (3 USARTs, SPI Interface, GPIO) for Flexible System Integration
- Low-power Management Enables Maximum Efficiency
- ROM/SRAM on Chip
- 2.3 - 3.6 V or 1.8 V Supply Voltage
- LDO (Low Drop Output) on Chip
- 0.21-CMOS Technology
- 100 BGA Package (9 x 9 mm)

LNA ATR0610

- Excellent Noise Figure (N_{fmin} < 1.6 dB)
- Very Low Power Design (< 10 mW)
- High Gain (> 16 dB)
- Integrated Power-up Control
- Integrated Output Match
- SiGe Technology
- Small PLLP6 Package (1.6 x 2 mm)

GPS Performance

Receiver Type	16 Channels, 8192 Parallel Search Bins, L1 Frequency, C/A Code		
Maximum Update Rate	4 Hz		
Accuracy	Position	3 m CEP	
Start-up Times	Hot Start		2.5 s
	Warm Start		33 s
	Cold Start		41 s
Signal Reacquisition	< 1 s		
Dynamics	< 4 g		

CEP = Circular Error Probability

Low-power module: < 100 mW @ 1 fix/sec
PCB board size: < 400 mm²
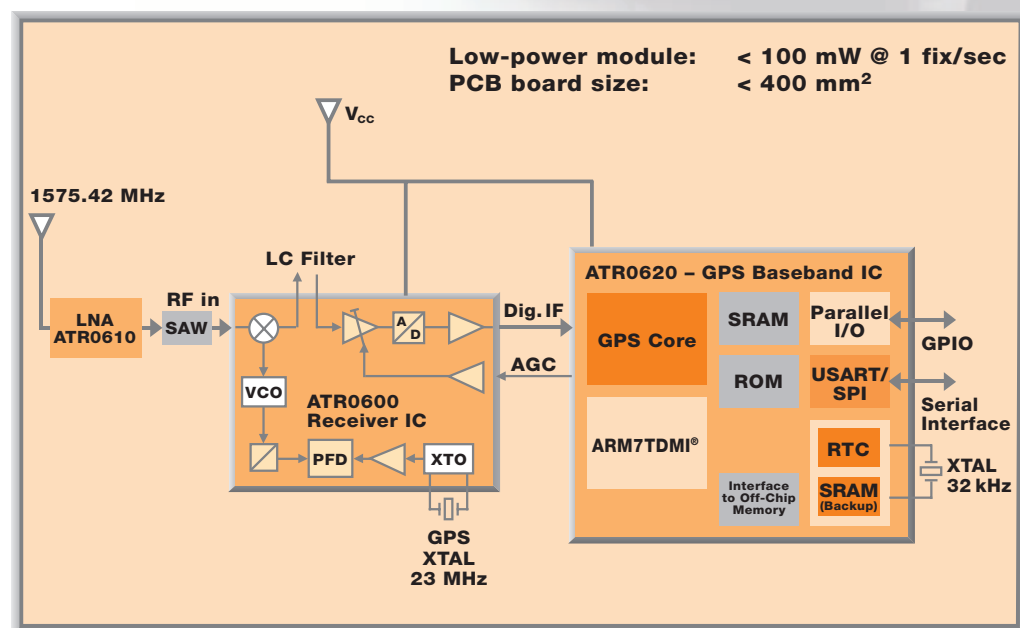
Support

For easy design-in, a complete application-specific support package including extensive GPS software and a highly sophisticated low-power reference design for time-efficient GPS platform development is available.