



DG201B/202B

Vishay Siliconix

Improved Quad CMOS Analog Switches

FEATURES

- $\pm 22\text{-V}$ Supply Voltage Rating
- TTL and CMOS Compatible Logic
- Low On-Resistance— $r_{DS(on)}$: $45\ \Omega$
- Low Leakage— $I_{D(on)}$: $20\ \text{pA}$
- Single Supply Operation Possible
- Extended Temperature Range
- Fast Switching— t_{ON} : $120\ \text{ns}$
- Low Glitching— Q : $1\ \text{pC}$

BENEFITS

- Wide Analog Signal Range
- Simple Logic Interface
- Higher Accuracy
- Minimum Transients
- Reduced Power Consumption
- Superior to DG201A/202
- Space Savings (TSSOP)

APPLICATIONS

- Industrial Instrumentation
- Test Equipment
- Communications Systems
- Disk Drives
- Computer Peripherals
- Portable Instruments
- Sample-and-Hold Circuits

DESCRIPTION

The DG201B/202B analog switches are highly improved versions of the industry-standard DG201A/202. These devices are fabricated in Vishay Siliconix' proprietary silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

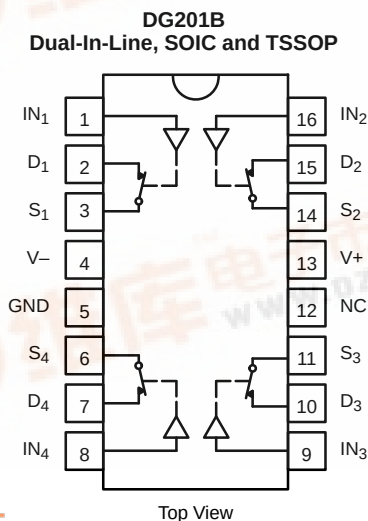
These quad single-pole single-throw switches are designed for a wide variety of applications in telecommunications, instrumentation, process control, computer peripherals, etc. An improved charge injection compensation design minimizes switching transients. The DG201B and DG202B can handle

up to $\pm 22\text{-V}$ input signals, and have an improved continuous current rating of $30\ \text{mA}$. An epitaxial layer prevents latchup.

All devices feature true bi-directional performance in the on condition, and will block signals to the supply voltages in the off condition.

The DG201B is a normally closed switch and the DG202B is a normally open switch. (See Truth Table.)

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	DG201B	DG202B
0	ON	OFF
1	OFF	ON

Logic "0" $\leq 0.8\ \text{V}$
Logic "1" $\geq 2.4\ \text{V}$



ORDERING INFORMATION		
Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG201BDJ
		DG202BDJ
	16-Pin CerDIP	DG201BDK
		DG202BDK
	16-Pin Narrow SOIC	DG201BDY
		DG202BDY
	16-Pin TSSOP	DG201BDQ
		DG202BDQ
-55 to 125°C	16-Pin CerDIP	DG201BAK
		DG201BAK/883
		DG202BAK
		DG202BAK/883

ABSOLUTE MAXIMUM RATINGS

Voltages Referenced to V-

V+ 44 V

GND 25 V

Digital Inputs^a V_S, V_D (V-) -2 V to (V+) +2 V
or 30 mA, whichever occurs first

Current, Any Terminal 30 mA

Peak Current, S or D 100 mA

(Pulsed at 1 ms, 10% duty cycle max)

Storage Temperature (AK, DK Suffix) -65 to 150°C

(DJ, DY, DQ Suffix) -65 to 125°C

Power Dissipation (Package)^b

16-Pin Plastic DIP^c 470 mW

16-Pin Narrow SOIC and TSSOP^d 640 mW

16-Pin CerDIP^e 900 mW

Notes:

a. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.

b. All leads welded or soldered to PC Board.

c. Derate 6.5 mW/°C above 75°C

d. Derate 7.6 mW/°C above 75°C

e. Derate 12 mW/°C above 75°C

SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

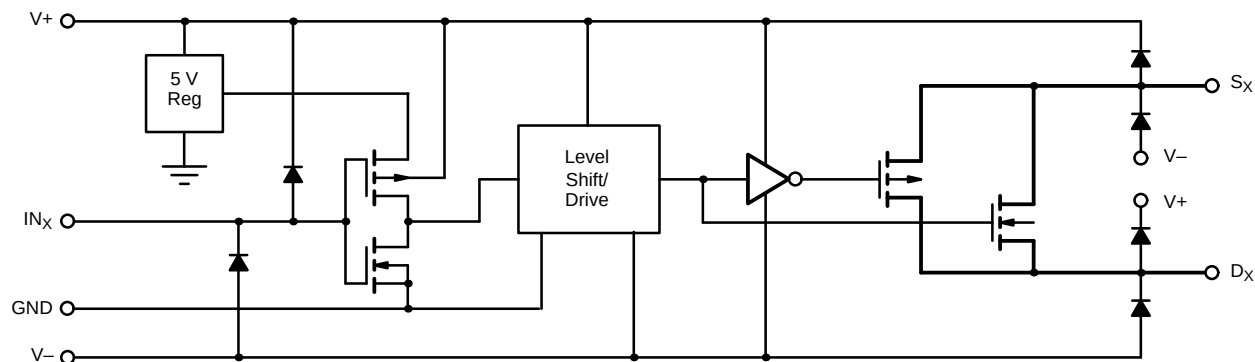


FIGURE 1.



DG201B/202B

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SPECIFICATIONS ^a									
Parameter	Symbol	Test Conditions Unless Specified V ₊ = 15 V, V ₋ = -15 V V _{IN} = 2.4 V, 0.8 V ^f	Temp ^b	Typ ^c	A Suffix -55 to 125°C		D Suffix -40 to 85°C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full		-15	15	-15	15	V
Drain-Source On-Resistance	r _{DS(on)}	V _D = ±10 V, I _S = 1 mA	Room Full	45		85 100		85 100	Ω
r _{DS(on)} Match	Δr _{DS(on)}		Room	2					
Source Off Leakage Current	I _{S(off)}	V _S = ±14 V, V _D = ∓14 V	Room Full	±0.01	-0.5 -20	0.5 20	-0.5 -5	0.5 5	nA
Drain Off Leakage Current	I _{D(off)}	V _D = ±14 V, V _S = ∓14 V	Room Full	±0.01	-0.5 -20	0.5 20	-0.5 -5	0.5 5	
Drain On Leakage Current	I _{D(on)}	V _S = V _D = ±14 V	Room Full	±0.02	-0.5 -40	0.5 40	-0.5 -10	0.5 10	
Digital Control									
Input Voltage High	V _{INH}		Full		2.4		2.4		V
Input Voltage Low	V _{INL}		Full			0.8		0.8	
Input Current	I _{INH} or I _{INL}	V _{INH} or V _{INL}	Full		-1	1	-1	1	μA
Input Capacitance	C _{IN}		Room	5					pF
Dynamic Characteristics									
Turn-On Time	t _{ON}	V _S = 2 V See Switching Time Test Circuit	Room Full	120		300		300	ns
Turn-Off Time	t _{OFF}		Room Full	65		200		200	
Charge Injection	Q	C _L = 1000 pF, V _g = 0 V R _g = 0 Ω	Room	1					pC
Source-Off Capacitance	C _{S(off)}	V _S = 0 V, f = 1 MHz	Room	5					pF
Drain-Off Capacitance	C _{D(off)}		Room	5					
Channel On Capacitance	C _{D(on)}	V _D = V _S = 0 V, f = 1 MHz	Room	16					
Off Isolation	OIRR	C _L = 15 pF, R _L = 50 Ω V _S = 1 V _{RMS} , f = 100 kHz	Room	90					dB
Channel-to-Channel Crosstalk	X _{TALK}		Room	95					
Power Supply									
Positive Supply Current	I ₊	V _{IN} = 0 or 5 V	Room Full			50 100		50 100	μA
Negative Supply Current	I ₋		Room Full		-1 -5		-1 -5		
Power Supply Range for Continuous Operation	V _{OP}		Full		±4.5	±22	±4.5	±22	V

DG201B/202B

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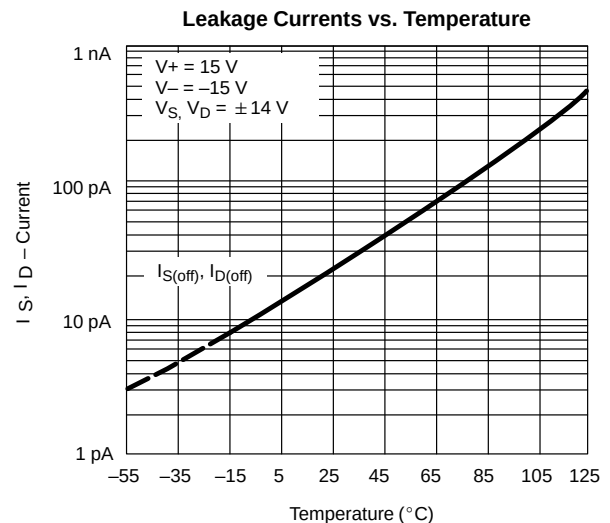
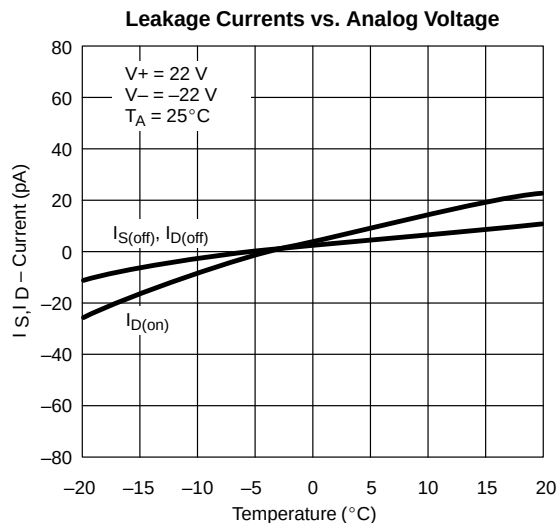
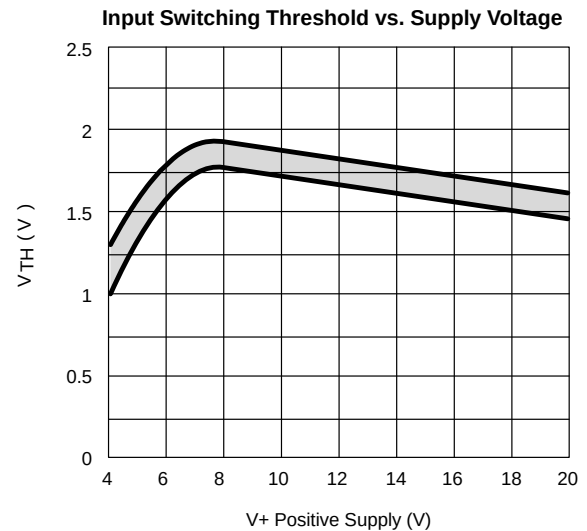
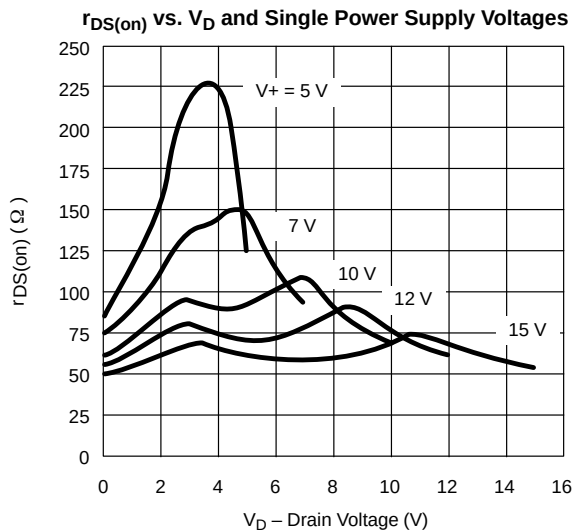
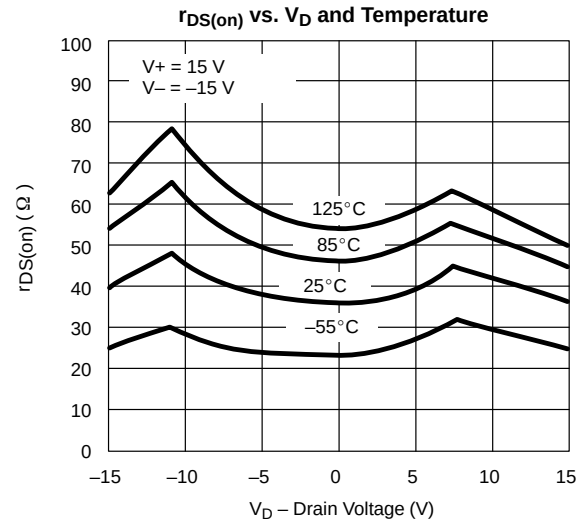
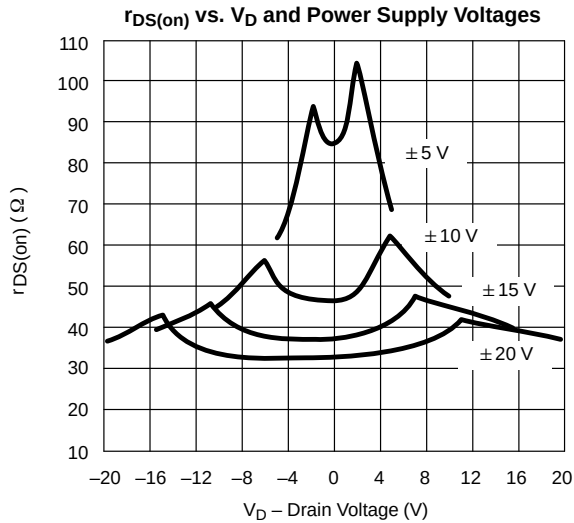
SPECIFICATIONS FOR SINGLE SUPPLY ^a									
Parameter	Symbol	Test Conditions Unless Specified V ⁺ = 12 V, V [–] = 0 V V _{IN} = 2.4 V, 0.8 V ^f	Temp ^b	Typ ^c	A Suffix –55 to 125°C		D Suffix –40 to 85°C		Unit
					Min ^d	Max ^d	Min ^d	Max ^d	
Analog Switch									
Analog Signal Range ^e	V _{ANALOG}		Full		0	12	0	12	V
Drain-Source On-Resistance	r _{DS(on)}	V _D = 3 V, 8 V, I _S = 1 mA	Room Full	90		160 200		160 200	Ω
Dynamic Characteristics									
Turn-On Time	t _{ON}	V _S = 8 V See Switching Time Test Circuit	Room	120		300		300	ns
Turn-Off Time	t _{OFF}		Room	60		200		200	
Charge Injection	Q	C _L = 1 nF, V _{gen} = 6 V, R _{gen} = 0 Ω	Room	4					pC
Power Supply									
Positive Supply Current	I ⁺	V _{IN} = 0 or 5 V	Room Full			50 100		50 100	μA
Negative Supply Current	I [–]		Room Full		–1 –5		–1 –5		
Power Supply Range for Continuous Operation	V _{OP}		Full		+4.5	+25	+4.5	+25	V

Notes:

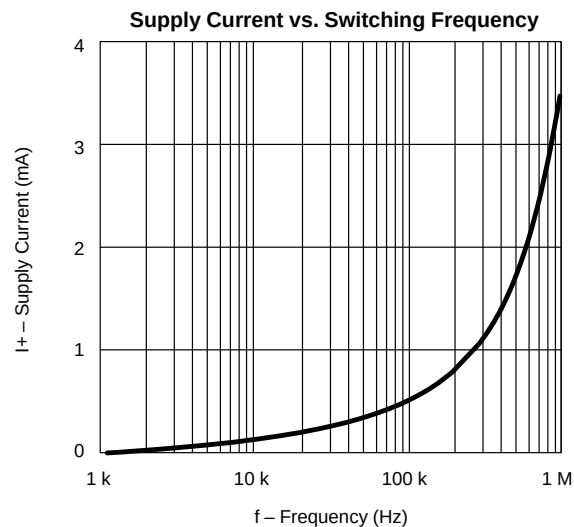
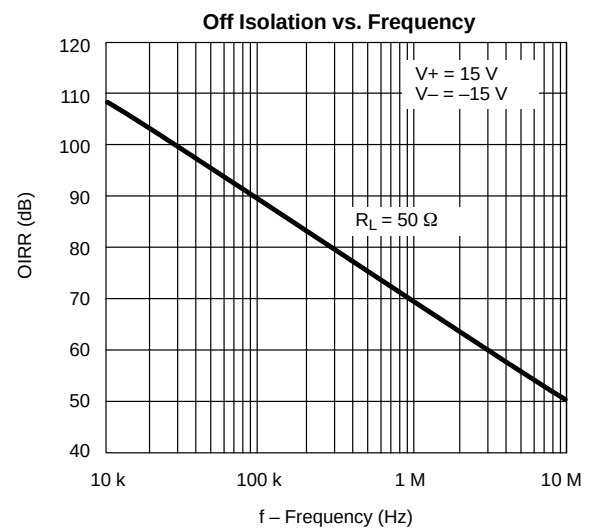
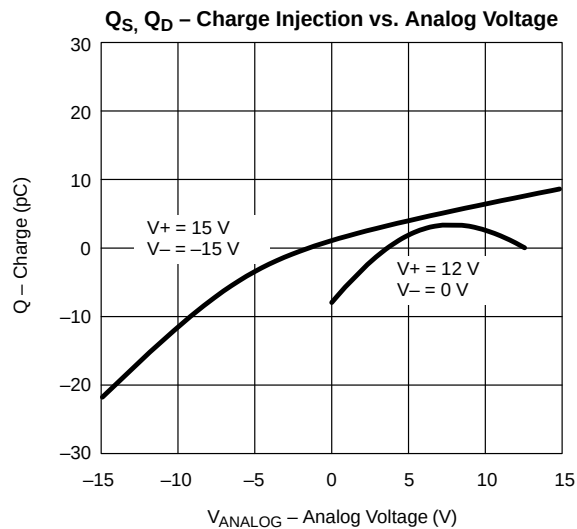
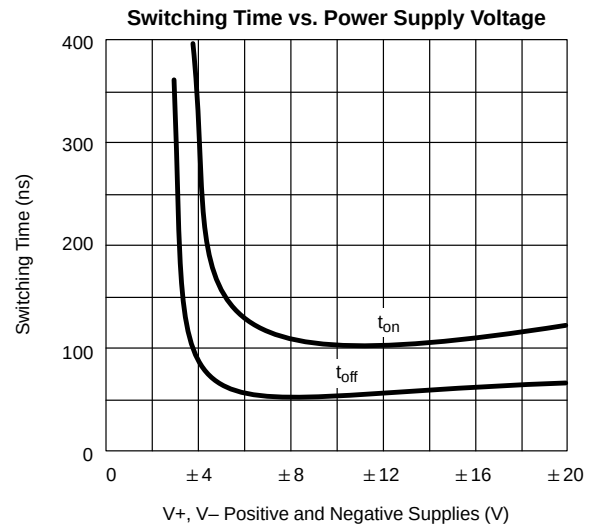
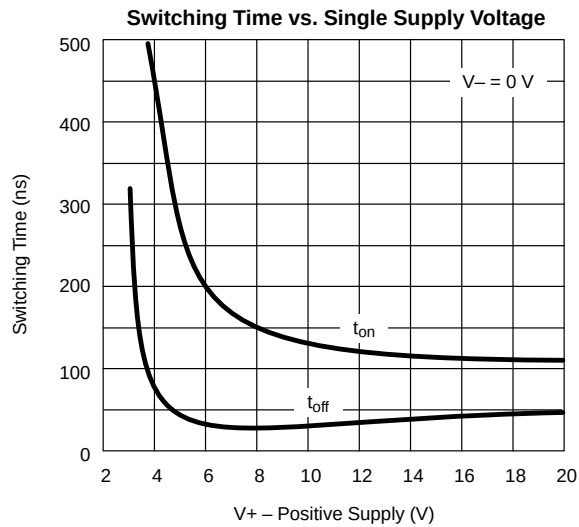
- Refer to PROCESS OPTION FLOWCHART.
- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





TEST CIRCUITS

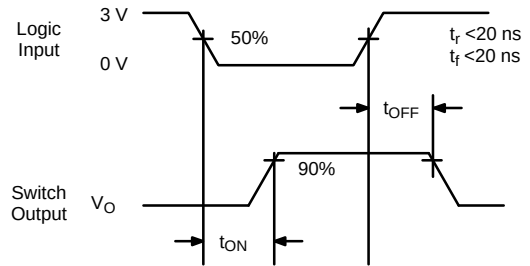
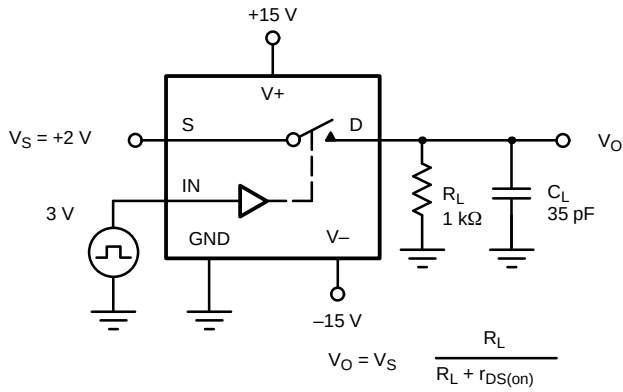


FIGURE 2. Switching Time

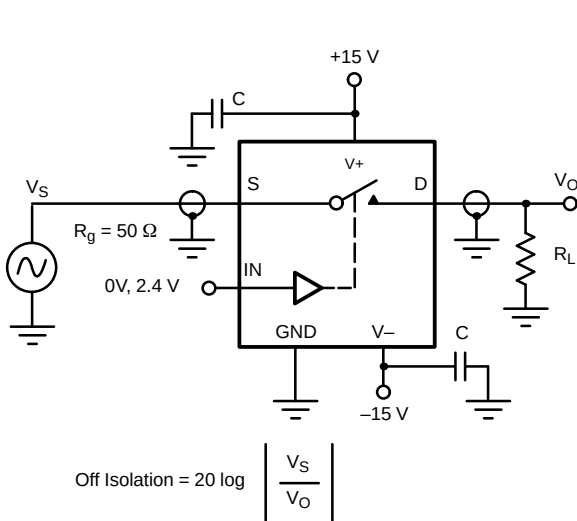


FIGURE 3. Off Isolation

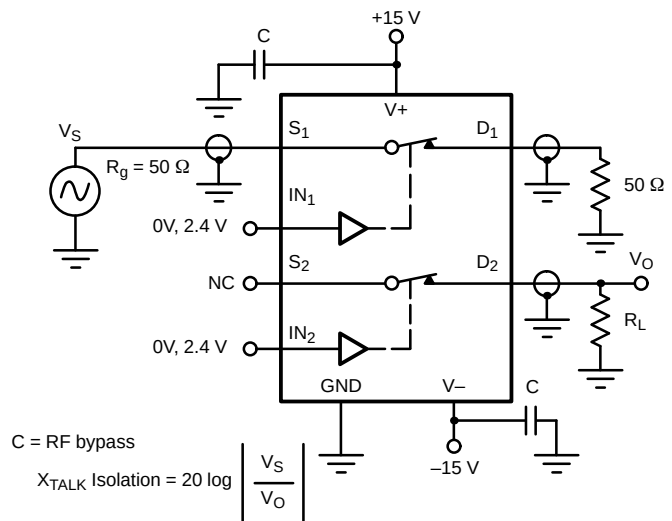
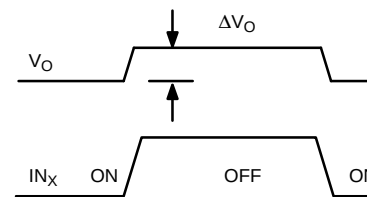
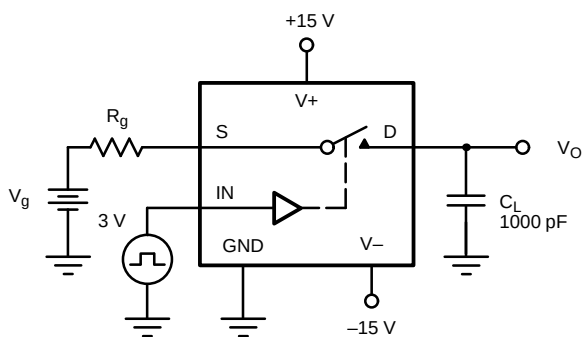


FIGURE 4. Channel-to-Channel Crosstalk



ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is $Q = C_L \times \Delta V_O$

FIGURE 5. Charge Injection

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APPLICATIONS

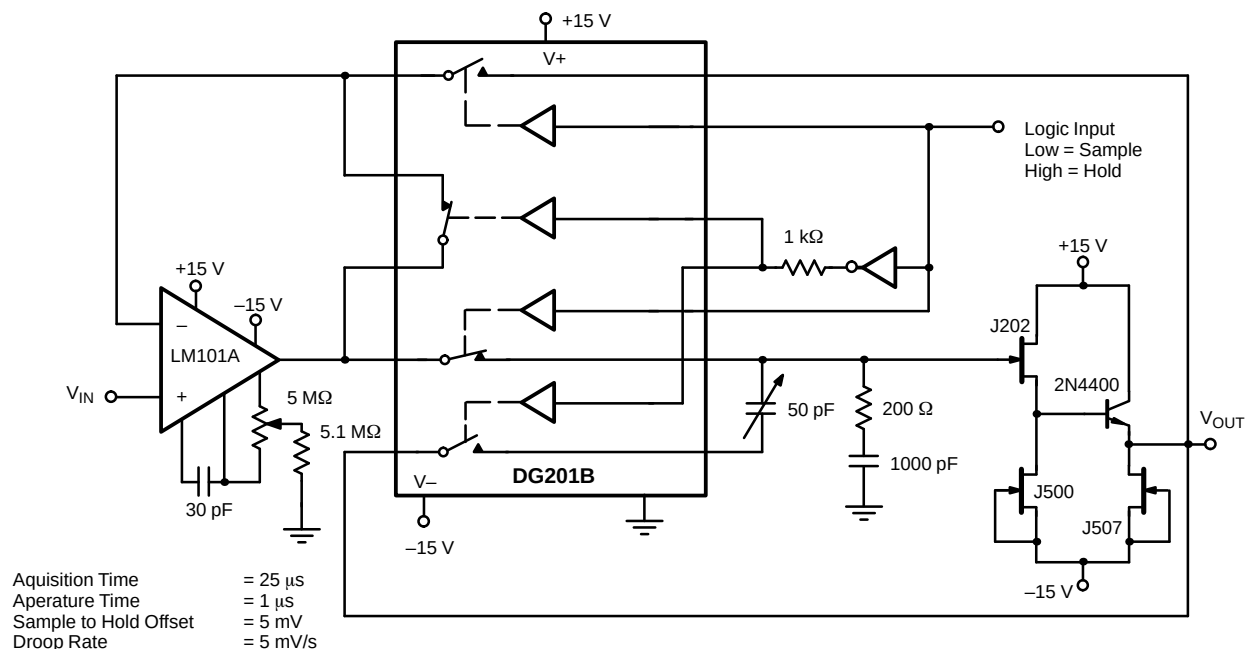
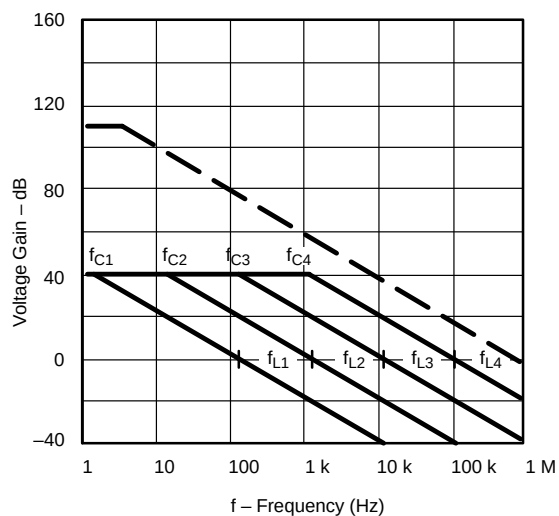
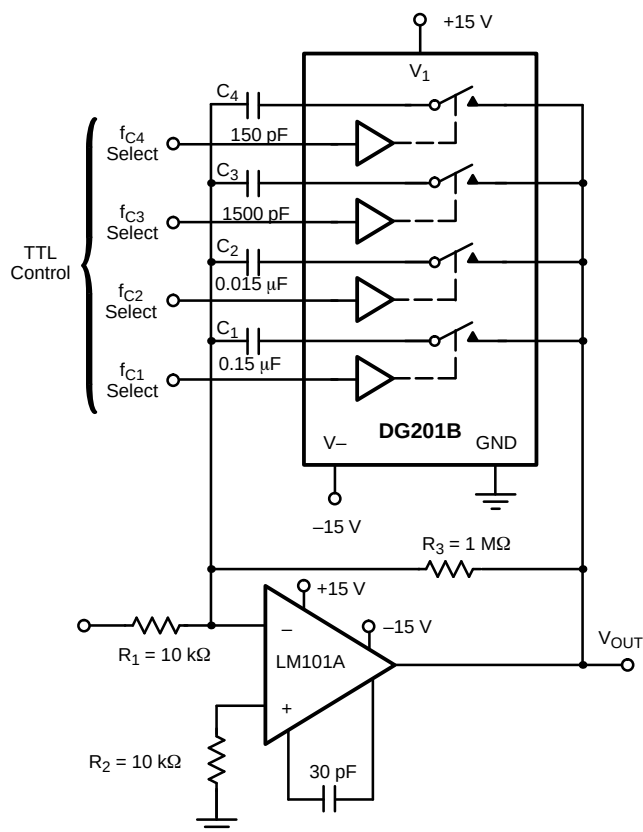


FIGURE 6. Sample-and-Hold



$$A_L \text{ (Voltage Gain Below Break Frequency)} = \frac{R_3}{R_1} = 100 \text{ (40 dB)}$$

$$f_C \text{ (Break Frequency)} = \frac{1}{2\pi R_3 C_X}$$

$$f_L \text{ (Unity Gain Frequency)} = \frac{1}{2\pi R_1 C_X}$$

$$\text{Max Attenuation} = \frac{f_{DS(on)}}{10 \text{ k}\Omega} \approx -47 \text{ dB}$$

FIGURE 7. Active Low Pass Filter with Digitally Selected Break Frequency



APPLICATIONS

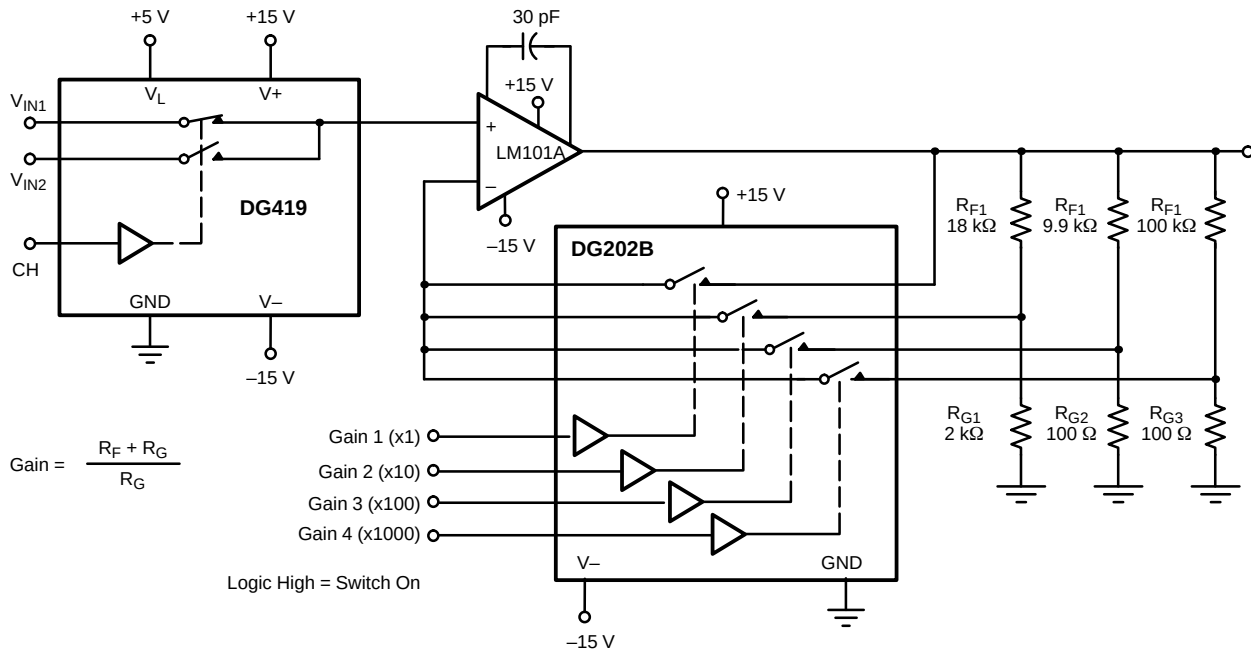


FIGURE 8. A Precision Amplifier with Digitally Programmable Input and Gains