19-4728; Rev 3; 9/99

MAXIM

Improved, Quad, SPST Analog Switches

General Description

Maxim's redesigned DG411/DG412/DG413 analog switches now feature low on-resistance matching between switches (3Ω max) and guaranteed on-resistance flatness over the signal range (Δ4Ω max). These low on-resistance switches conduct equally well in either direction. They guarantee low charge injection, low power consumption, and an ESD tolerance of 2000V minimum per Method 3015.7. The new design offers lower off leakage current over temperature (less than 5nA at +85°C).

The DG411/DG412/DG413 are quad, single-pole/single-throw (SPST) analog switches. The DG411 is normally closed (NC), and the DG412 is normally open (NO). The DG413 has two NC switches and two NO switches. Switching times are less than 150ns max for t_{ON} and less than 100ns max for t_{OFF}. These devices operate from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies. Maxim's improved DG411/DG412/DG413 are fabricated with a 44V silicon-gate process.

Applications

- Sample-and-Hold Circuits
- Test Equipment
- Heads-Up Displays
- Guidance & Control Systems
- Military Radios
- Communication Systems
- Battery-Operated Systems
- PBX, PABX
- Audio Signal Routing

New Features

- **Plug-In Upgrade for Industry-Standard DG411/DG412/DG413**
- **Improved $r_{DS(ON)}$ Match Between Channels (3Ω max)**
- **Guaranteed $r_{FLAT(ON)}$ Over Signal Range (Δ4Ω)**
- **Improved Charge Injection (10pC max)**
- **Improved Off Leakage Current Over Temperature (<5nA at +85°C)**
- **Withstand Electrostatic Discharge (2000V min) per Method 3015.7**

Existing Features

- **Low $r_{DS(ON)}$ (35Ω max)**
- **Single-Supply Operation +10V to +30V**
- **Bipolar-Supply Operation ±4.5V to ±20V**
- **Low Power Consumption (35µW max)**
- **Rail-to-Rail Signal Handling**
- **TTL/CMOS-Logic Compatible**

Ordering Information

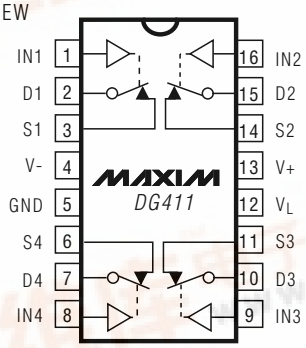
PART	TEMP. RANGE	PIN-PACKAGE
DG411CJ	0°C to +70°C	16 Plastic DIP
DG411CUE	0°C to +70°C	16 TSSOP
DG411CY	0°C to +70°C	16 Narrow SO
DG411C/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

**Contact factory for dice specifications.*

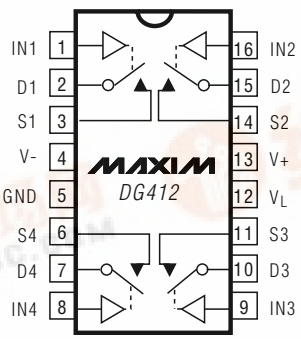
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



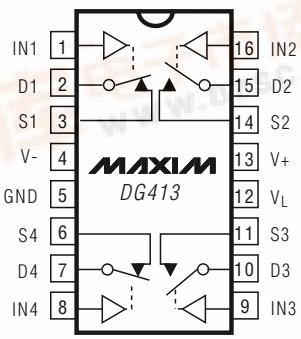
DIP/SO/TSSOP

DG411	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO/TSSOP

DG412	
LOGIC	SWITCH
0	OFF
1	ON



DIP/SO/TSSOP

DG413		
LOGIC	SWITCHES 1, 4	SWITCHES 2, 3
0	OFF	ON
1	ON	OFF

SWITCHES SHOWN FOR LOGIC "0" INPUT

Improved, Quad, SPST Analog Switches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
V_L ..... (GND -0.3V) to (V+ +0.3V)
Digital Inputs, V_S, V_D (Note 1) ..... (V- -2V) to (V+ +2V) or 30mA (whichever occurs first)
Continuous Current (any terminal) 30mA
Peak Current
(pulsed at 1ms, 10% duty cycle max) 100mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) .842mW
16-Pin Narrow SO (derate 8.70mW/°C above +70°C) ...696mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) 800mW
16-Pin TSSOP (derate 6.7mW/°C above +70°C) 457mW
Operating Temperature Ranges
DG41_C_ ..... 0°C to +70°C
DG41_D_ ..... -40°C to +85°C
DG41_AK_ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP (Note 2)	MAX	UNITS
SWITCH								
Analog Signal Range	V_{ANALOG}	(Note 3)			-15		15	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V+ = 13.5V, V- = -13.5V, V_D = ±8.5V, I_S = -10mA	T_A = +25°C	C, D		17	45	Ω
				A		17	30	
			T_A = T_{MIN} to T_{MAX}				45	
On-Resistance Match Between Channels (Note 4)	$\Delta r_{DS(ON)}$	V+ = 15V, V- = -15V, V_D = ±10V, I_S = -10mA	T_A = +25°C				3	Ω
			T_A = T_{MIN} to T_{MAX}				5	
On-Resistance Flatness (Note 4)	$r_{FLAT(ON)}$	V+ = 15V, V- = -15V, V_D = ±5V, 0V, I_S = -10mA	T_A = +25°C				4	Ω
			T_A = T_{MIN} to T_{MAX}				6	
Source-Off Leakage Current (Note 7)	$I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	T_A = +25°C	C, D, A	-0.25	-0.10	0.25	nA
			T_A = T_{MIN} to T_{MAX}	C, D	-5		5	
				A	-10		10	
Drain-Off Leakage Current (Note 7)	$I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	T_A = +25°C	C, D, A	-0.25	-0.10	0.25	nA
			T_A = T_{MIN} to T_{MAX}	C, D	-5		5	
				A	-10		10	
Drain-On Leakage Current (Note 7)	$I_{D(ON)}$ + $I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	T_A = +25°C	C, D, A	-0.4	-0.1	0.4	nA
			T_A = T_{MIN} to T_{MAX}	C, D	-20		20	
				A	-40		40	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = 15V, V- = -15V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
INPUT							
Input Current with Input Voltage High	I_{INH}	IN = 2.4V, all others = 0.8V		-0.500	0.005	0.500	µA
Input Current with Input Voltage Low	I_{INL}	IN = 0.8V, all others = 2.4V		-0.500	0.005	0.500	µA
SUPPLY							
Power-Supply Range				±4.5		±20.0	V
Positive Supply Current	I+	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Negative Supply Current	I-	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Logic Supply Current	I_L	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
DYNAMIC							
Turn-On Time	t_{ON}	V_D = ±10V, Figure 2	T_A = +25°C		110	175	ns
			T_A = T_{MIN} to T_{MAX}			220	
Turn-Off Time	t_{OFF}	V_D = ±10V, Figure 2	T_A = +25°C		100	145	ns
			T_A = T_{MIN} to T_{MAX}			160	
Break-Before-Make Time Delay	t_D	DG413 only, R_L = 300Ω, C_L = 35pF, Figure 3	T_A = +25°C		25		ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{GEN} = 0V, R_{GEN} = 0Ω, Figure 4	T_A = +25°C		5	10	pC
Off Isolation (Note 5)	OIRR	R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 5	T_A = +25°C		68		dB
Crosstalk (Note 6)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 6	T_A = +25°C		85		dB
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, Figure 7	T_A = +25°C		9		pF
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, Figure 7	T_A = +25°C		9		pF
Drain-On Capacitance	$C_{D(ON)}$ + $C_{S(ON)}$	f = 1MHz, Figure 8	T_A = +25°C		35		pF

Improved, Quad, SPST Analog Switches

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = 12V, V- = 0V, V_L = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
SWITCH							
Analog Signal Range	V_{ANALOG}	(Note 3)		0		12	V
Drain-Source On Resistance	$r_{DS(ON)}$	V+ = 10.8V, V_D = 3.8V, I_S = -10mA	T_A = +25°C		40	80	Ω
			T_A = T_{MIN} to T_{MAX}			100	
SUPPLY							
Positive Supply Current	I+	All channels on or off, V+ = 13.2V, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MAX}	-5		5	
Negative Supply Current	I-	All channels on or off, V+ = 13.2V, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MAX}	-5		5	
Logic Supply Current	I_L	All channels on or off, V_L = 5.25V, V_{IN} = 0V or 5V	T_A = +25°C	-1	0.0001	1	µA
			T_A = T_{MAX}	-5		5	
Ground Current	I_{GND}	All channels on or off, V_L = 5.25V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MAX}	-5		5	
DYNAMIC							
Turn-On Time	t_{ON}	V_S = 8V, Figure 2	T_A = +25°C		175	250	ns
			T_A = T_{MIN} to T_{MAX}			315	
Turn-Off Time	t_{OFF}	V_S = 8V, Figure 2	T_A = +25°C		95	125	ns
			T_A = T_{MIN} to T_{MAX}			140	
Break-Before-Make Time Delay	t_D	DG413 only, R_L = 300Ω, C_L = 35pF, Figure 3	T_A = +25°C		25		ns
Charge Injection (Note 3)	Q	C_L = 1.0nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 4	T_A = +25°C		5	10	pC

Note 2: The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: $\Delta R_{ON} = \Delta R_{ON}$ max - ΔR_{ON} min. On-resistance match between channels and flatness are guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and minimum value of on resistance as measured at the extremes of the specified analog signal range.

Note 5: Off Isolation = 20 log (V_D/V_S), V_D = output, V_S = input to off switch. See Figure 5.

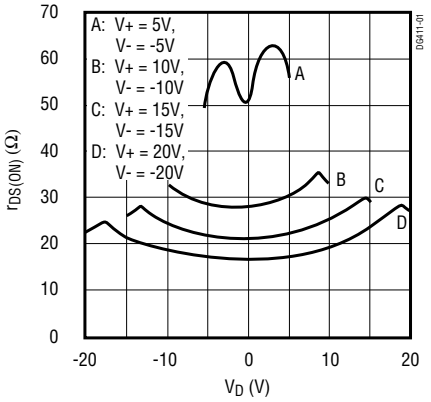
Note 6: Between any two switches. See Figure 6.

Note 7: Leakage parameters $I_{S(OFF)}$, $I_{D(OFF)}$, and $I_{D(ON)}$ are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

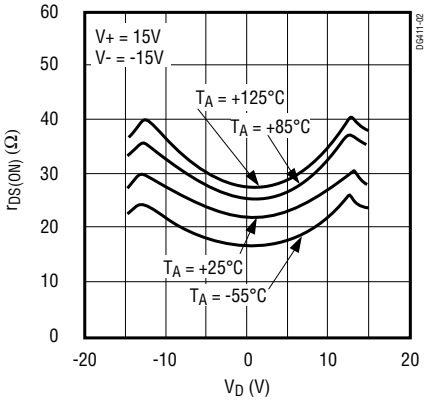
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

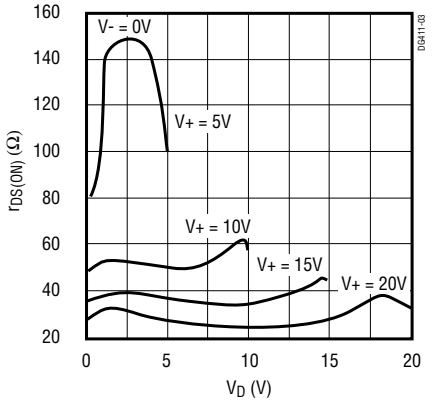
ON-RESISTANCE vs. V_D AND POWER-SUPPLY VOLTAGE



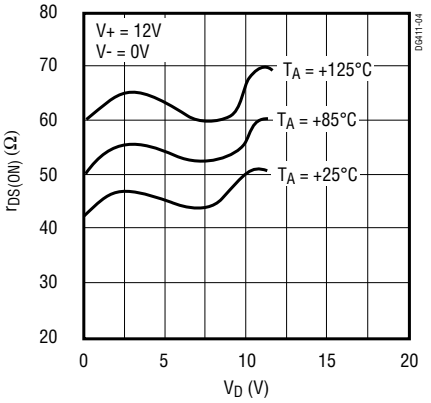
ON-RESISTANCE vs. V_D AND TEMPERATURE



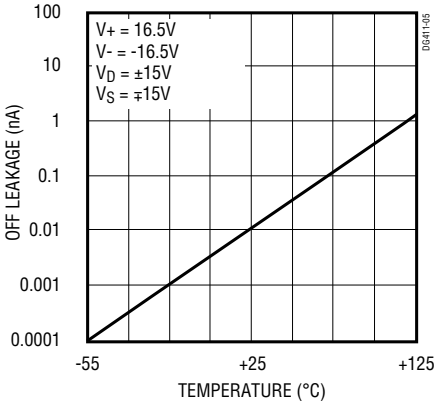
ON-RESISTANCE vs. V_D AND TEMPERATURE (SINGLE SUPPLY)



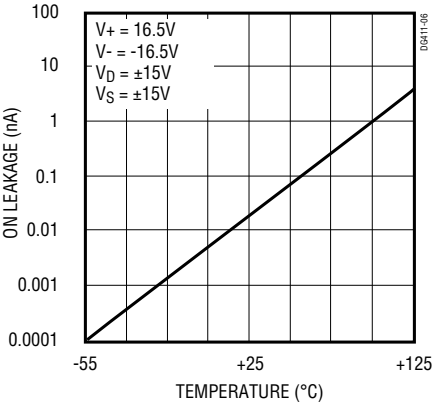
ON-RESISTANCE vs. V_D (SINGLE SUPPLY)



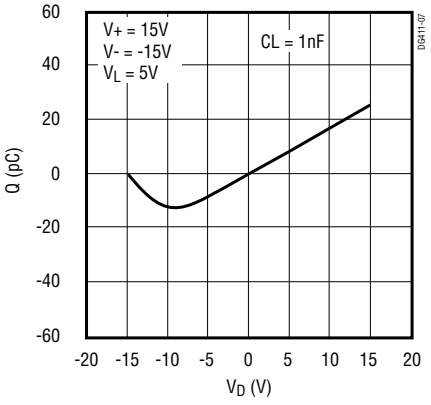
OFF LEAKAGE CURRENTS vs. TEMPERATURE



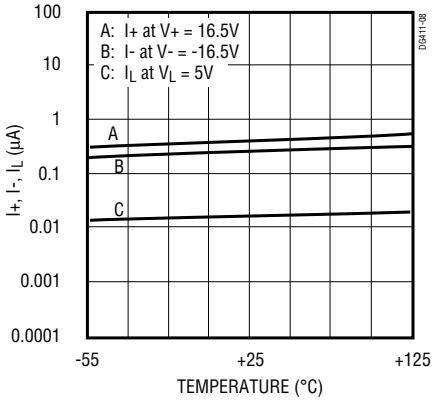
ON LEAKAGE CURRENTS vs. TEMPERATURE



CHARGE INJECTION vs. ANALOG VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



Improved, Quad, SPST Analog Switches

Pin Description

PIN	NAME	FUNCTION
1, 16, 9, 8	IN1-IN4	Inputs
2, 15, 10, 7	D1-D4	Analog-Switch Drain Terminal
3, 14, 11, 6	S1-S4	Analog-Switch Source Terminal
4	V-	Negative Supply-Voltage Input
5	GND	Ground
12	V_L	Logic Supply Voltage
13	V+	Positive Supply-Voltage Input—connected to substrate

Applications Information

Operation with Supply Voltages Other Than 15V

Using supply voltages other than 15V will reduce the analog signal range. The DG411/DG412/DG413 switches operate with ±4.5V to ±20V bipolar supplies or with a +10V to +30V single supply; connect V- to 0V when operating with a single supply. Also, all device types can operate with unbalanced supplies such as +24V and -5V. V_L must be connected to +5V to be TTL compatible, or to V+ for CMOS-logic level inputs. The *Typical Operating Characteristics* graphs show typical on-resistance with ±15V, ±10V, and ±5V supplies. (Switching times increase by a factor of two or more for operation at ±5V.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by V_L, V-, and logic inputs. If power-supply sequencing is not possible, add two small, external signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V below V+ and 1V below V-, without affecting low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed +44V.

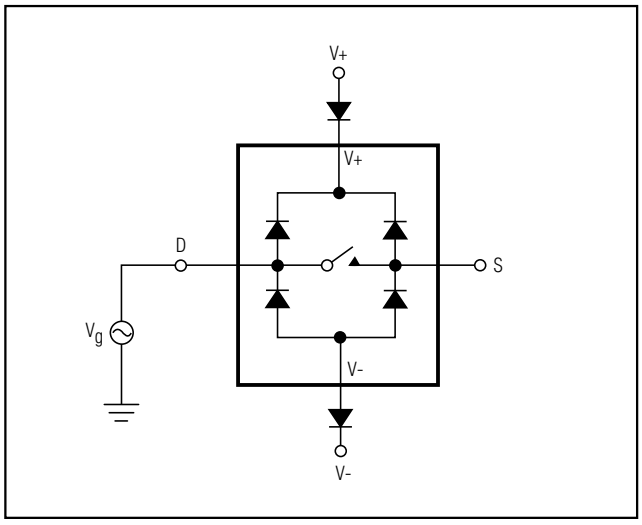


Figure 1. Overvoltage Protection Using External Blocking Diodes

Timing Diagrams/Test Circuits

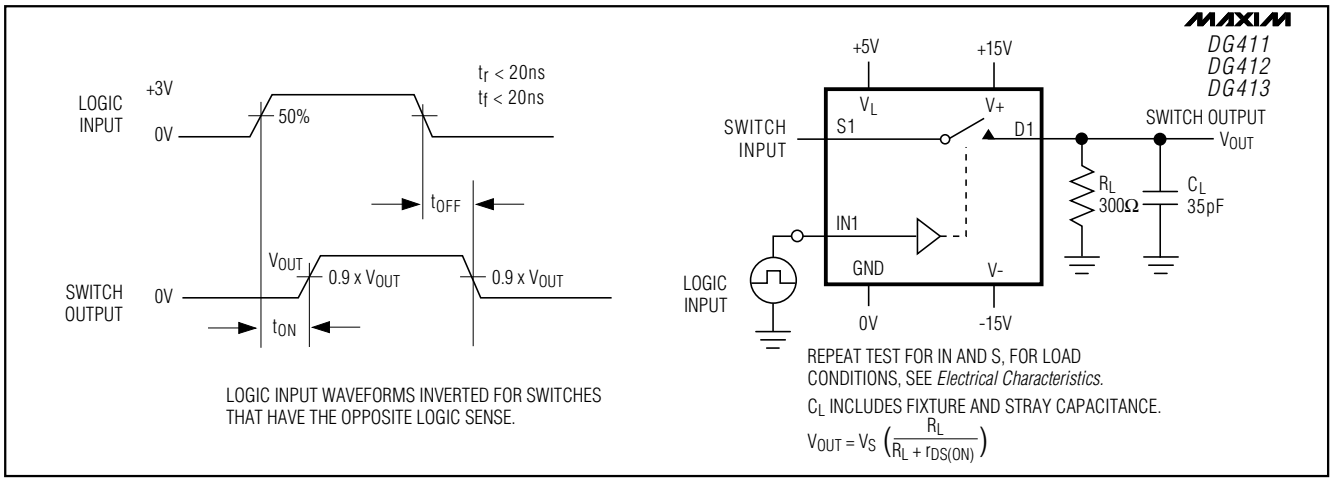


Figure 2. Switching-Time

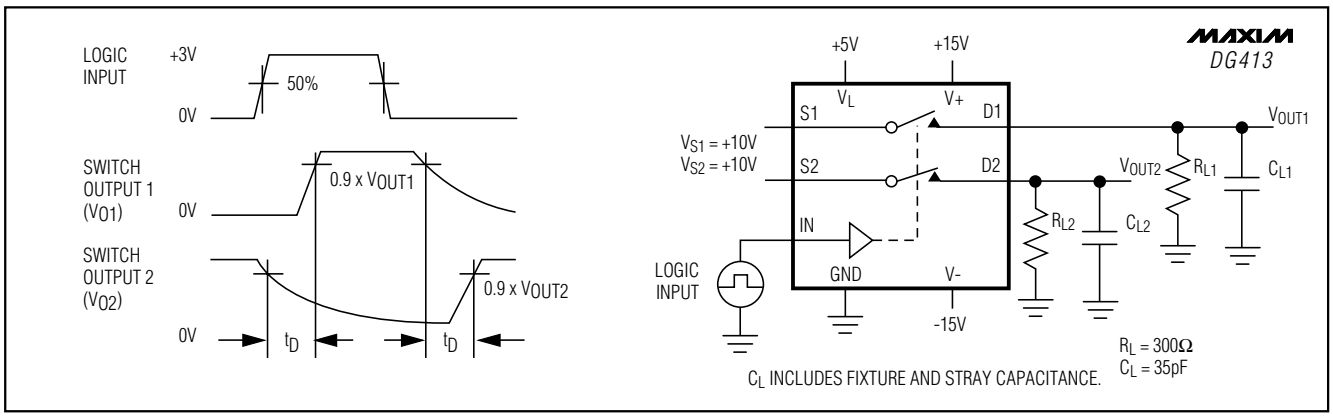


Figure 3. DG413 Break-Before-Make

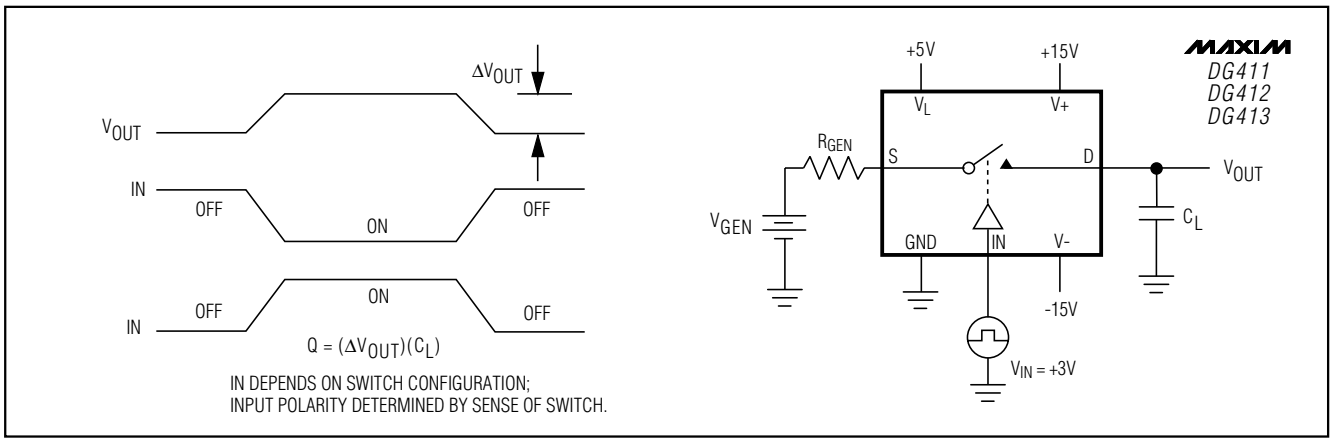


Figure 4. Charge-Injection

Improved, Quad, SPST Analog Switches

Timing Diagrams/Test Circuits (continued)

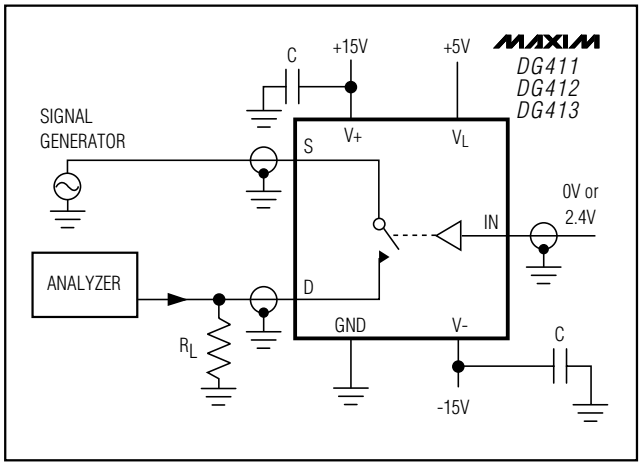


Figure 5. Off-Isolation

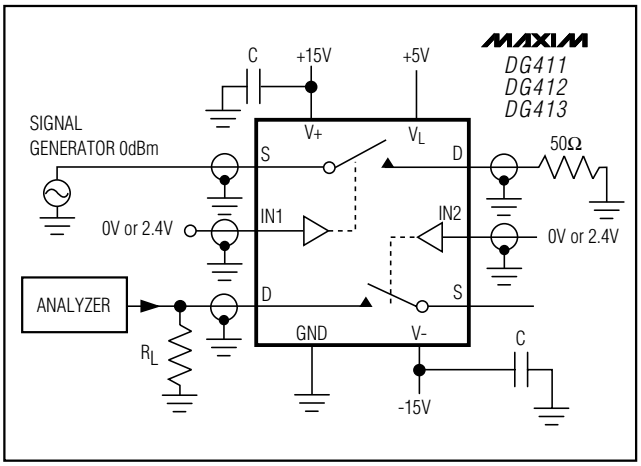


Figure 6. Crosstalk

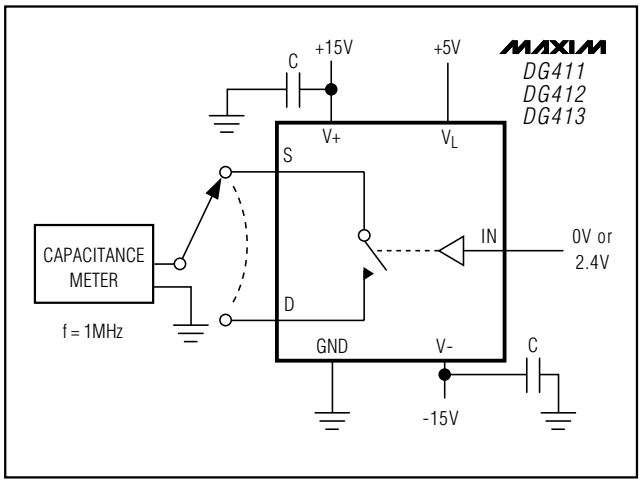


Figure 7. Channel-Off Capacitance

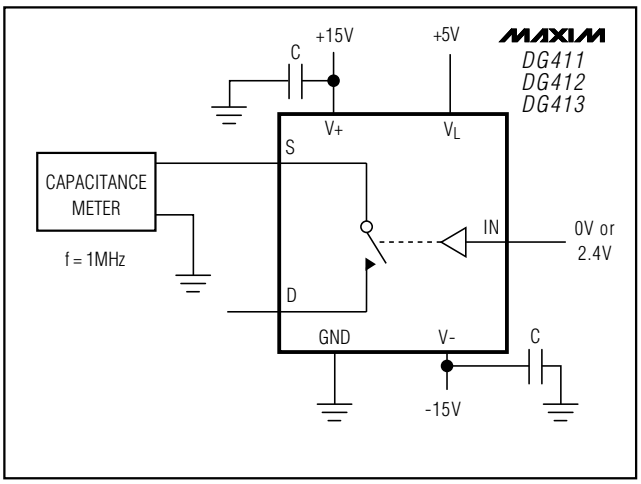


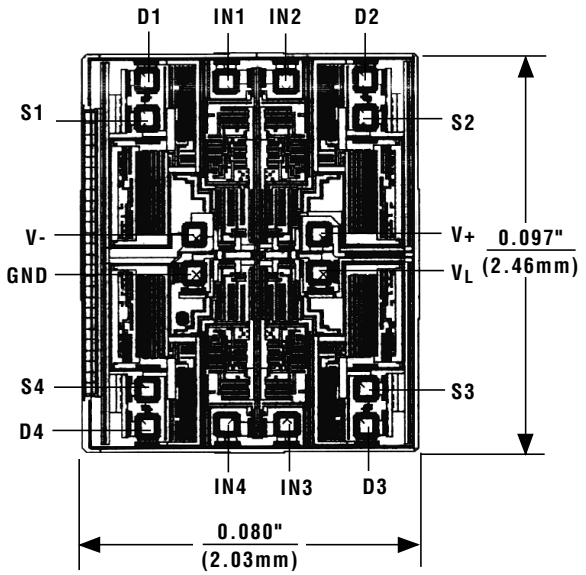
Figure 8. Channel-On Capacitance

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
DG411DJ	-40°C to +85°C	16 Plastic DIP
DG411DY	-40°C to +85°C	16 Narrow SO
DG411DK	-40°C to +85°C	16 CERDIP
DG411AK	-55°C to +125°C	16 CERDIP**
DG412CJ	0°C to +70°C	16 Plastic DIP
DG412CUE	0°C to +70°C	16 TSSOP
DG412CY	0°C to +70°C	16 Narrow SO
DG412C/D	0°C to +70°C	Dice*
DG412DJ	-40°C to +85°C	16 Plastic DIP
DG412DY	-40°C to +85°C	16 Narrow SO
DG412DK	-40°C to +85°C	16 CERDIP
DG412AK	-55°C to +125°C	16 CERDIP**
DG413CJ	0°C to +70°C	16 Plastic DIP
DG413CUE	0°C to +70°C	16 TSSOP
DG413CY	0°C to +70°C	16 Narrow SO
DG413C/D	0°C to +70°C	Dice*
DG413DJ	-40°C to +85°C	16 Plastic DIP
DG413DY	-40°C to +85°C	16 Narrow SO
DG413DK	-40°C to +85°C	16 CERDIP
DG413AK	-55°C to +125°C	16 CERDIP**

** Contact factory for dice specifications.*
***Contact factory for availability and processing to MIL-STD-883B.*

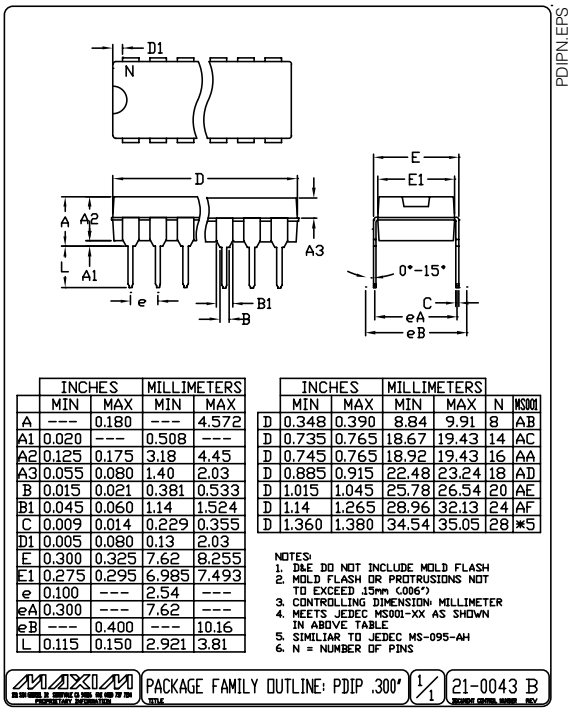
Chip Topography



TRANSISTOR COUNT: 136
SUBSTRATE CONNECTED TO V+

Improved, Quad, SPST Analog Switches

Package Information



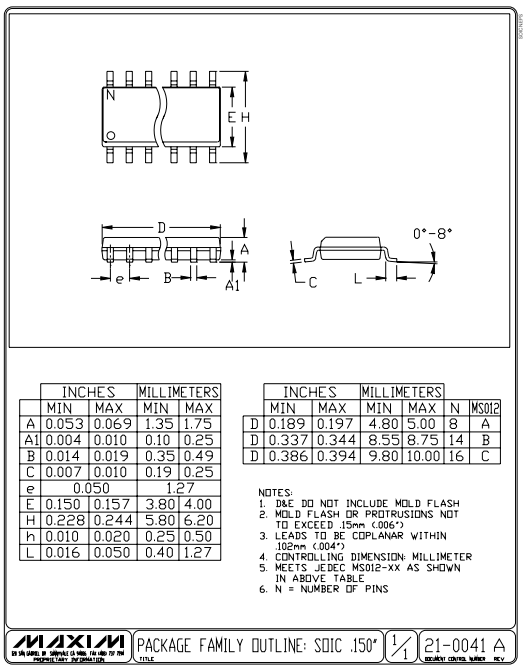
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.020	---	0.508	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.021	0.381	0.533
B1	0.045	0.060	1.14	1.524
C	0.009	0.014	0.229	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.255
E1	0.275	0.295	6.985	7.493
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MS-095-AH
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 B

Package Information (continued)

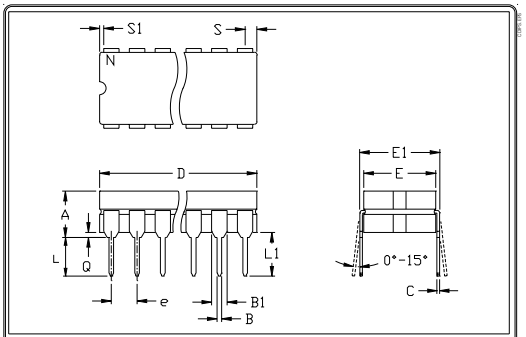


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | 21-0041 A



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	---	0.00	---
Q	0.015	0.070	0.38	1.78
S	---	0.098	---	2.49
S1	0.005	---	0.13	---

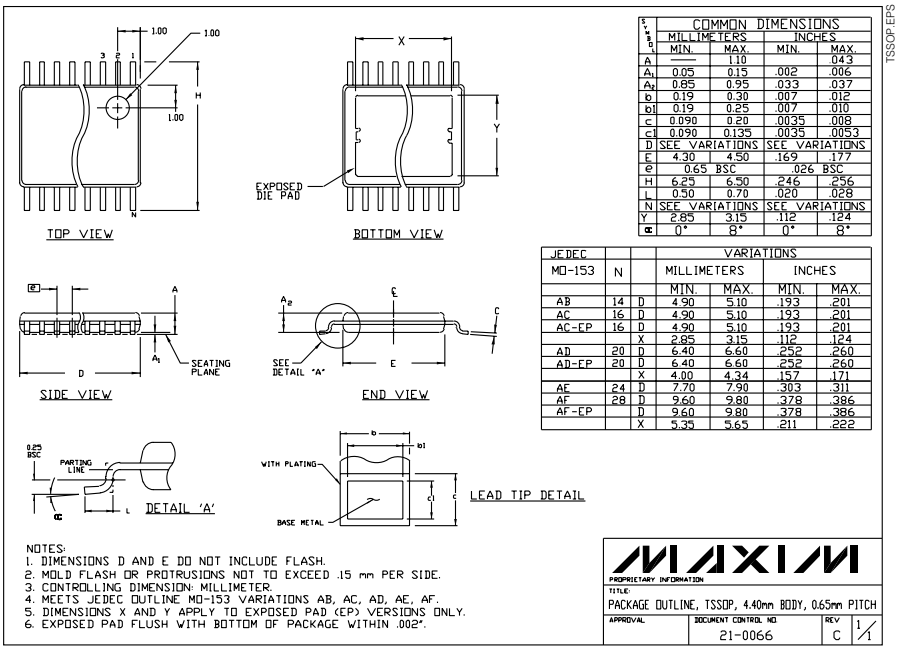
	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	0.405	---	10.29	8	P:D4
D	---	0.785	---	19.94	14	C:D1
D	---	0.840	---	21.34	16	E:D2
D	---	0.960	---	24.38	18	V:D6
D	---	1.060	---	26.92	20	R:D8
D	---	1.280	---	32.51	24	L:D9

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #1 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: CDIP .300" | 1/1 | 21-0045 A

Improved, Quad, SPST Analog Switches

Package Information (continued)



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	———	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b1	0.19	0.25	.007	.010
c	0.090	0.20	.0035	.008
c1	0.090	0.135	.0035	.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.50	.246	.256
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	.112	.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
AB	14	D	4.90	5.10	.193	.201
AC	16	D	4.90	5.10	.193	.201
AC-EP	16	D	4.90	5.10	.193	.201
		X	2.85	3.15	.112	.124
AD	20	D	6.40	6.60	.252	.260
AD-EP	20	D	6.40	6.60	.252	.260
		X	4.00	4.34	.157	.171
AE	24	D	7.70	7.90	.303	.311
AF	28	D	9.60	9.80	.378	.386
AF-EP		D	9.60	9.80	.378	.386
		X	5.35	5.65	.211	.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15 mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETER.
4. MEETS JEDEC OUTLINE MO-153 VARIATIONS AB, AC, AD, AE, AF.
5. DIMENSIONS X AND Y APPLY TO EXPOSED PAD (EP) VERSIONS ONLY.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".

MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP, 4.40mm BODY, 0.65mm PITCH

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0066	C	1/1

TSSOP.EPS