19-0114; Rev 2; 12/96

MAXIM

Improved, SPST/SPDT Analog Switches

General Description

Maxim's redesigned DG417/DG418/DG419 precision, CMOS, monolithic analog switches now feature guaranteed on-resistance matching (3Ω max) between switches and guaranteed on-resistance flatness over the signal range (4Ω max). These switches conduct equally well in either direction and guarantee low charge injection, low power consumption, and an ESD tolerance of 2000V minimum per Method 3015.7. The new design offers low off-leakage current over temperature (less than 5nA at +85°C).

The DG417/DG418 are single-pole/single-throw (SPST) switches. The DG417 is normally closed, and the DG418 is normally open. The DG419 is single-pole/double-throw (SPDT) with one normally closed switch and one normally open switch. Switching times are less than 175ns max for t_{ON} and less than 145ns max for t_{OFF}. Operation is from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies. The improved DG417/DG418/DG419 are fabricated with a 44V silicon-gate process.

Applications

Sample-and-Hold Circuits	Communications Systems
Test Equipment	Battery-Operated Systems
Modems	Fax Machines
Guidance and Control Systems	PBX, PABX
Audio Signal Routing	Military Radios

New Features

- **Plug-In Upgrades for Industry-Standard DG417/DG418/DG419**
- **Improved $R_{DS(ON)}$ Match Between Channels (3Ω max, DG419 only)**
- **Guaranteed $R_{FLAT(ON)}$ Over Signal Range (4Ω max)**
- **Improved Charge Injection (10pC max)**
- **Improved Off-Leakage Current Over Temperature (<5nA at +85°C)**
- **Withstand Electrostatic Discharge (2000V min) per Method 3015.7**

Existing Features

- **Low $R_{DS(ON)}$ (35Ω max)**
- **Single-Supply Operation +10V to +30V Bipolar-Supply Operation ±4.5V to ±20V**
- **Low Power Consumption (35µW max)**
- **Rail-to-Rail Signal Handling**
- **TTL/CMOS-Logic Compatible**

Ordering Information

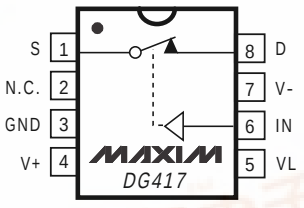
PART	TEMP. RANGE	PIN-PACKAGE
DG417CJ	0°C to +70°C	8 Plastic DIP
DG417CY	0°C to +70°C	8 SO
DG417C/D	0°C to +70°C	Dice*
DG417DJ	-40°C to +85°C	8 Plastic DIP
DG417DY	-40°C to +85°C	8 SO

Ordering Information continued at end of data sheet.

** Contact factory for dice specifications.*

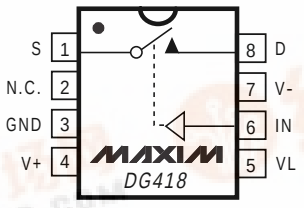
Pin Configurations/Functional Diagrams/Truth Tables

TOP VIEW



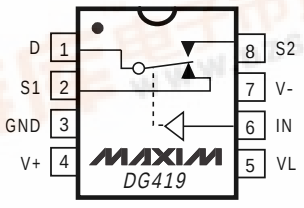
DIP/SO

DG417	
LOGIC	SWITCH
0	ON
1	OFF



DIP/SO

DG418	
LOGIC	SWITCH
0	OFF
1	ON



DIP/SO

DG419		
LOGIC	SWITCH 1	SWITCH 2
0	ON	OFF
1	OFF	ON

N.C. = NO INTERNAL CONNECTION

SWITCHES SHOWN FOR LOGIC "0" INPUT

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
VL .....(GND - 0.3V) to (V+ + 0.3V)
Digital Inputs V_S, V_D (Note 1) .....(V- - 2V) to (V+ + 2V) or 30mA (whichever occurs first)
Continuous Current (any terminal) (Note 1) 30mA
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max) ..100mA

Continuous Power Dissipation (T_A = +70°C)
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
SO (derate 5.88mW/°C above +70°C) 471mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges
DG41_C_ .....0°C to +70°C
DG41_D_ .....-40°C to +85°C
DG41_AK .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Note 1: Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—Dual Supplies

(V+ = +15V, V- = -15V, VL = 5V, GND = 0V, V_{INL} = 0.8V, V_{INH} = 2.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS				MIN	TYP (Note 2)	MAX	UNITS
SWITCH									
Analog Signal Range	$V_{S\_}$, V_D	(Note 3)				-15		15	V
Drain-Source On-Resistance	$R_{DS(ON)}$	V+ = 13.5V, V- = -13.5V, V_D = ±10V, I_S = -10mA		T_A = +25°C	C, D		20	35	Ω
					A		20	30	
				T_A = T_{MIN} to T_{MAX}				45	
On-Resistance Match Between Channels (Note 4)	$\Delta R_{DS(ON)}$	V+ = 15V, V- = -15V, V_D = ±10V, I_S = -10mA		T_A = +25°C				3	Ω
				T_A = T_{MIN} to T_{MAX}				4	
On-Resistance Flatness (Note 4)	$R_{FLAT(ON)}$	V+ = 15V, V- = -15V, V_D = ±5V, I_S = -10mA		T_A = +25°C				4	Ω
				T_A = T_{MIN} to T_{MAX}				6	
Source-Off Leakage Current (Note 5)	$I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V		T_A = +25°C		-0.25		0.25	nA
				T_A = T_{MIN} to T_{MAX}	C, D	-5		5	
					A	-20		20	
Drain-Off Leakage Current (Note 5)	$I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	DG417/ DG418	T_A = +25°C		-0.25	0.1	0.25	nA
				T_A = T_{MIN} to T_{MAX}	C, D	-5		5	
					A	-20		20	
			DG419	T_A = +25°C		-0.75	-0.1	0.75	
				T_A = T_{MIN} to T_{MAX}	C, D	-10		10	
					A	-40		40	
Drain-On Leakage Current (Note 5)	$I_{D(ON)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ±15.5V	DG417/ DG418	T_A = +25°C		-0.4		0.4	nA
				T_A = T_{MIN} to T_{MAX}	C, D	-10		10	
					A	-40		40	
			DG419	T_A = +25°C		-0.75		0.75	
				T_A = T_{MIN} to T_{MAX}	C, D	-10		10	
					A	-40		40	

ELECTRICAL CHARACTERISTICS—Dual Supplies (continued)

(V+ = +15V, V- = -15V, VL = 5V, GND = 0V, V_{INL} = 0.8V, V_{INH} = 2.4V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
LOGIC INPUT							
Logic Input Current with Input Voltage High	I_{INH}	V_{IN} = 2.4V		-0.5	0.005	0.5	µA
Logic Input Current with Input Voltage Low	I_{INL}	V_{IN} = 0.8V		-0.5	0.005	0.5	µA
DYNAMIC							
Turn-On Time	t_{ON}	DG417/DG418, V_D = ±10V, Figure 2	T_A = +25°C		100	175	ns
			T_A = T_{MIN} to T_{MAX}			250	
Turn-Off Time	t_{OFF}	DG417/DG418, V_D = ±10V, Figure 2	T_A = +25°C		60	145	ns
			T_A = T_{MIN} to T_{MAX}			210	
Transition Time	t_{TRANS}	DG419, V_S = ±10V, Figure 3	T_A = +25°C			175	ns
			T_A = T_{MIN} to T_{MAX}			250	
Break-Before-Make Interval	t_D	DG419, V_{S1} = V_{S2} = ±10V, Figure 4, T_A = +25°C		5	13		ns
Charge Injection (Note 3)	Q	V_{GEN} = 0V, Figure 5, T_A = +25°C			3	10	pC
Off-Isolation Rejection Ratio (Note 6)	OIRR	R_L = 500Ω, C_L = 5pF, f = 1MHz, Figure 6, T_A = +25°C			68		dB
Crosstalk (Note 7)		DG419, R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 7, T_A = +25°C			85		dB
Drain Off-Capacitance	$C_{D\ (OFF)}$	V_D = 0V, f = 1MHz, Figure 8, T_A = +25°C			8		pF
Source Off-Capacitance	$C_{S\ (OFF)}$	V_D = 0V, f = 1MHz, Figure 8, T_A = +25°C			8		pF
Drain-Source On-Capacitance	$C_{D\ (ON)}$ or $C_{S\ (ON)}$	V_S = 0V, f = 1MHz, Figure 9, T_A = +25°C	DG417/DG418		30		pF
			DG419		35		
SUPPLY							
Positive Supply Current	I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Negative Supply Current	I-	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Logic Supply Current	I_L	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	
Ground Current	I_{GND}	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1	-0.0001	1	µA
			T_A = T_{MIN} to T_{MAX}	-5		5	

ELECTRICAL CHARACTERISTICS—Single Supply

(V+ = +12V, V- = 0V, VL = 5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
SWITCH						
Analog Signal Range	V_{ANALOG}	(Note 3)	0		12	V
Drain-Source On-Resistance	$R_{DS(ON)}$	I_S = -10mA, V_D = 3.8V, V+ = 10.8V		40	100	Ω
DYNAMIC						
Turn-On Time	t_{ON}	DG417/DG418, V_D = 8V, Figure 2		110		ns
Turn-Off Time	t_{OFF}	DG417/DG418, V_D = 8V, Figure 2		40		ns
Break-Before-Make Interval	t_D	DG419, R_L = 1000Ω, C_L = 35pF, Figure 4		60		ns
Charge Injection (Note 3)	Q	C_L = 10nF, V_{GEN} = 0V, R_{GEN} = 0V, Figure 5		2	10	pC
SUPPLY						
Positive Supply Current	I+	All channels on or off, V+ = 13.2V, V_L = 5.25V, V_{IN} = 0V or 5V		-0.0001		µA
Negative Supply Current	I-	All channels on or off, V+ = 13.2V, V_L = 5.25V, V_{IN} = 0V or 5V		-0.0001		µA
Logic Supply Current	I_L	All channels on or off, V_L = 5.25V, V_{IN} = 0V or 5V		-0.0001		µA
Ground Current	I_{GND}	All channels on or off, V_L = 5.25V, V_{IN} = 0V or 5V		-0.0001		µA

Note 2: Typical values are for **design aid only**, are not guaranteed, and are not subject to production testing. The algebraic convention where the most negative value is a minimum and the most positive value a maximum is used in this data sheet.

Note 3: Guaranteed by design.

Note 4: On-resistance match between channels and flatness is guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and the minimum value of on-resistance as measured at the extremes of the specified analog range.

Note 5: Leakage parameters $I_{S(OFF)}$, $I_{D(OFF)}$, and $I_{D(ON)}$ are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.

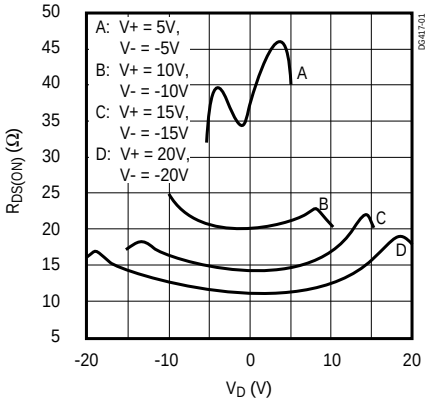
Note 6: Off-Isolation Rejection Ratio = 20log (V_D/V_S), V_D = output, V_S = input to off switch.

Note 7: Between any two switches.

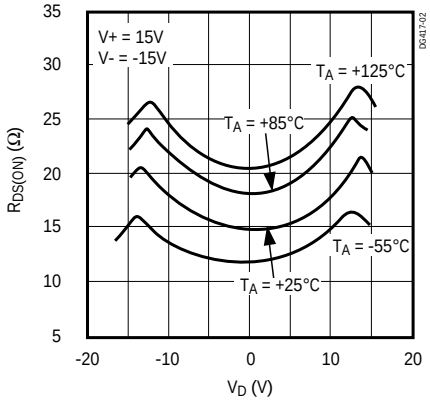
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

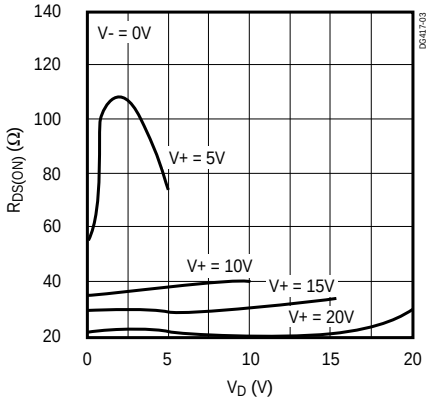
ON-RESISTANCE vs. V_D AND POWER-SUPPLY VOLTAGE



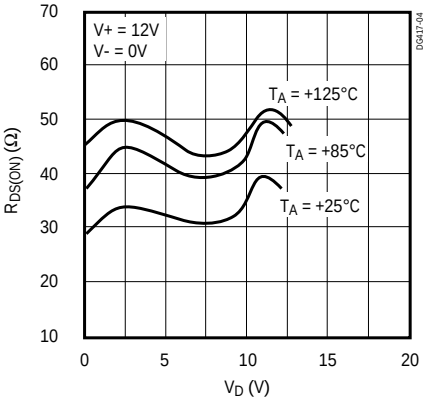
ON-RESISTANCE vs. V_D AND TEMPERATURE



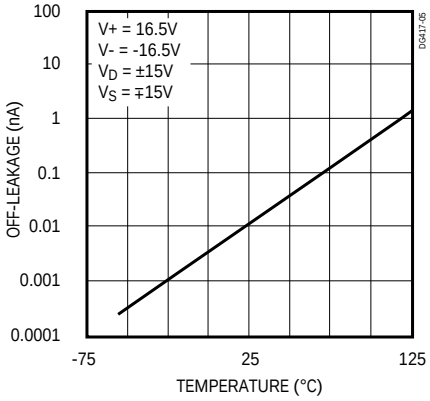
ON-RESISTANCE vs. V_D (SINGLE SUPPLY)



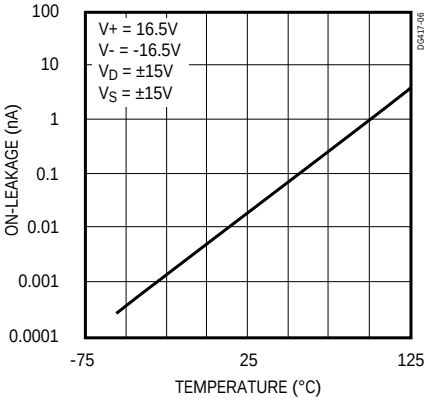
ON-RESISTANCE vs. V_D AND TEMPERATURE



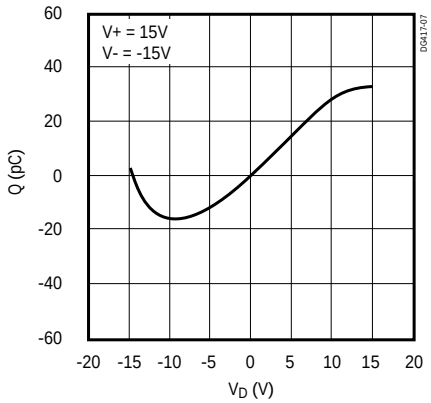
OFF-LEAKAGE CURRENT vs. TEMPERATURE



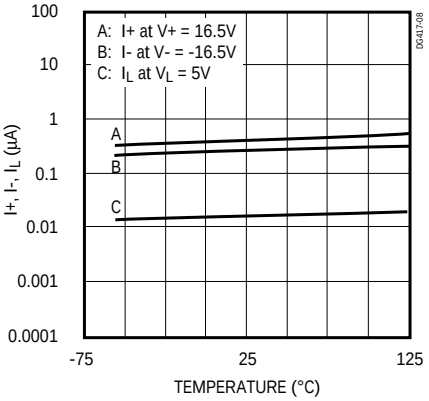
ON-LEAKAGE CURRENT vs. TEMPERATURE



CHARGE INJECTION vs. ANALOG VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



Pin Description

PIN			NAME	FUNCTION
DG417	DG418	DG419		
1	—	—	S	Analog-Switch Source Terminal (normally closed)
—	1	—	S	Analog-Switch Source Terminal (normally open)
—	—	2	S1	Analog-Switch Source Terminal 1 (normally closed)
2	2	—	N.C.	No Internal Connection
3	3	3	GND	Logic Ground
4	4	4	V+	Analog-Signal Positive Supply Input
5	5	5	VL	Logic-Level Positive Supply Input
6	6	6	IN	Logic-Level Input
7	7	7	V-	Analog-Signal Negative Supply Input
8	8	1	D	Analog-Switch Drain Terminal
—	—	8	S2	Analog-Switch Source Terminal 2 (normally open)

Applications Information

Operation with Supply Voltages Other than ±15V

Using supply voltages other than ±15V reduces the analog signal range. The DG417/DG418/DG419 switches operate with ±4.5V to ±20V bipolar supplies or with a +10V to +30V single supply; connect V- to 0V when operating with a single supply. Also, all device types can operate with unbalanced supplies, such as +24V and -5V. VL must be connected to +5V to be TTL compatible, or to V+ for CMOS-logic level inputs. The *Typical Operating Characteristics* graphs show typical on-resistance with ±20V, ±15V, ±10V, and ±5V supplies. (Switching times increase by a factor of two or more for operation at ±5V.)

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by VL, V-, and logic inputs. If power-supply sequencing is not possible, add two small, external signal diodes in series with the supply pins for overvoltage protection (Figure 1).

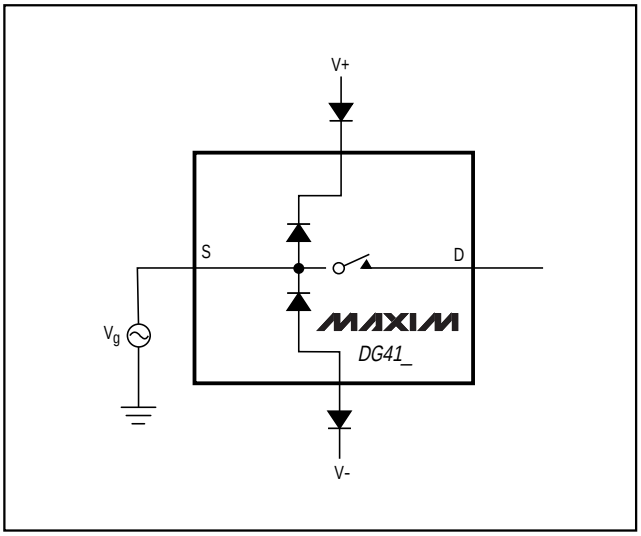


Figure 1. Overvoltage Protection Using External Blocking Diodes

Adding diodes reduces the analog signal range to 1V below V+ and 1V above V-, without affecting low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed +44V.

Test Circuits/Timing Diagrams

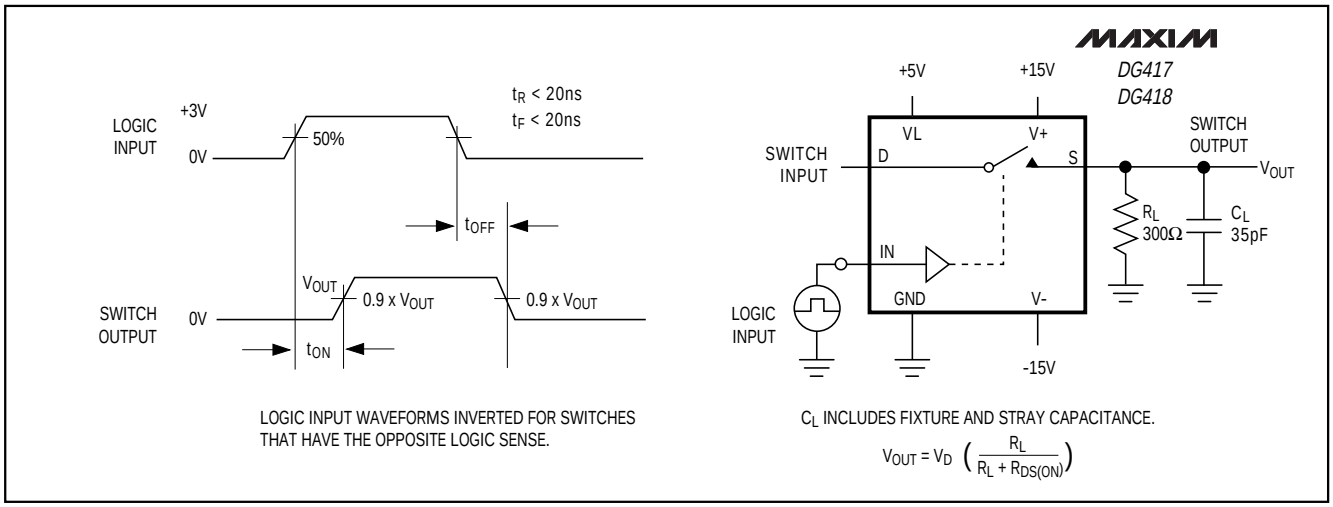


Figure 2. DG417/DG418 Switching Time

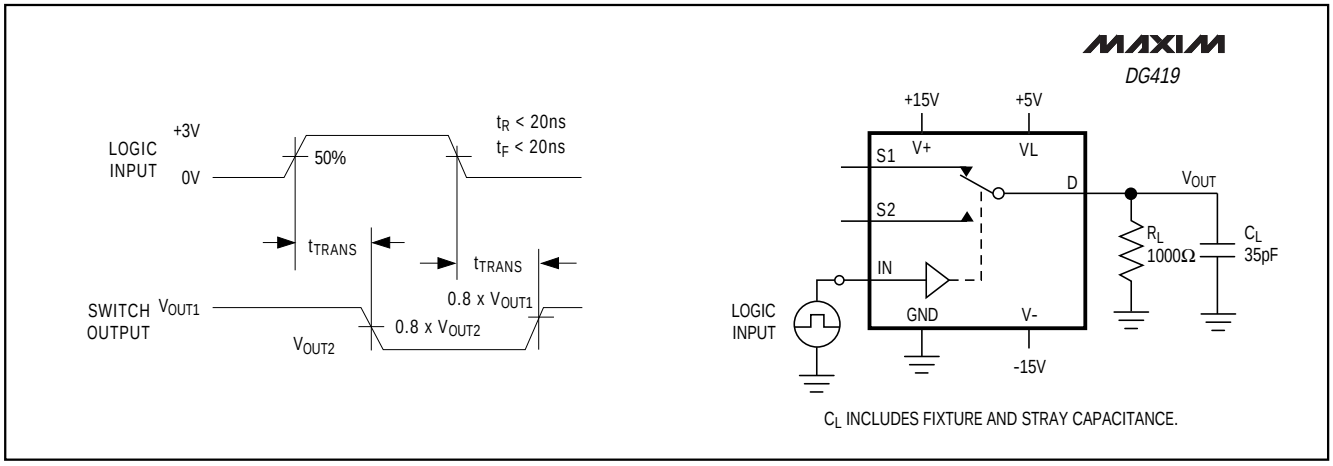


Figure 3. DG419 Transition Time

Test Circuits/Timing Diagrams (continued)

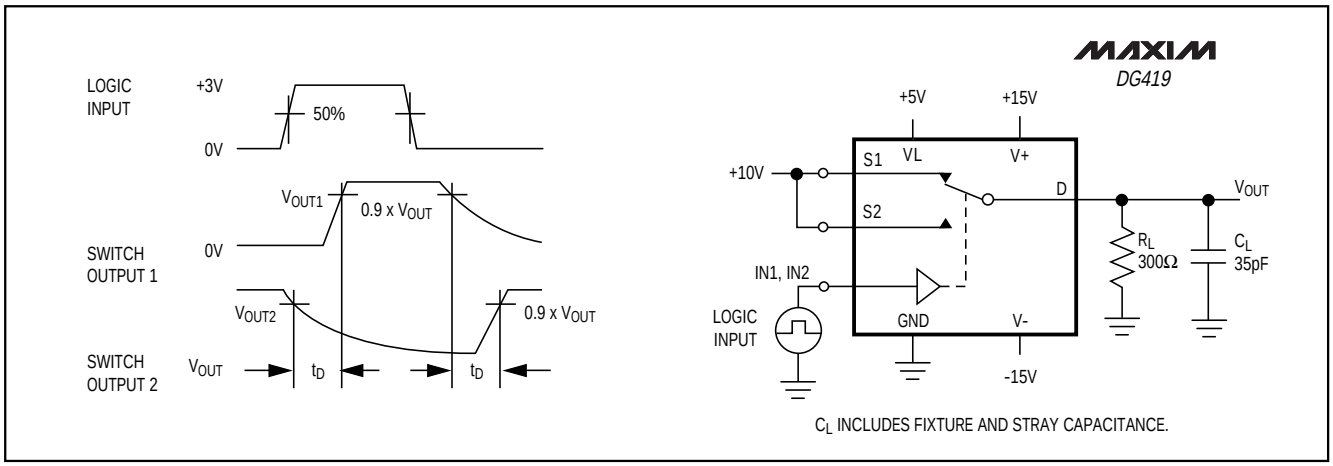


Figure 4. DG419 Break-Before-Make Interval

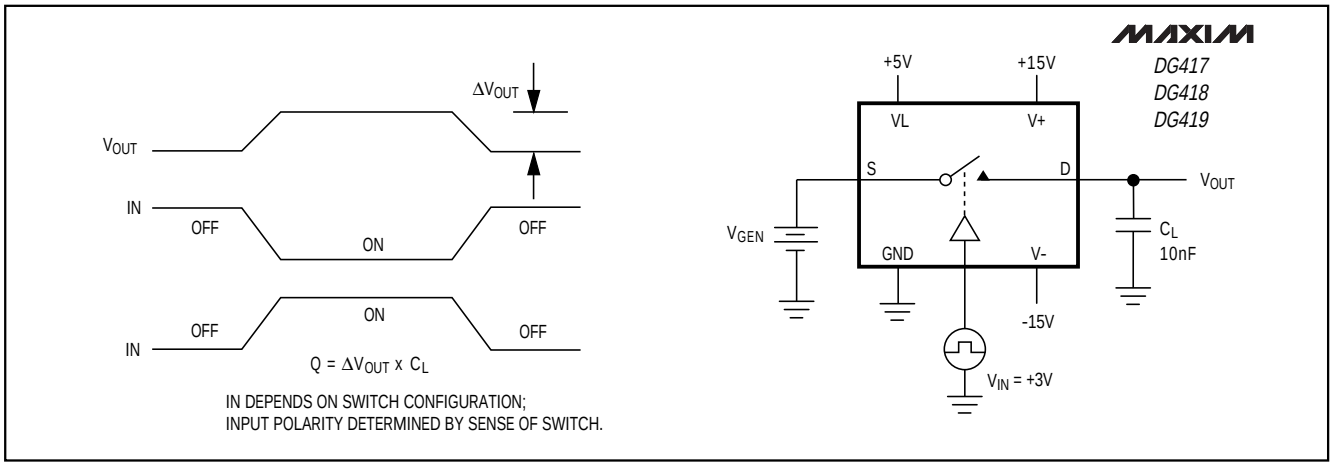


Figure 5. Charge Injection

Test Circuits/Timing Diagrams (continued)

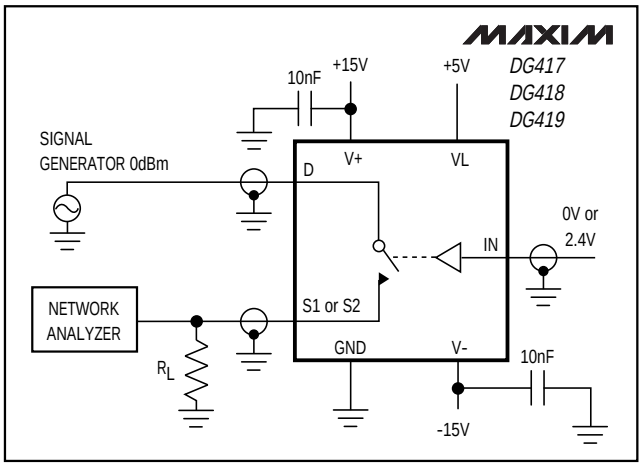


Figure 6. Off-Isolation Rejection Ratio

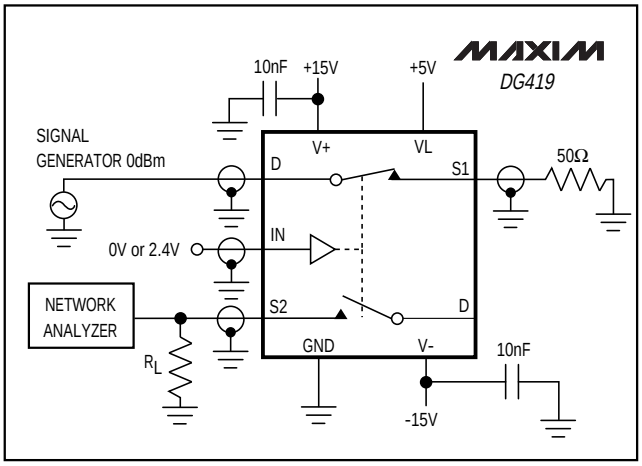


Figure 7. DG419 Crosstalk

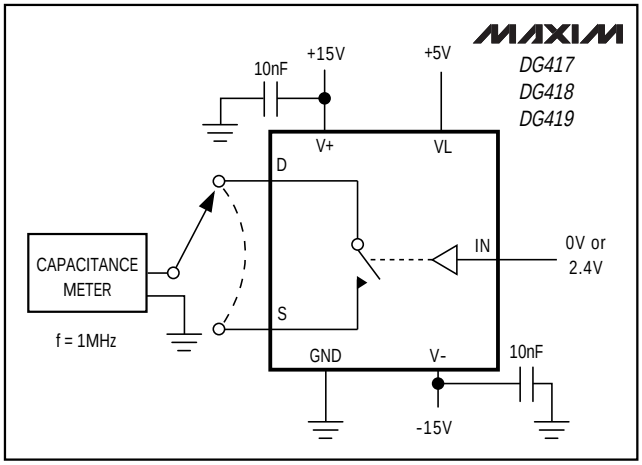


Figure 8. Drain-Source Off-Capacitance

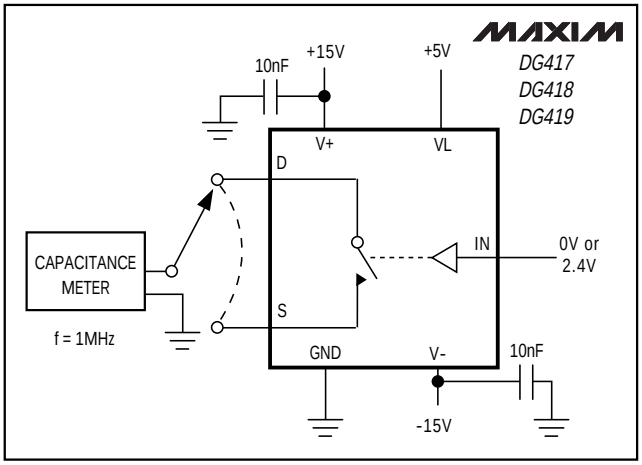


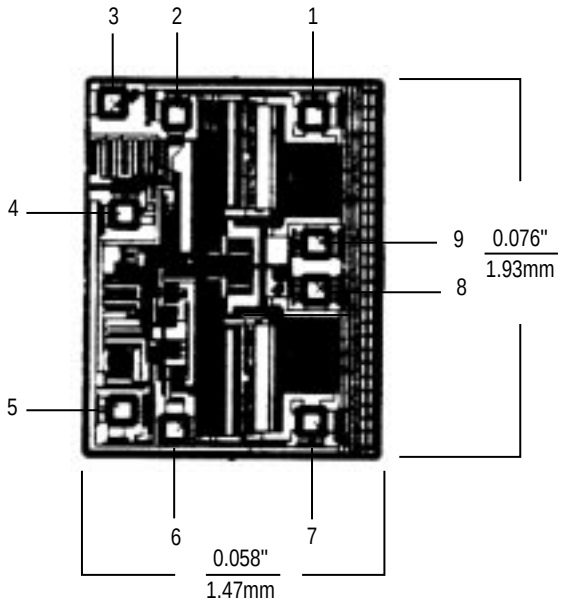
Figure 9. Drain-Source On-Capacitance

Ordering Information (continued)

PART	TEMP. RANGE	PIN-PACKAGE
DG417DK	-40°C to +85°C	8 CERDIP
DG417AK	-55°C to +125°C	8 CERDIP**
DG418CJ	0°C to +70°C	8 Plastic DIP
DG418CY	0°C to +70°C	8 SO
DG418C/D	0°C to +70°C	Dice*
DG418DJ	-40°C to +85°C	8 Plastic DIP
DG418DY	-40°C to +85°C	8 SO
DG418DK	-40°C to +85°C	8 CERDIP
DG418AK	-55°C to +125°C	8 CERDIP**
DG419CJ	0°C to +70°C	8 Plastic DIP
DG419CY	0°C to +70°C	8 SO
DG419C/D	0°C to +70°C	Dice*
DG419DJ	-40°C to +85°C	8 Plastic DIP
DG419DY	-40°C to +85°C	8 SO
DG419DK	-40°C to +85°C	8 CERDIP
DG419AK	-55°C to +125°C	8 CERDIP**

** Contact factory for dice specifications.*
***Contact factory for availability and processing to MIL-STD-883B.*

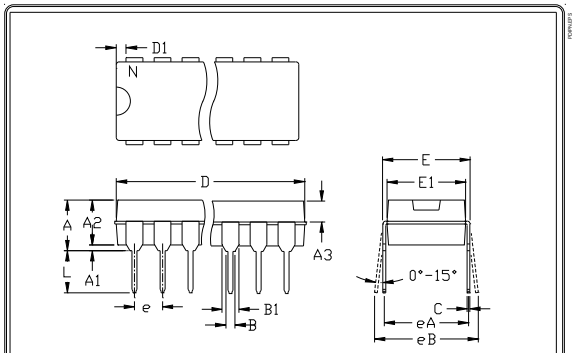
Chip Topography



TRANSISTOR COUNT: 32
SUBSTRATE CONNECTED TO V+

DIE PAD	DG417	DG418	DG419
1	D	N.C.	S
2	GND	GND	GND
3	V+	V+	V+
4	VL	VL	VL
5	IN	IN	IN
6	V-	V-	V-
7	N.C.	S	S
8	N.C.	D	D
9	S	N.C.	D

Package Information

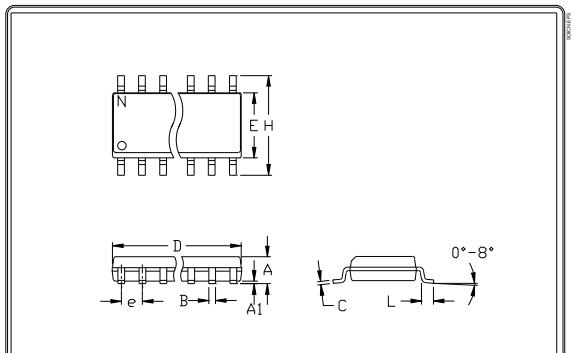


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 A



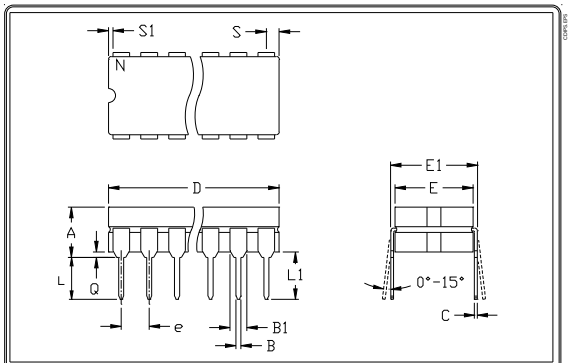
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.014	0.019	0.35	0.49
C	0.007	0.010	0.19	0.25
e	0.050		1.27	
E	0.150	0.157	3.80	4.00
H	0.228	0.244	5.80	6.20
h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS012
D	0.189	0.197	4.80	5.00	8	A
D	0.337	0.344	8.55	8.75	14	B
D	0.386	0.394	9.80	10.00	16	C

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SOIC .150" | 1/1 | 21-0041 A

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	---	0.00	---
Q	0.015	0.070	0.38	1.78
S	---	0.098	---	2.49
S1	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	0.405	---	10.29	8	P:D4
D	---	0.785	---	19.94	14	C:D1
D	---	0.840	---	21.34	16	E:D2
D	---	0.960	---	24.38	18	V:D6
D	---	1.060	---	26.92	20	R:D8
D	---	1.280	---	32.51	24	L:D9

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #1 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: CDIP .300" | 1/1 | 21-0045 A