19-0137; Rev 1; 3/94

MAXIM

Improved Low-Power, CMOS Analog Switches with Latches

General Description

Maxim's redesigned DG421/DG423/DG425 monolithic analog switches now feature guaranteed on-resistance matching (3Ω max) between switches and on-resistance flatness over the signal range (4Ω max). These low on-resistance switches (20Ω typ) conduct equally well in both directions. They guarantee a low charge injection of 15pC maximum and an ESD tolerance of 2000V minimum per Method 3015.7. Off leakage current over temperature has also been reduced (less than 5nA at +85°C).

The DG421/DG423/DG425 are precision, dual CMOS switches with latchable logic inputs that simplify interfacing with microprocessors (µPs). The single-pole/single-throw DG421 and double-pole/single-throw DG425 are normally open dual switches. The dual, single-pole/double-throw DG423 has two normally open and two normally closed switches. Fast switching times (175ns for t_{ON} and 145ns for t_{OFF}) and low power consumption (35µW max) make these parts ideal for battery-powered applications requiring µP-compatible switches. Operation is from a single +10V to +30V supply, or bipolar ±4.5V to ±20V supplies. Fabricated with the same 44V silicon-gate process, these switches have rail-to-rail signal handling capabilities.

Applications

Sample-and-Hold Circuits	Modems
Fax Machines	Test Equipment
Battery-Operated Systems	PBX, PABX
Guidance and Control Systems	Military Radios
Audio Signal Routing	Communication Systems

New Features

- **Plug-In Upgrades for Industry-Standard DG421/DG423/DG425**
- **Improved $r_{(DS)ON}$ Match Between Channels (3Ω max)**
- **Guaranteed $r_{FLAT(ON)}$ Over Signal Range (4Ω max)**
- **Improved Charge Injection (15pC max)**
- **Improved Off Leakage Current Over Temperature (<5nA at +85°C)**
- **Withstands Electrostatic Discharge (2000V min) per Method 3015.7**

Existing Features

- **Low $r_{DS(ON)}$ (35Ω max)**
- **Single-Supply Operation +10V to +30V Bipolar-Supply Operation ±4.5V to ±20V**
- **Low Power Consumption (35µW max)**
- **Rail-to-Rail Signal Handling Capability**
- **TTL/CMOS-Logic Compatible**

Ordering Information

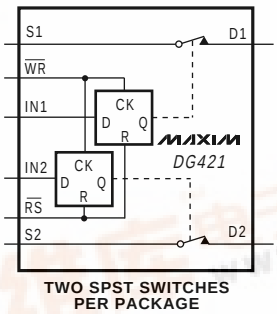
PART	TEMP. RANGE	PIN-PACKAGE
DG421CJ	0°C to +70°C	16 Plastic DIP
DG421CY	0°C to +70°C	16 SO
DG421C/D	0°C to +70°C	Dice*
DG421DJ	-40°C to +85°C	16 Plastic DIP
DG421DY	-40°C to +85°C	16 SO
DG421DK	-40°C to +85°C	16 CERDIP
DG421AK	-55°C to +125°C	16 CERDIP**

Ordering Information continued at end of data sheet.

** Contact factory for dice specifications.*

***Contact factory for availability and processing to MIL-STD-883B.*

Functional Diagrams/Truth Tables



TWO SPST SWITCHES PER PACKAGE

DG421 TRUTH TABLE

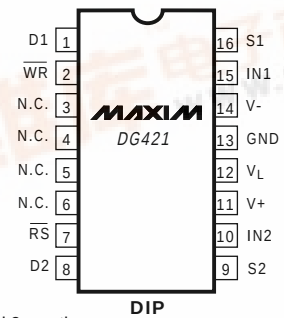
WR	RS	IN	SWITCH
0	1	0	Off
		1	On

LOGIC "0" ≤ 0.8V
LOGIC "1" ≥ 2.4V

SWITCHES SHOWN FOR LOGIC "1" INPUT

Functional Diagrams/Truth Tables continued at end of data sheet.

Pin Configurations



DIP

N.C. = No Internal Connection

Pin Configurations continued at end of data sheet.

Improved Low-Power, CMOS Analog Switches with Latches

ABSOLUTE MAXIMUM RATINGS

Voltage Referenced to V-
V+ 44V
GND 25V
V_L ..... (GND - 0.3V) to (V+ + 0.3V)
Digital Inputs, V_S, V_D (Note 1) ..... (V- - 2V) to (V+ + 2V)
Current (any terminal, except S or D) 30mA
Continuous Current, S or D 20mA
Peak Current, S or D (pulsed at 1ms, 10% duty cycle max) ... 100mA

Continuous Power Dissipation (T_A = +70°C)
16-Pin Plastic DIP (derate 10.53mW/°C above +70°C) ... 842mW
20-Pin PLCC (derate 10.00mW/°C above +70°C) 800mW
16-Pin CERDIP (derate 10.00mW/°C above +70°C) ... 800mW
Operating Temperature Ranges
DG42_C_ ..... 0°C to +70°C
DG42_D_ ..... -40°C to +85°C
DG42_A_ ..... -55°C to +125°C
Storage Temperature Ranges
DG42_C_/DG42_D_ ..... -65°C to +125°C
DG42_A_ ..... -65°C to +150°C
Lead Temperature (soldering, 10sec) ..... +300°C

Note 1: Signals on S, D, or IN exceeding V+ or V- are clamped by internal diodes. Limit forward current to maximum current ratings.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = 15V, V- = -15V, V_L = +5V, GND = 0V, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		DG42_C, DG42_D MIN	DG42_C, DG42_D TYP	DG42_C, DG42_D MAX	DG42_A MIN	DG42_A TYP	DG42_A MAX	UNITS
				(Note 2)			(Note 2)			
SWITCH										
Analog Signal Range	V_{ANALOG}	(Note 3)		-15		15	-15		15	V
Drain-Source On-Resistance	$r_{DS(ON)}$	V+ = 13.5V, V- = -13.5V, I_S = -10mA, V_D = ±10V	T_A = +25°C		20	45		20	35	Ω
			T_A = T_{MIN} to T_{MAX}			45			45	
On-Resistance Match Between Channels (Note 4)	$\Delta r_{DS(ON)}$	V+ = 16.5V, V- = -16.5V, I_S = -10mA, V_D = ±10V	T_A = +25°C			3			3	Ω
			T_A = T_{MIN} to T_{MAX}			4			4	
On-Resistance Flatness (Note 4)	$r_{FLAT(ON)}$	V+ = 15V, V- = -15V, I_S = -10mA, V_D = ±5V	T_A = +25°C			4			4	Ω
			T_A = T_{MIN} to T_{MAX}			5			5	
Source-Off Leakage Current (Note 5)	$I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	T_A = +25°C	-0.50	-0.01	0.50	-0.25	-0.01	0.25	nA
			T_A = T_{MIN} to T_{MAX}	-5		5	-10		10	
Drain-Off Leakage Current (Note 5)	$I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	T_A = +25°C	-0.50	-0.01	0.50	-0.25	-0.01	0.25	nA
			T_A = T_{MIN} to T_{MAX}	-5		5	-10		10	
Drain-On Leakage Current (Note 5)	$I_{D(ON)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ±15.5V	T_A = +25°C	-1.0	-0.04	1.0	-0.40	-0.04	0.40	nA
			T_A = T_{MIN} to T_{MAX}	-10		10	-20		20	

ELECTRICAL CHARACTERISTICS (continued)

(V+ = 15V, V- = -15V, V_L = +5V, GND = 0V, V_{INH} = +2.4V, V_{INL} = +0.8V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP (Note 2)	MAX	UNITS
INPUT							
Input Current with Input Voltage High	I_{INH}	IN = 2.4V, all others = 0.8V		-0.50	0.005	0.50	µA
Input Current with Input Voltage Low	I_{INL}	IN = 0.8V, all others = 2.4V		-0.50	0.005	0.50	µA
SUPPLY							
Power Supply Range	V+, V-	(Note 3)		±4.5		±20	V
Positive Supply Current	I+	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1.0	0.01	1.0	µA
			T_A = T_{MIN} to T_{MAX}	-5.0		5.0	
Negative Supply Current	I-	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1.0	-0.01	1.0	µA
			T_A = T_{MIN} to T_{MAX}	-5.0		5.0	
Logic Supply Current	I_L	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1.0	-0.01	1.0	µA
			T_A = T_{MIN} to T_{MAX}	-5.0		5.0	
Ground Current	I_{GND}	All channels on or off, V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	T_A = +25°C	-1.0	-0.01	1.0	µA
			T_A = T_{MIN} to T_{MAX}	-5.0		5.0	
DYNAMIC							
Turn-On Time	t_{ON}	Figure 2	T_A = +25°C		150	250	ns
			T_A = T_{MIN} to T_{MAX}			300	
Turn-Off Time	t_{OFF}	Figure 2				200	ns
Latch Timing	t_{WW}	V_S = ±10V, R_L = 300Ω, C_L = 35pF, Figure 3	T_A = +25°C	200			ns
			T_A = -55°C to +125°C	200			
	t_{DW}		T_A = +25°C	100			
			T_A = -55°C to +125°C	100			
	t_{WD}		T_A = +25°C	60			
			T_A = -55°C to +125°C	100			
Break-Before-Make Interval (Note 3)	t_D	DG423, Figure 4	T_A = +25°C	5	25		ns
Charge Injection (Note 3)	Q	C_L = 10nF, V_G = 0V, R_G = 0Ω, Figure 5	T_A = +25°C		10	15	pC
Off-Isolation Rejection Ratio (Note 6)	OIRR	R_L = 100Ω, C_L = 5pF, f = 1MHz, Figure 6	T_A = +25°C		72		dB
Crosstalk (Note 7)		R_L = 50Ω, C_L = 5pF, f = 1MHz, Figure 7	T_A = +25°C		90		dB
Drain-Off Capacitance	$C_{D(OFF)}$	f = 1MHz, Figure 8	T_A = +25°C		12		pF
Source-Off Capacitance	$C_{S(OFF)}$	f = 1MHz, Figure 8	T_A = +25°C		12		pF
Drain-On Capacitance	$C_{D(ON)}$	f = 1MHz, Figure 9	T_A = +25°C		39		pF
Source-On Capacitance	$C_{S(ON)}$	f = 1MHz, Figure 9	T_A = +25°C		39		pF

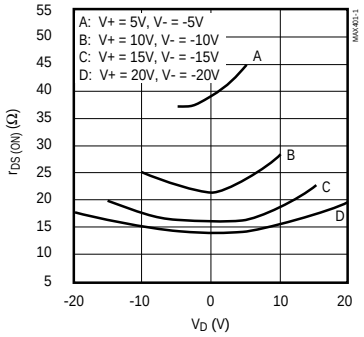
Note 2: Typical values are **for design aid only**, are not guaranteed, and are not subject to production testing. The algebraic convention, where the most negative value is a minimum and the most positive value a maximum, is used in this data sheet.
Note 3: Guaranteed by design.
Note 4: On-resistance match between channels and flatness are guaranteed only with bipolar-supply operation. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured at the extremes of the specified analog signal range.
Note 5: Leakage parameters $I_{S(OFF)}$, $I_{D(OFF)}$, and $I_{D(ON)}$ are 100% tested at the maximum rated hot temperature and guaranteed by correlation at +25°C.
Note 6: Off-Isolation Rejection Ratio = 20log (V_D/V_S), V_D = output, V_S = input to off switch.
Note 7: Between any two switches.

Improved Low-Power, CMOS Analog Switches with Latches

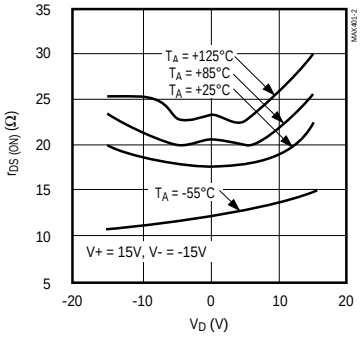
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

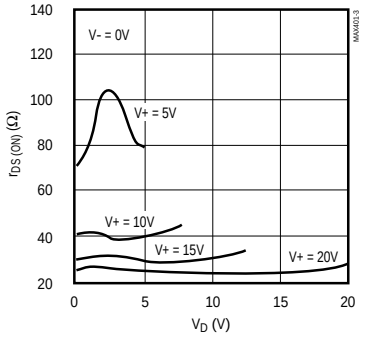
ON-RESISTANCE vs. V_D (DUAL-SUPPLIES)



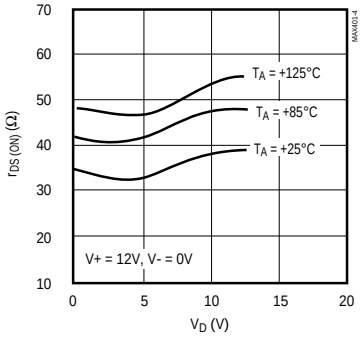
ON-RESISTANCE vs. V_D AND TEMPERATURE (DUAL SUPPLIES)



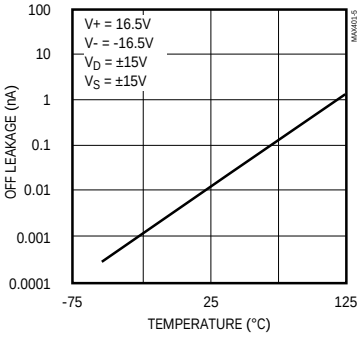
ON-RESISTANCE vs. V_D (SINGLE SUPPLY)



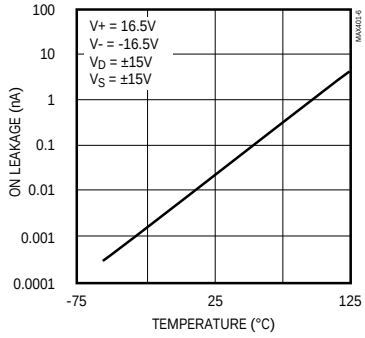
ON-RESISTANCE vs. V_D AND TEMPERATURE (SINGLE SUPPLY)



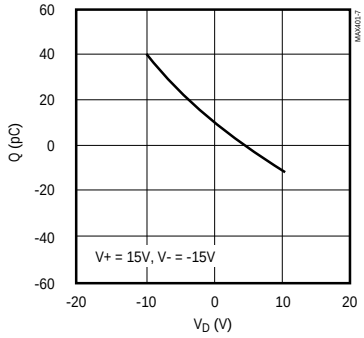
OFF LEAKAGE CURRENTS vs. TEMPERATURE



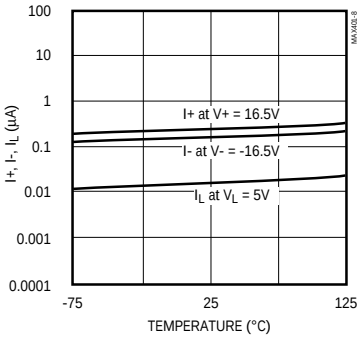
ON LEAKAGE CURRENTS vs. TEMPERATURE



CHARGE INJECTION vs. ANALOG VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



Pin Descriptions

DG421		
PIN	**NAME**	**FUNCTION**
1, 8	D1, D2	Drain Terminals
2	$\overline{WR}$	Write Select
3, 4, 5, 6	N.C.	No Internal Connection
7	$\overline{RS}$	Reset Select
9, 16	S1, S2	Source Terminals
10, 15	IN1, IN2	Input Control
11	V+	Positive Supply
12	V_L	Logic Supply
13	GND	Ground
14	V-	Negative Supply

DG423/DG425			
DIP	**PLCC**	**NAME**	**FUNCTION**
1, 8, 3, 6	2, 10, 4, 8	D1-D4	Drain Terminals
2	3	$\overline{WR}$	Write Select
16, 9, 4, 5	20, 12, 5, 7	S1-S4	Source Terminals
7	9	$\overline{RS}$	Resets Select
15, 10	19, 13	IN1, IN2	Input Control
11	14	V+	Positive Supply
12	15	V_L	Logic Supply
—	1, 6, 11, 16	N.C.	No Internal Connection
14	18	V-	Negative Supply
13	17	GND	Ground

Applications Information

Operation with Supply Voltages Other Than ±15V

The DG421/DG423/DG425 switches operate with ±4.5V to ±20V bipolar supplies or with a +10V to +30V single supply. In either case, analog signals ranging from V+ to V- can be switched. The *Typical Operating Characteristics* graphs illustrate typical analog-signal and supply-voltage on-resistance variations. The usual on-resistance temperature coefficient is 0.5%/°C (typ).

Logic Inputs

These devices operate with a single positive supply or with bipolar supplies. They maintain TTL compatibility with supplies anywhere in the ±4.5V to ±20V range as long as V_L = +5V. If V_L is connected to V+ or another supply at voltages other than +5V, the devices will operate at CMOS-logic-level inputs.

Overvoltage Protection

Proper power-supply sequencing is recommended for all CMOS devices. Do not exceed the absolute maximum ratings because stresses beyond the listed ratings may cause permanent damage to the devices. Always sequence V+ on first, followed by V_L, V-, and logic inputs. If power-supply sequencing is not possible, add two small, external signal diodes in series with supply pins for overvoltage protection (Figure 1). Adding diodes reduces the analog signal range to 1V below V+ and 1V above V-, without affecting low switch resistance and low leakage characteristics. Device operation is unchanged, and the difference between V+ and V- should not exceed +44V.

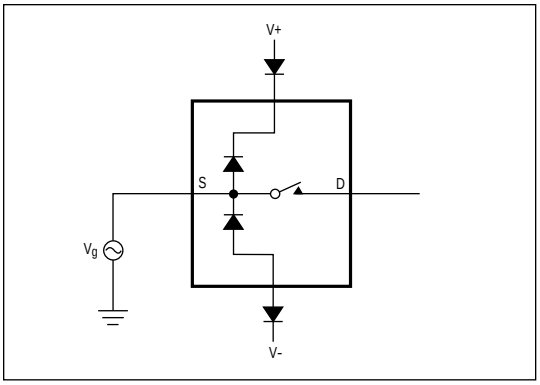


Figure 1. Overvoltage Protection Using External Blocking Diodes

Improved Low-Power, CMOS Analog Switches with Latches

Timing Diagrams/Test Circuits

V_{OUT} is the steady-state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

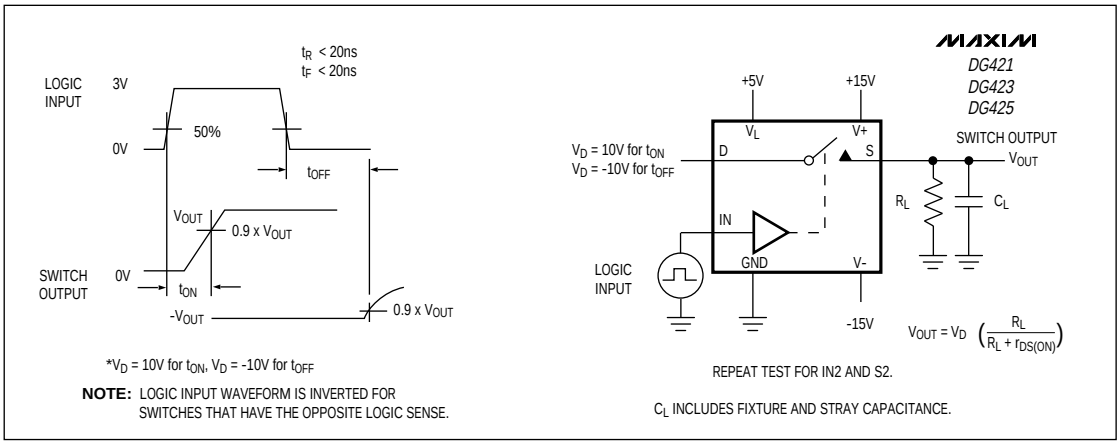


Figure 2. Switching Time

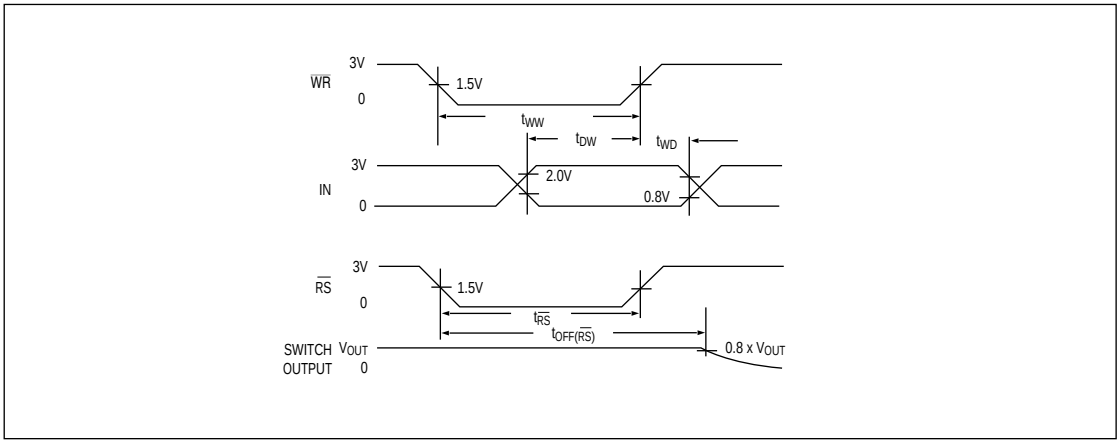


Figure 3. Latch Timing

Timing Diagrams/Test Circuits (continued)

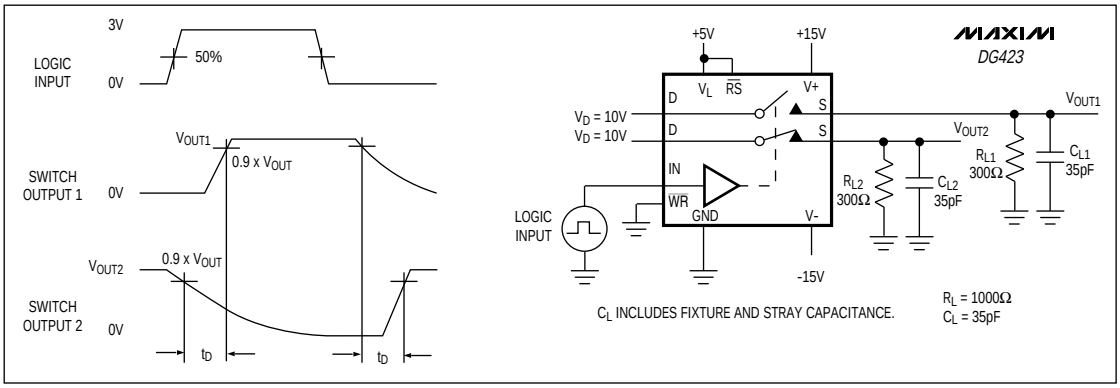


Figure 4. DG423 Break-Before-Make Interval

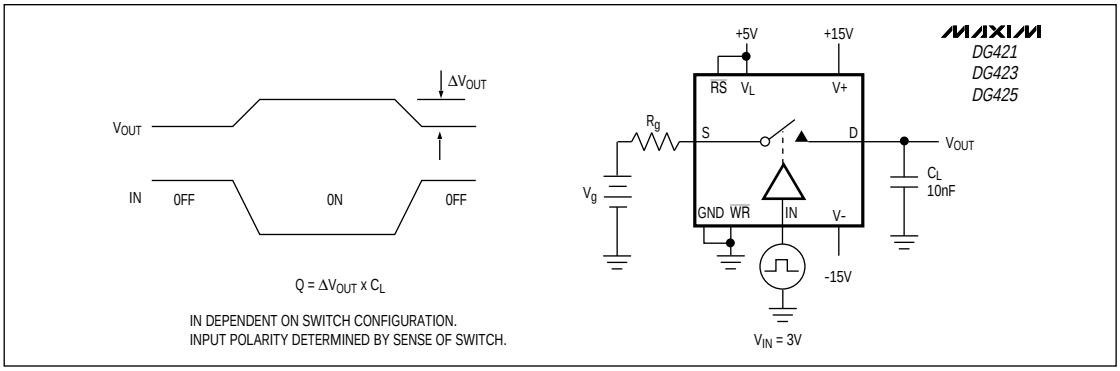


Figure 5. Charge Injection

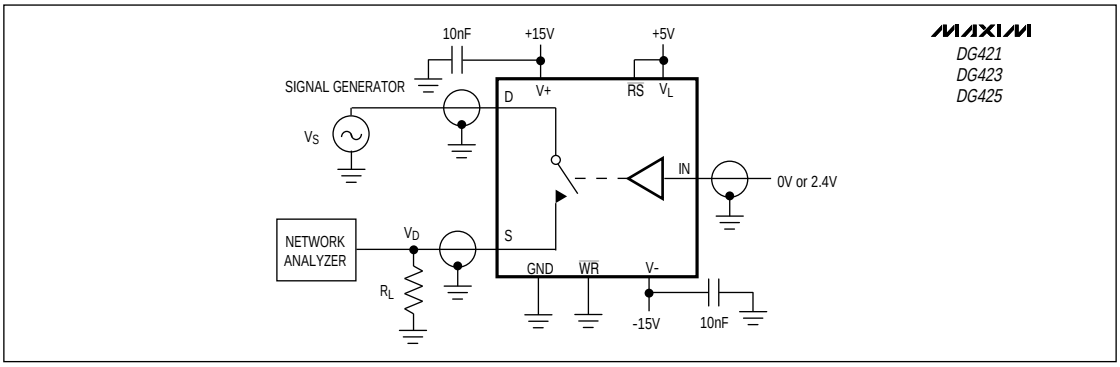


Figure 6 . Off-Isolation Rejection Ratio

Timing Diagrams/Test Circuits (continued)

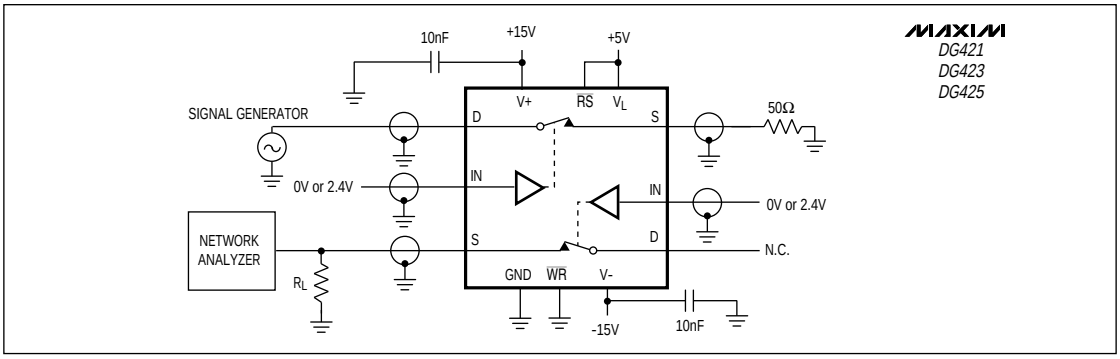


Figure 7. Crosstalk

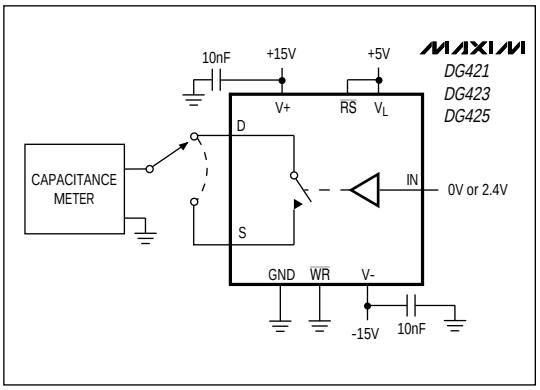


Figure 8. Drain/Source-Off Capacitance

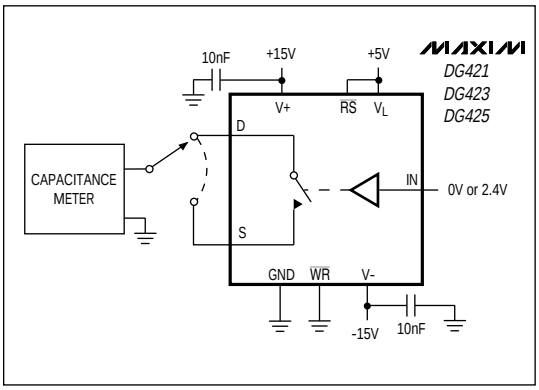
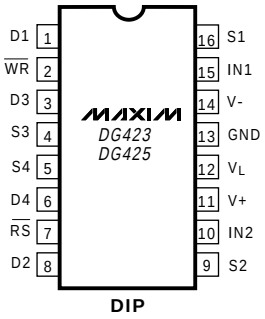


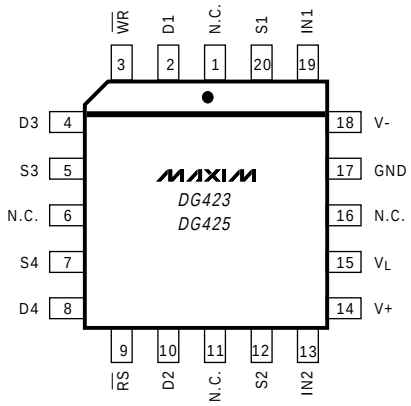
Figure 9. Drain/Source-On Capacitance

Pin Configurations (continued)



DIP

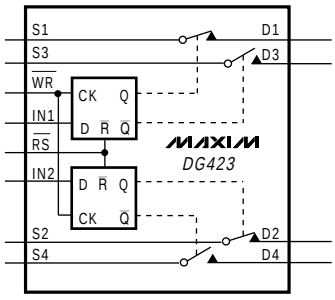
TOP VIEW



PLCC

N.C. = No Internal Connection

Functional Diagrams/Truth Tables (continued)

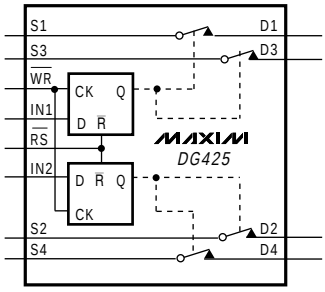


TWO SPDT SWITCHES PER PACKAGE

DG423 TRUTH TABLE

$\overline{WR}$	$\overline{RS}$	IN	SWITCH 1, 2	SWITCH 3, 4
0	1	0	Off	On
		1	On	Off

LOGIC "0" ≤ 0.8V
LOGIC "1" ≥ 2.4V



TWO DPST SWITCHES PER PACKAGE

DG425 TRUTH TABLE

$\overline{WR}$	$\overline{RS}$	IN	SWITCH
0	1	0	Off
		1	On

LOGIC "0" ≤ 0.8V
LOGIC "1" ≥ 2.4V

LATCH OPERATION TRUTH TABLE

IN	$\overline{RS}$	$\overline{WR}$	LATCH/SWITCH X
X	1	0	Latch operation transparent.
X	1	↑	Control data latched in. Switches on or off as selected by last IN.
X	0	X	All latches reset. Switches on or off as when IN = 0, $\overline{WR}$ = 0, $\overline{RS}$ = 1.
X	↓	X	

Improved Low-Power, CMOS Analog Switches with Latches

_Ordering Information (continued)

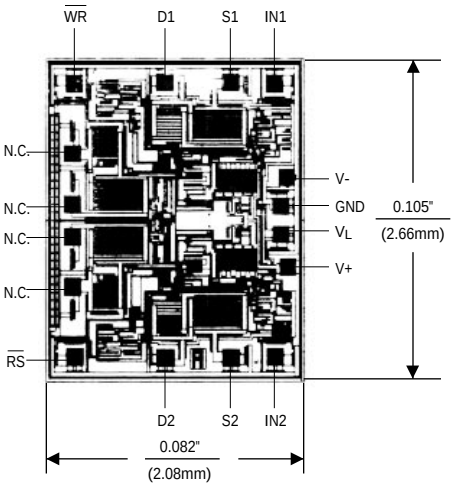
PART	TEMP. RANGE	PIN-PACKAGE
DG423CJ	0°C to +70°C	16 Plastic DIP
DG423CY	0°C to +70°C	16 SO
DG423C/D	0°C to +70°C	Dice*
DG423DJ	-40°C to +85°C	16 Plastic DIP
DG423DY	-40°C to +85°C	16 SO
DG423DN	-40°C to +85°C	20 PLCC
DG423DK	-40°C to +85°C	16 CERDIP
DG423AK	-55°C to +125°C	16 CERDIP**
DG425CJ	0°C to +70°C	16 Plastic DIP
DG425CY	0°C to +70°C	16 SO
DG425C/D	0°C to +70°C	Dice*
DG425DJ	-40°C to +85°C	16 Plastic DIP
DG425DY	-40°C to +85°C	16 SO
DG425DN	-40°C to +85°C	20 PLCC
DG425DK	-40°C to +85°C	16 CERDIP
DG425AK	-55°C to +125°C	16 CERDIP**

** Contact factory for dice specifications.*

***Contact factory for availability and processing to MIL-STD-883B.*

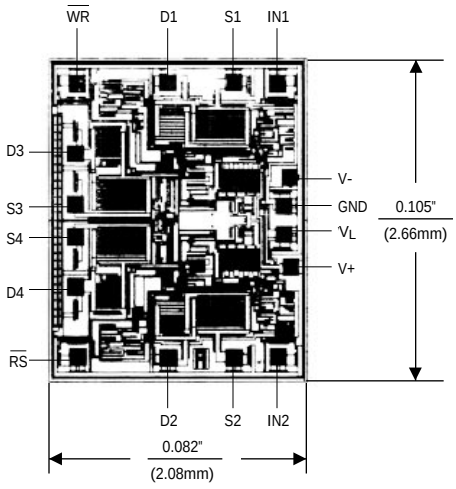
Chip Topographies

DG421



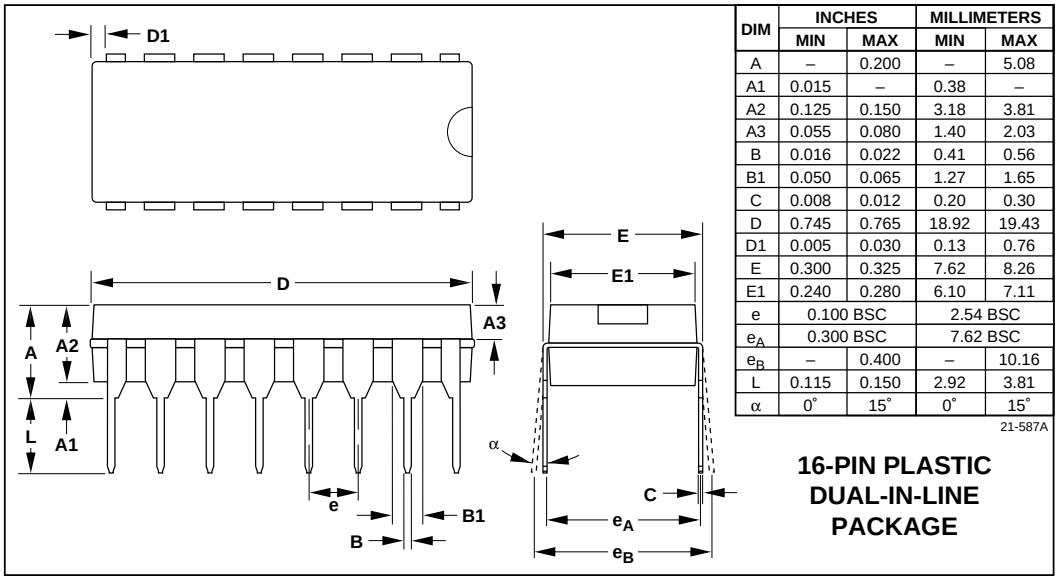
TRANSISTOR COUNT: 100
SUBSTRATE CONNECTED TO V+

DG423/DG425



TRANSISTOR COUNT: 100
SUBSTRATE CONNECTED TO V+

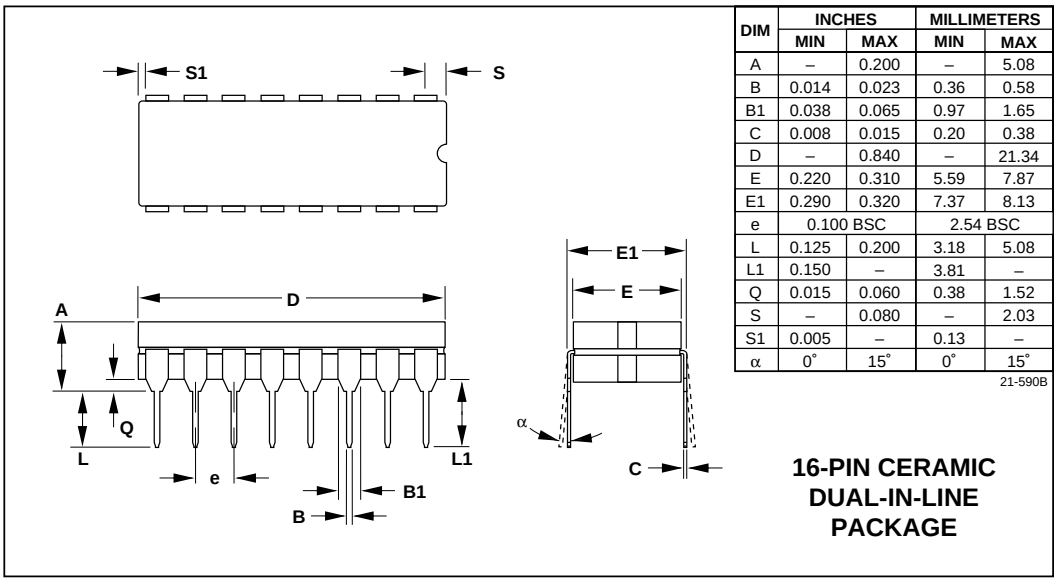
Package Information



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
A1	0.015	–	0.38	–
A2	0.125	0.150	3.18	3.81
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.050	0.065	1.27	1.65
C	0.008	0.012	0.20	0.30
D	0.745	0.765	18.92	19.43
D1	0.005	0.030	0.13	0.76
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
e_A	0.300 BSC		7.62 BSC	
e_B	–	0.400	–	10.16
L	0.115	0.150	2.92	3.81
α	0°	15°	0°	15°

21-587A

16-PIN PLASTIC DUAL-IN-LINE PACKAGE



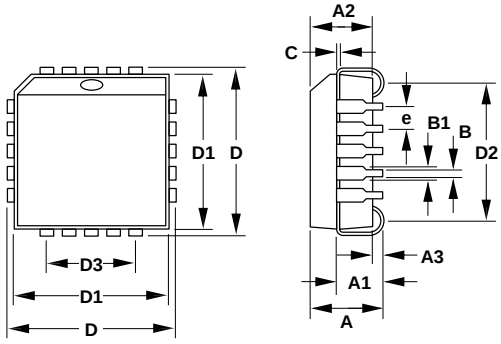
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	–	0.200	–	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
D	–	0.840	–	21.34
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100 BSC		2.54 BSC	
L	0.125	0.200	3.18	5.08
L1	0.150	–	3.81	–
Q	0.015	0.060	0.38	1.52
S	–	0.080	–	2.03
S1	0.005	–	0.13	–
α	0°	15°	0°	15°

21-590B

16-PIN CERAMIC DUAL-IN-LINE PACKAGE

Improved Low-Power, CMOS Analog Switches with Latches

Package Information (continued)



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.100	0.110	2.54	2.79
A2	0.145	0.156	3.68	3.96
A3	0.020	–	0.51	–
B	0.013	0.021	0.33	0.53
B1	0.026	0.032	0.66	0.81
C	0.009	0.011	0.23	0.28
D	0.385	0.395	9.78	10.03
D1	0.350	0.355	8.89	9.02
D2	0.290	0.330	7.37	8.38
D3	0.200 REF		5.08 REF	
e	0.050 REF		1.27 REF	

21-981A

20-PIN PLASTIC LEADED CHIP CARRIER PACKAGE