

Supertex inc.**DN3135**

N-Channel Depletion-Mode Vertical DMOS FETs

Ordering Information

$BV_{DSX} /$ BV_{DGX}	$R_{DS(ON)}$ (max)	I_{DSS} (min)	Order Number / Package		
			TO-236AB**	TO-243AA*	Die***
350V	35Ω	180mA	DN3135K1	DN3135N8	DN3135NW

* Same as SOT-89. Products shipped on 2000 piece carrier tape reels.

** Same as SOT-23. Products shipped on 3000 piece carrier tape reels.

*** Die in wafer form.

Features

- ☐ High input impedance
- ☐ Low input capacitance
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage

Applications

- ☐ Normally-on switches
- ☐ Solid state relays
- ☐ Converters
- ☐ Linear amplifiers
- ☐ Constant current sources
- ☐ Power supply circuits
- ☐ Telecom

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSX}
Drain-to-Gate Voltage	BV_{DGX}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

* Distance of 1.6 mm from case for 10 seconds.

Product marking for TO-243AA:

DN1S*

Where * = 2-week alpha date code

Product marking for SOT-23:

N1S*

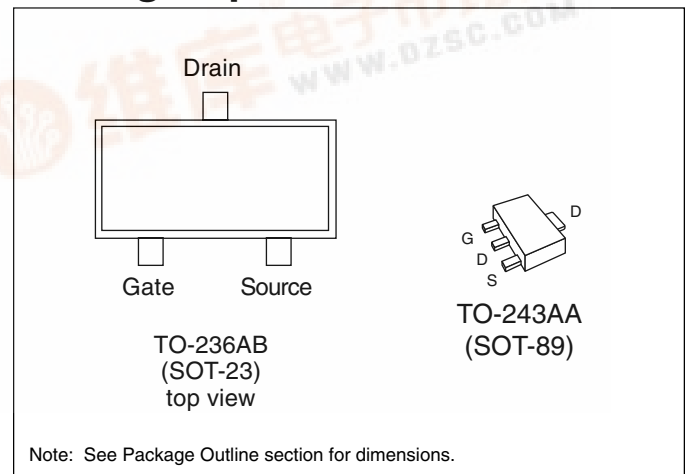
Where * = 2-week alpha date code

Advanced DMOS Technology

These low threshold depletion-mode (normally-on) transistors utilize an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_A = 25^\circ\text{C}$	θ_{JC} $^\circ\text{C/W}$	θ_{JA} $^\circ\text{C/W}$	I_{DR}^*	I_{DRM}
TO-236AB	72mA	300mA	0.36W	200	350	72mA	300mA
TO-243AA	135mA	300mA	1.3W †	34	97†	135mA	300mA

* I_D (continuous) is limited by max rated T_J .

† Mounted on FR4 board, 25mm x 25mm x 1.57mm. Significant P_D increase possible on ceramic substrate.

Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSX}	Drain-to-Source Breakdown Voltage	350			V	$V_{GS} = -5.0V$, $I_D = 100\mu A$
$V_{GS(OFF)}$	Gate-to-Source OFF Voltage	-1.5		-3.5	V	$V_{DS} = 15V$, $I_D = 10\mu A$
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with Temperature			4.5	mV/ $^\circ\text{C}$	$V_{DS} = 15V$, $I_D = 10\mu A$
I_{GSS}	Gate Body Leakage Current			100	nA	$V_{GS} = \pm 20V$, $V_{DS} = 0V$
$I_{D(OFF)}$	Drain-to-Source Leakage Current			1.0	μA	$V_{GS} = -5.0V$, $V_{DS} = \text{Max Rating}$
				1.0	mA	$V_{GS} = -5.0V$, $V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
I_{DSS}	Saturated Drain-to-Source Current	180			mA	$V_{GS} = 0V$, $V_{DS} = 15V$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			35	Ω	$V_{GS} = 0V$, $I_D = 150mA$
				35		$V_{GS} = -0.8V$, $I_D = 50mA$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.1	%/ $^\circ\text{C}$	$V_{GS} = 0V$, $I_D = 150mA$
G_{FS}	Forward Transconductance	140			m Ω	$I_D = 100mA$, $V_{DS} = 10V$
C_{ISS}	Input Capacitance		60	120	pF	$V_{GS} = -5.0V$, $V_{DS} = 25V$, $f = 1.0MHz$
C_{OSS}	Common Source Output Capacitance		6.0	15		
C_{RSS}	Reverse Transfer Capacitance		3.0	10		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = 25V$, $I_D = 150mA$, $R_{GEN} = 25\Omega$, $V_{GS} = 0V \text{ to } -10V$
t_r	Rise Time			15		
$t_{d(OFF)}$	Turn-OFF Delay Time			15		
t_f	Fall Time			20		
V_{SD}	Diode Forward Voltage Drop			1.8	V	$V_{GS} = -5.0V$, $I_{SD} = 150mA$
t_{rr}	Reverse Recovery Time		800		ns	$V_{GS} = -5.0V$, $I_{SD} = 150mA$

Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

