



New Product

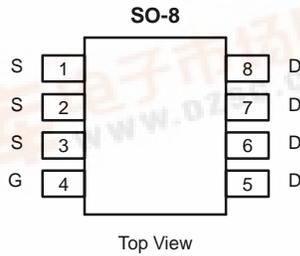
**Si9410BDY**  
Vishay Siliconix

## N-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
30	0.024 @ $V_{GS} = 10$ V	8.1
	0.033 @ $V_{GS} = 4.5$ V	6.9

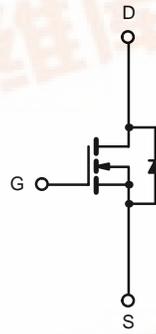
### FEATURES

- TrenchFET® Power MOSFETS



Top View

Ordering Information: Si9410BDY  
Si9410BDY-T1 (with Tape and Reel)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		$V_{DS}$	30		V
Gate-Source Voltage		$V_{GS}$	$\pm 20$		
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) <sup>a</sup>	$T_A = 25^\circ\text{C}$	$I_D$	8.1	6.2	A
	$T_A = 70^\circ\text{C}$		6.5	5.0	
Pulsed Drain Current (10 $\mu\text{s}$ Pulse Width)		$I_{DM}$	30		
Continuous Source Current (Diode Conduction) <sup>a</sup>		$I_S$	2.1	1.2	
Maximum Power Dissipation <sup>a</sup>	$T_A = 25^\circ\text{C}$	$P_D$	2.5	1.5	W
	$T_A = 70^\circ\text{C}$		1.6	0.9	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient <sup>a</sup>	$t \leq 10$ sec	$R_{thJA}$	40	50	$^\circ\text{C/W}$
	Steady State		70	85	
Maximum Junction-to-Foot	Steady State	$R_{thJF}$	20	24	

Notes:  
a. Surface Mounted on 1" x 1" FR4 Board.

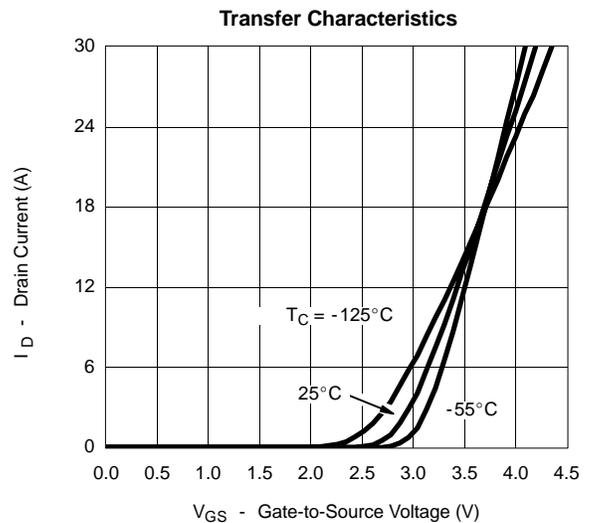
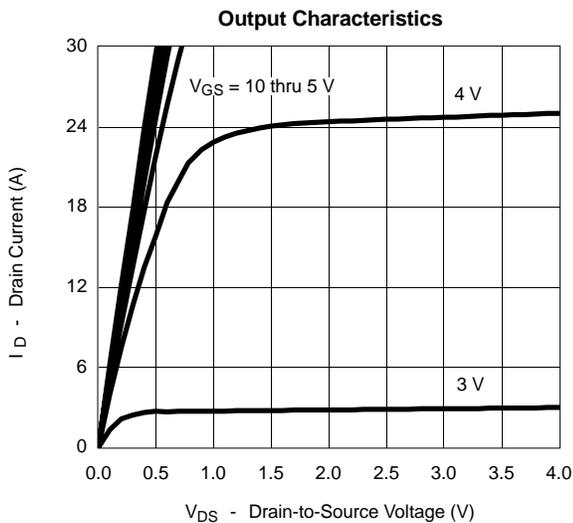


SPECIFICATIONS (T <sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.0		3.0	V
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C			5	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ 5 V, V <sub>GS</sub> = 10 V	30			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 8.1 A		0.019	0.024	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 6.9 A		0.026	0.033	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 8.1 A		20		S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = 2.1 A, V <sub>GS</sub> = 0 V		0.8	1.2	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = 15 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 8.1 A		15	23	nC
Gate-Source Charge	Q <sub>gs</sub>			3.2		
Gate-Drain Charge	Q <sub>gd</sub>			2.5		
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = 15 V, R <sub>L</sub> = 15 Ω I <sub>D</sub> = 1 A, V <sub>GEN</sub> = 10 V, R <sub>G</sub> = 6 Ω		10	15	ns
Rise Time	t <sub>r</sub>			15	25	
Turn-Off Delay Time	t <sub>d(off)</sub>			30	45	
Fall Time	t <sub>f</sub>			11	20	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>		I <sub>F</sub> = 2.1 A, di/dt = 100 A/μs		25	

**Notes**

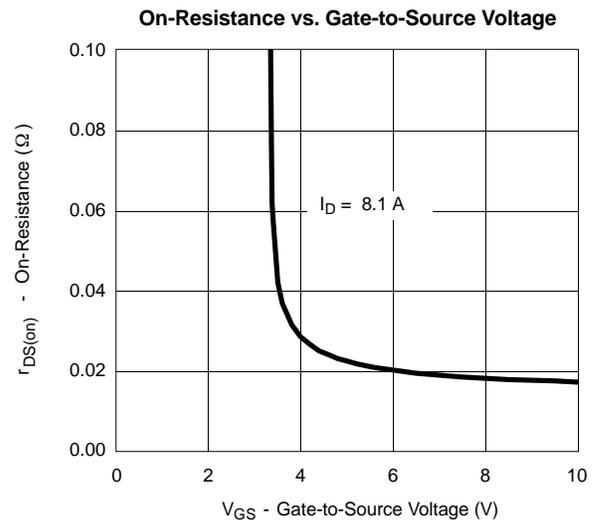
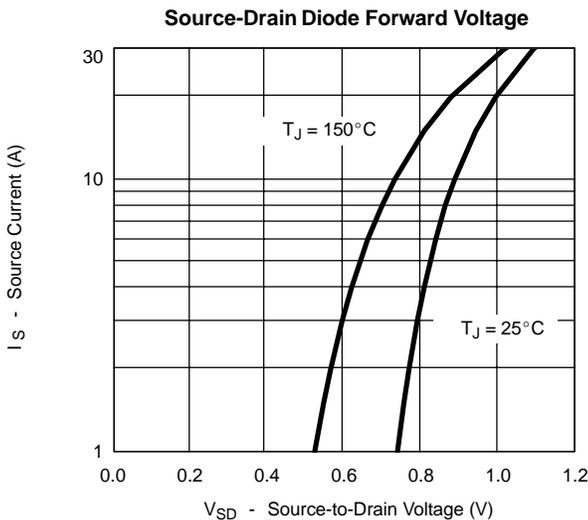
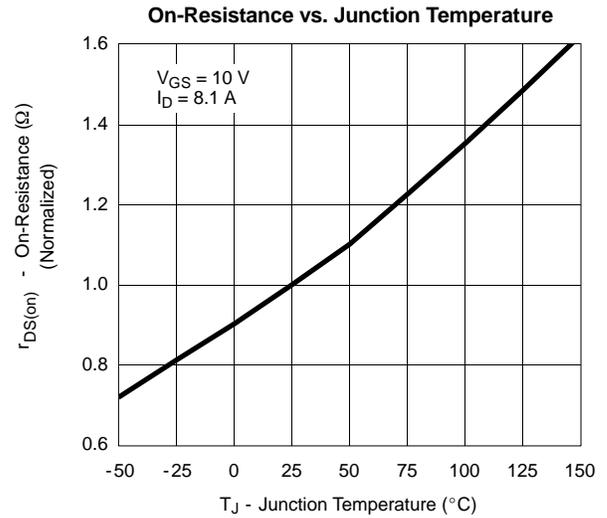
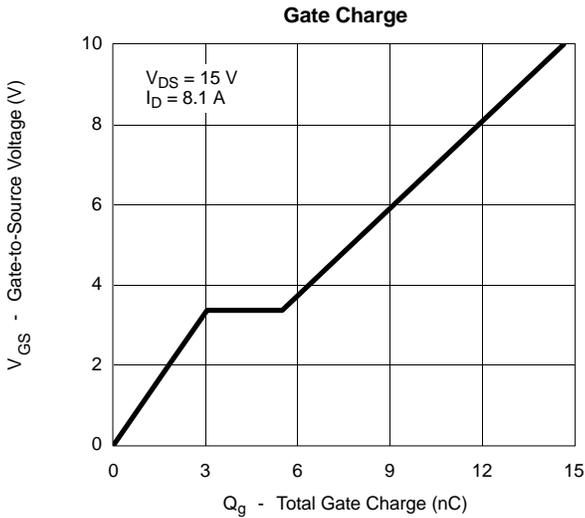
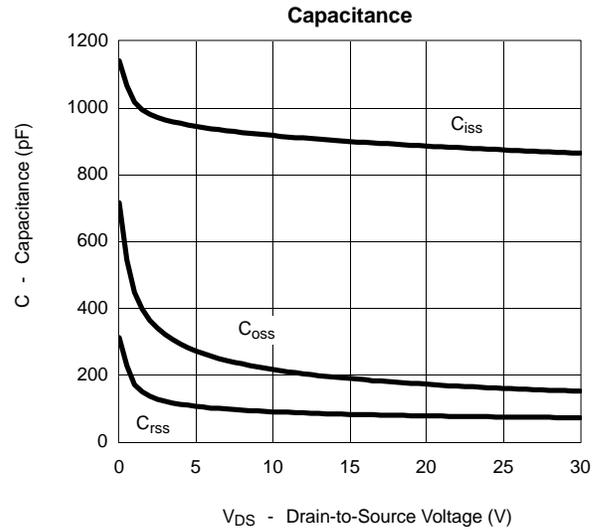
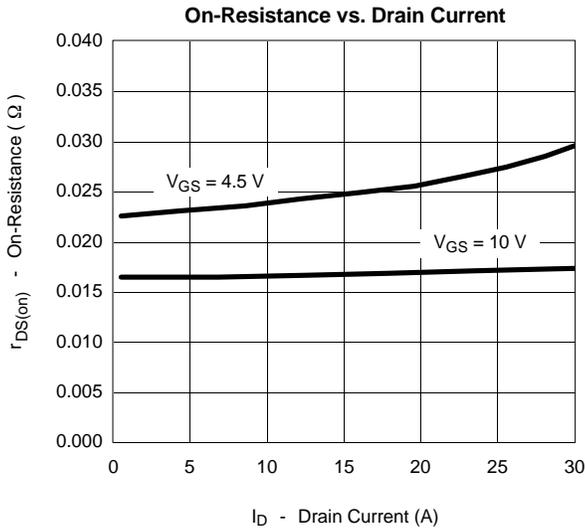
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Guaranteed by design, not subject to production testing.

### TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)



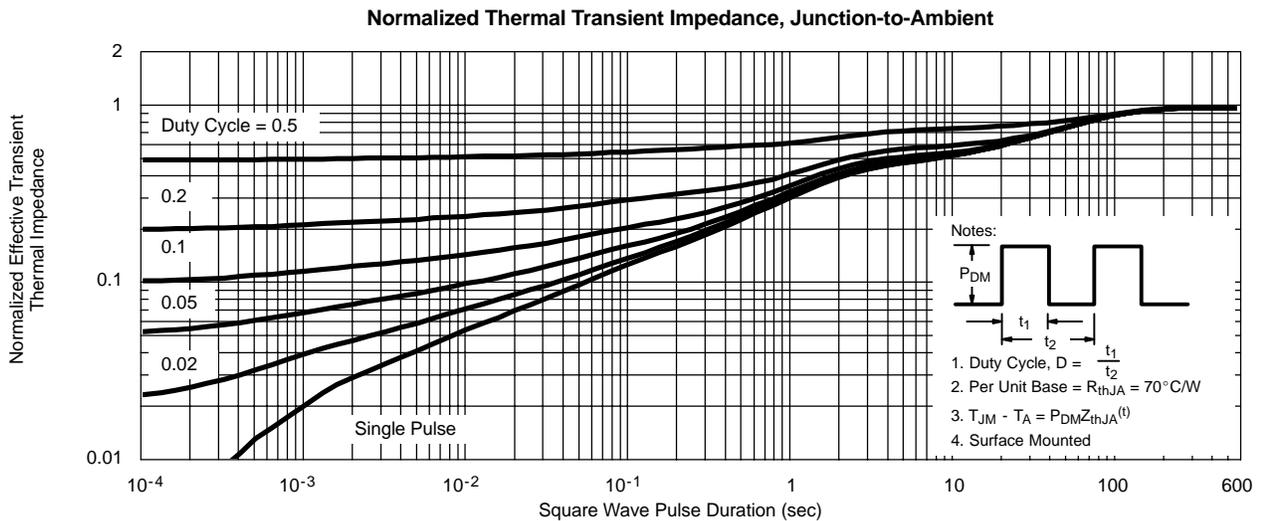
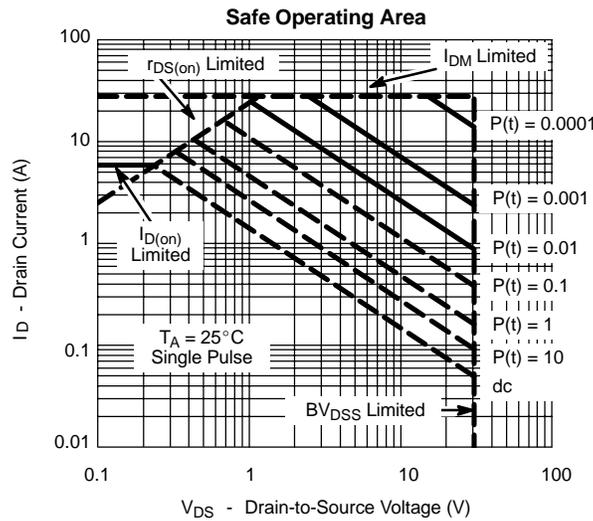
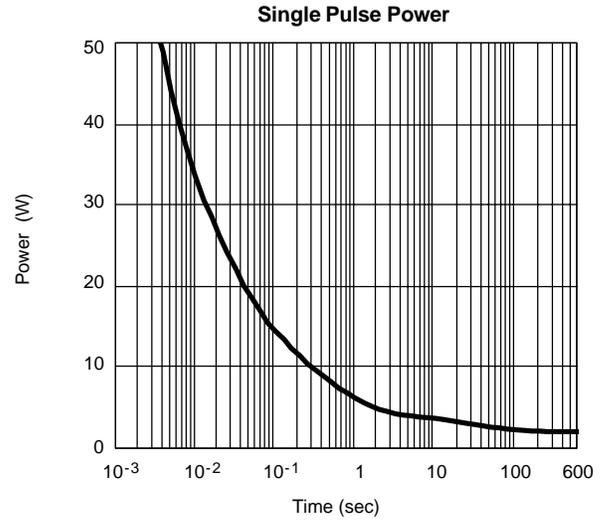
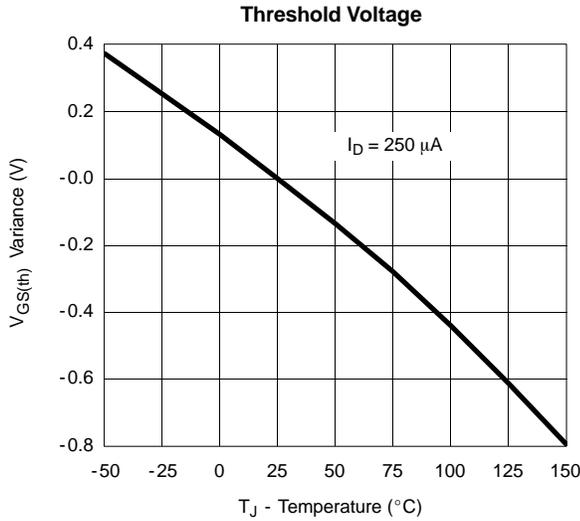


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