



TDA7478

SINGLE CHIP RDS DEMODULATOR

1 FEATURES

- VERY HIGH RDS DEMODULATION QUALITY WITH IMPROVED DIGITAL SIGNAL PROCESSING
- HIGH PERFORMANCE, 57KHz BANDPASS FILTER (8th ORDER)
- FILTER ADJUSTMENT FREE AND WITHOUT EXTERNAL COMPONENTS
- PURELY DIGITAL RDS DEMODULATION WITHOUT EXTERNAL COMPONENTS
- RDS SIGNAL QUALITY OUTPUT
- 4.332MHz CRYSTAL OSCILLATOR(8.664MHz OPTIONAL)
- LOW NOISE CMOS TECHNOLOGY
- LOW RADIATION

2 DESCRIPTION

The TDA7478 recovers the additional inaudible RDS information which is transmitted by FM radio broadcasting stations and operates in accordance with the

Figure 1. Packages



Table 1. Order Codes

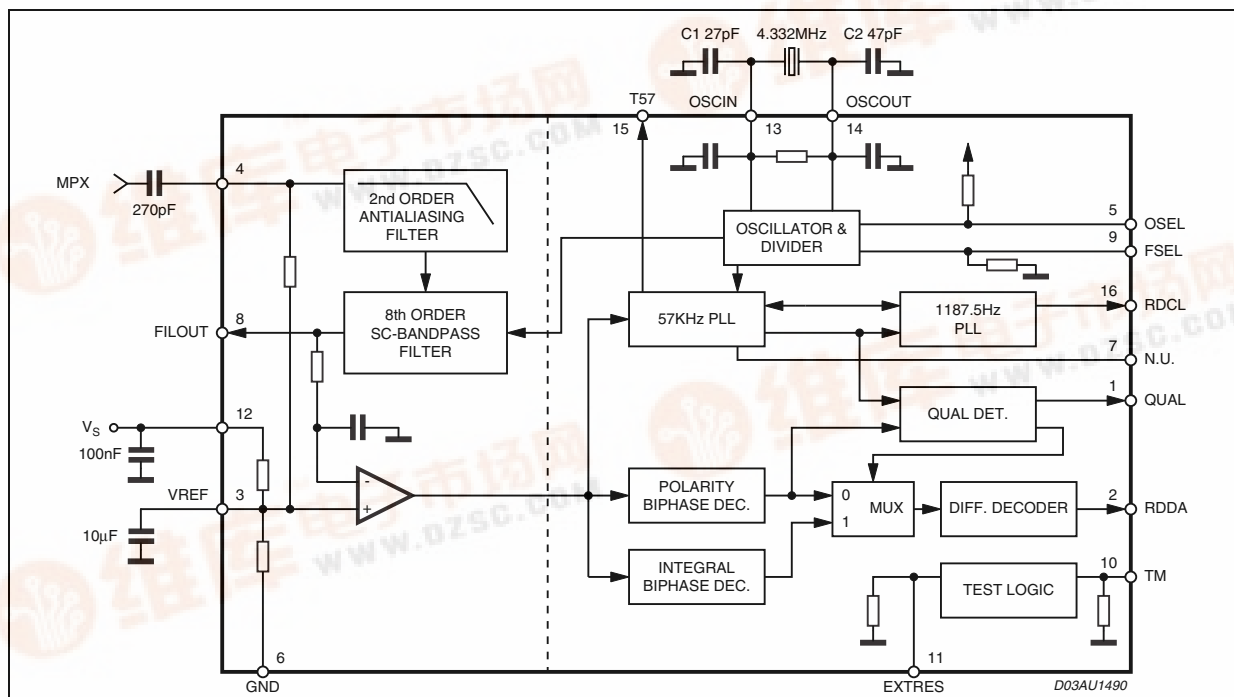
Part Number	Package
TDA7478D	SO16
E-TDA7478AD	TSSOP16

EBU (European Broadcasting Union) specifications.

The device is made up of two sections: a cascaded antialiasing + switched capacitors 8th bandpass filter for precise RDS band selection and a demodulating section that performs the extraction of RDS data stream (RDDA) and clock (RDCL), to be further processed by a suitable RDS decoder.

Output for RDS signal quality is also present.

Figure 2. Block Diagram



TDA7478

Table 2. Pin Description

No pin	Name	Description
1	QUAL	Output for signal quality indication (High = good)
2	RDDA	RDS data output
3	VREF	Reference voltage
4	MPX	RDS input signal
5	OSEL	Oscillator selector pin: - open, closed to V_S = quartz oscillator - closed to GND=external driven
6	GND	Ground
7	N.U.	Not Used (to be left open)
8	FILOUT	Filter output
9	FSEL	Frequency selector pin: - open = 4.332MHz - closed to V_S = 8.664MHz
10	TM	Test mode pin: - open = normal operation - closed to V_S = testmode
11	EXTRES	Reset pin: - open=run mode - closed to V_S = reset condition
12	V_S	Supply voltage
13	OSCIN	Oscillator input
14	OSCOUT	Oscillator output
15	T57	Testing output pin: 57kHz clock output
16	RDCL	RDS clock output 1187.5Hz

Figure 3. Pin Connection (Top view)

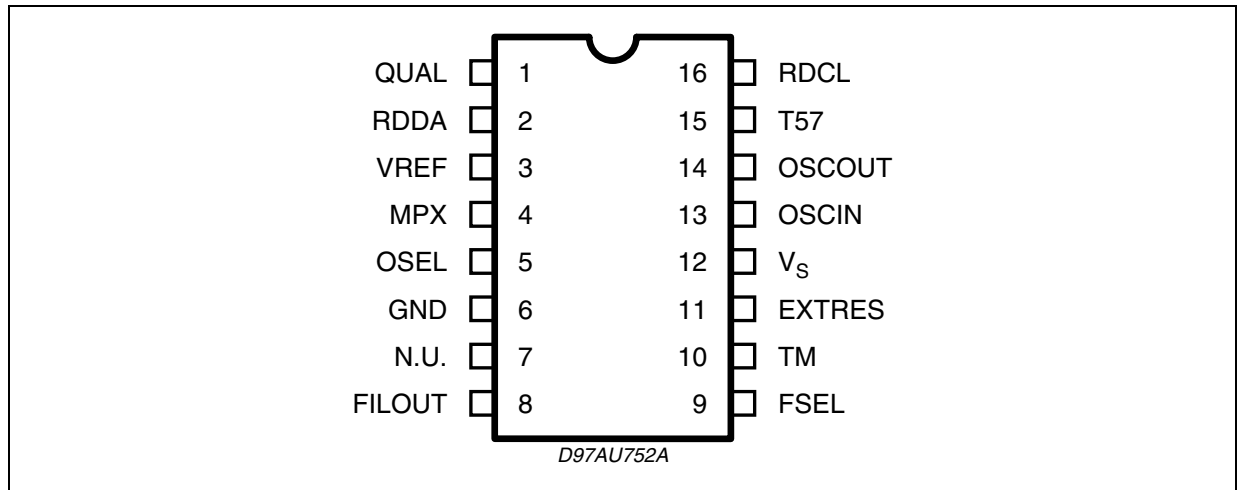


Table 3. Thermal Data

Symbol	Description	Value	Unit
$R_{th\ j-case}$	Thermal Resistance Junction-case Max.	200	$^{\circ}C/W$

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V _S	Supply Voltage	-0.3 to 7	V
T _{op}	Operating Temperature Range	-40 to 85	°C
T _{stg}	Storage Temperature	-55 to 150	°C

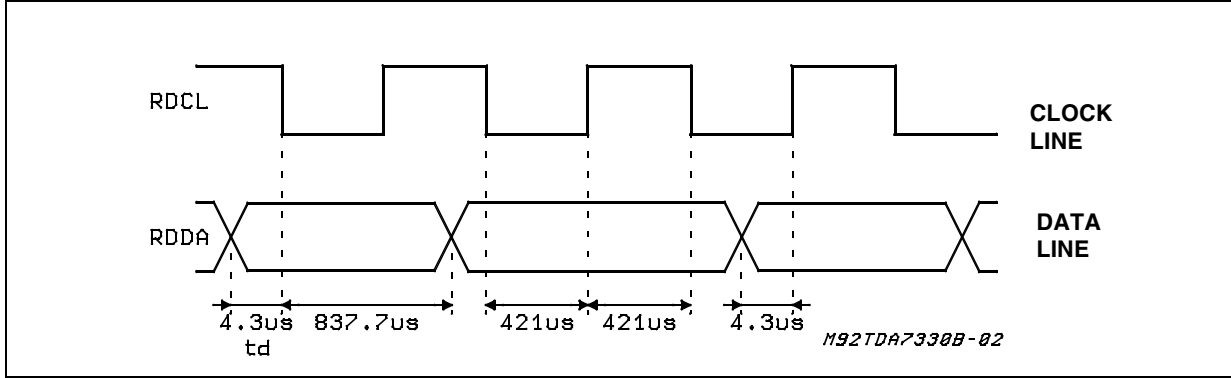
Table 5. Electrical Characteristics

(T_{amb} = 25°C, V_S = 5V, unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V _S	Supply voltage		4.5	5	5.5	V
I _S	Supply current			7.5	12.0	mA
FILTER						
f _C	Center frequency		56.6	57	57.4	kHz
BW	3dB Bandwidth		2.5	3	3.5	kHz
G	Gain	f = 57kHz	17	20	23	dB
A	Attenuation	Δf ± 4kHz		22		dB
		f = 38kHz		60		dB
		f = 67kHz		45		dB
R _I	Input impedance of MPX			120		KΩ
R _L	Load impedance on FILOUT		1			MΩ
S/N	Signal to noise ratio	V _{IN} = 3mVRMS	30	40		dB
V _{IN}	MPX input signal	f = 19kHz; T ₃ ≤ 40dB ⁽¹⁾ f = 57kHz (RDS)			1000 50	mVRMS mVRMS
S _{RDS}	RDS Detection Sensitivity		1			mVrms
S _{ARI}	ARI Detection Sensitivity		3			mVrms
V _{REF}	Reference			V _S /2		V
DEMODULATOR						
Input pins (EXTRES, FSEL, TM)			all with internal pull down resistor			
Input pin (OSEL)			with internal pull up resistor			
I _{PD}	Input Current	V _{IN} = 5V (pull-down input)	15		30	μA
I _{PU}	Input Current	V _{IN} = 0V (pull-up input)	-25		-10	μA
V _{IH}	Input voltage high		0.7 · V _S	0.8 · V _S		V
V _{IL}	Input voltage low			0.2 · V _S	0.3 · V _S	V
Output pins (RDCL, RDDA, QUAL, T57)						
V _{OH}	Output voltage high	I _L = 0.5mA	4	4.6		V
V _{OL}	Output voltage low	I _L = 0.5mA		0.4	1	V
OSCILLATOR						
V _{CLL}	Input level OSCIN pin	OSEL = open circuit			1	V
V _{CLH}	Input level OSCIN pin	OSEL = open circuit	4			V
	Amplitude OSCOUT	OSEL = open circuit		4.5		V
V _{PP}	Amplitude OSCIN (for external drive)	OSEL = GND, f = 4.332MHz		100		mVpp
		OSEL = GND, f = 8.664MHz		120		mVpp

(1) The 3rd harmonic (57kHz) must be less than -40dB with respect to the input signal plus gain.

Figure 4. RDS timing diagram



3 OUTPUT TIMING

The RDS (1187.5Hz) output clock on RDCL line is synchronized to the incoming data. According to the internal PLL lock condition data change can result on the falling or on the rising clock edge. (see Fig. 1) Whichever clock edge is used by the decoder (rising or falling edge) the data will remain valid for 416.7 µs after the clock transition.

4 OSCILLATOR CONTROLS (FSEL, OSEL)

Two different crystal frequencies can be used. The adaption of the internal clock divider to the external crystal is achieved via the input pin FSEL. See the following table for reference:

Table 6.

Crystal	FSEL (pin configuration)
4.332MHz	connected to GND or open
8.664MHz	connected to Vs

A special mode is introduced to reduce EMI. With pin OSEL connected to GND the internal oscillator is switched off and an external sinusoidal frequency could be applied on OSCIN. The peak to peak voltage of this signal can be reduced down to 60mV.

In this mode the frequency selection via FSEL is still active.

Suggested values of C1 and C2 are shown in the following table:

Table 7.

Crystal	C1	C2
4.332MHz	27pF	47pF
8.664MHz	27pF	-

Figure 5. SO16 Mechanical Data & Package Dimensions

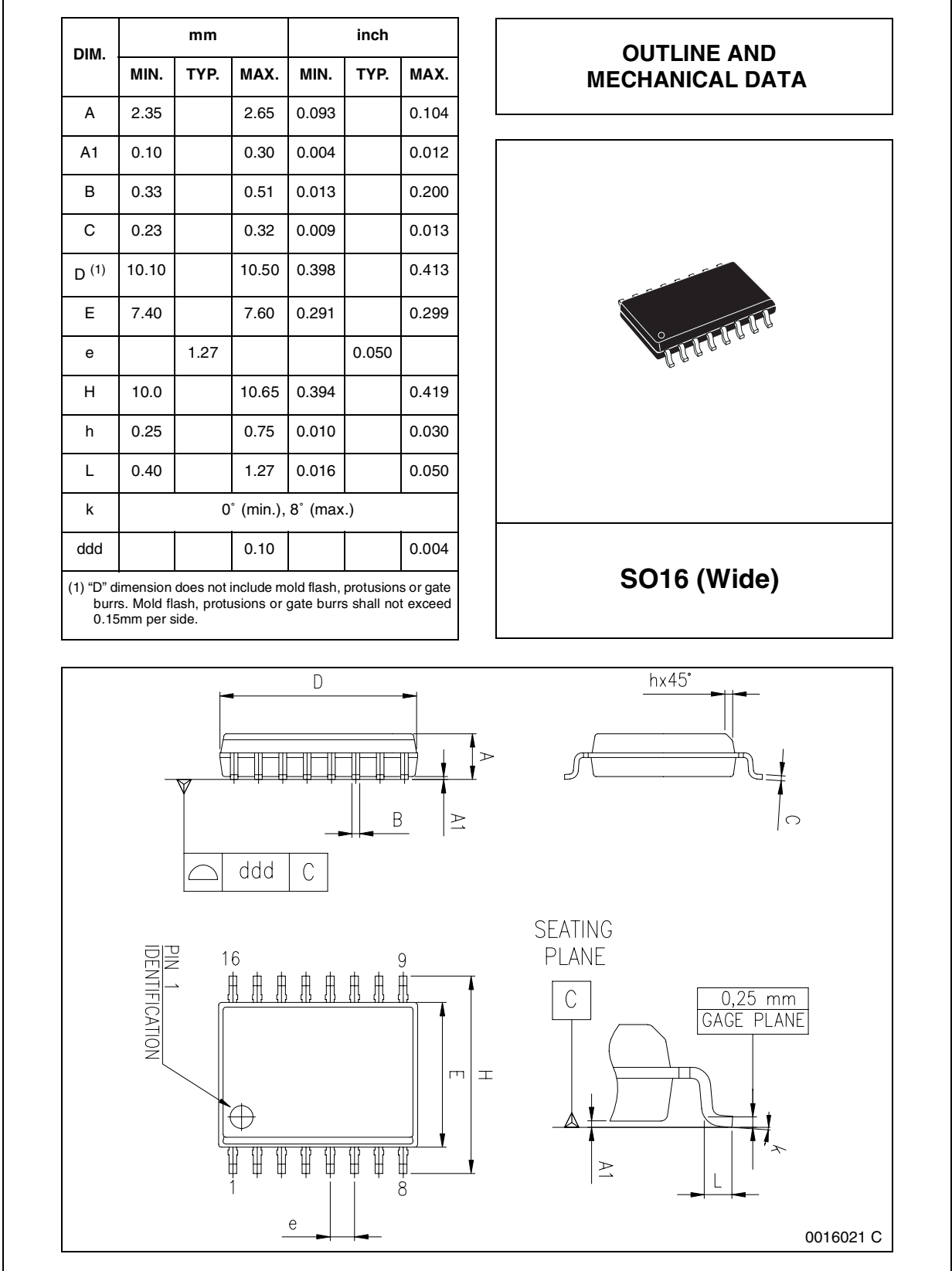


Figure 6. TSSOP16 Mechanical Data & Package Dimensions

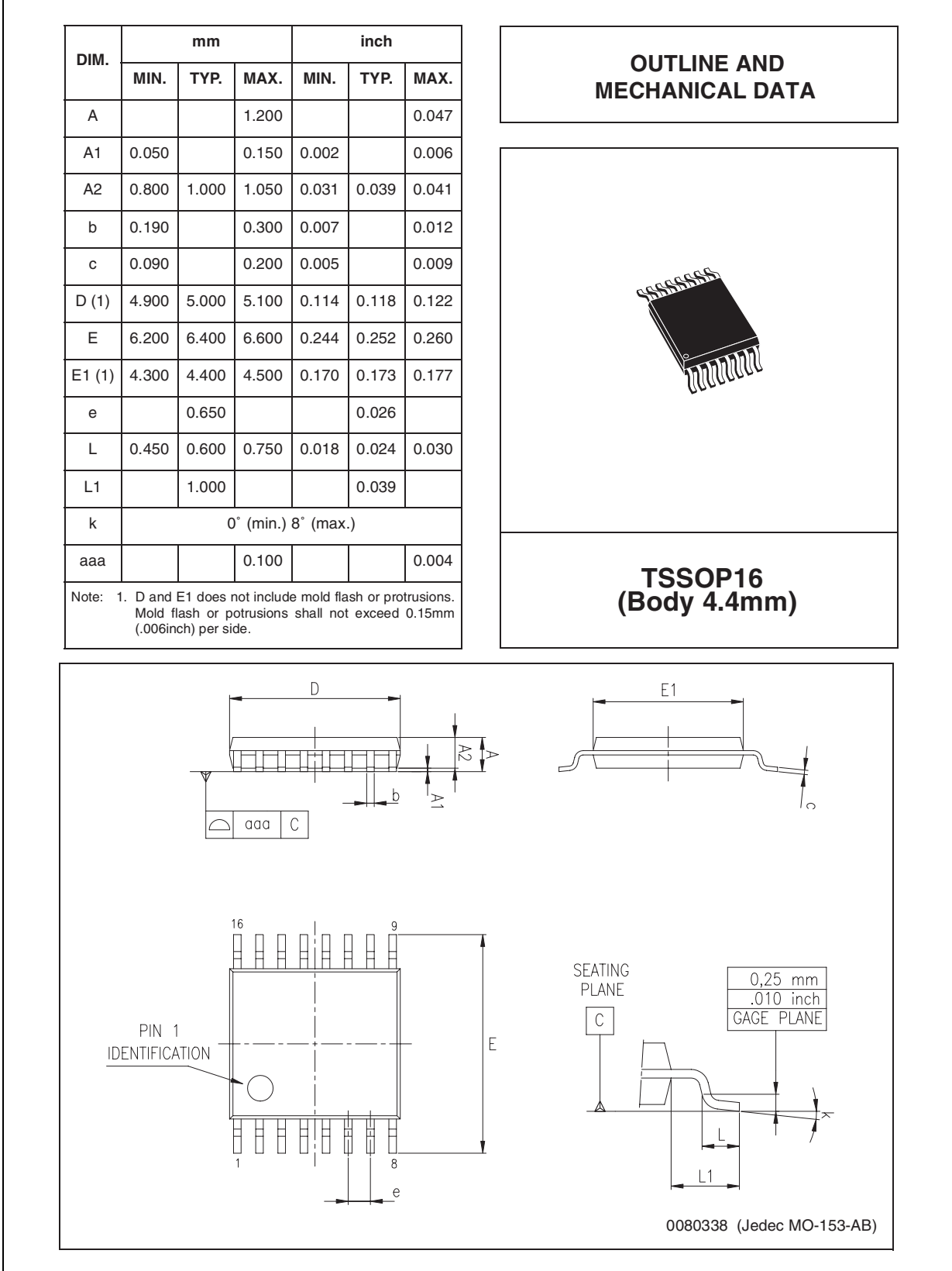


Table 8. Revision History

Date	Revision	Description of Changes
July 2004	1	First Issue
November 2004	2	Add in the table 5 "RDS and ARI Detection Sensitivity" parameters.

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