



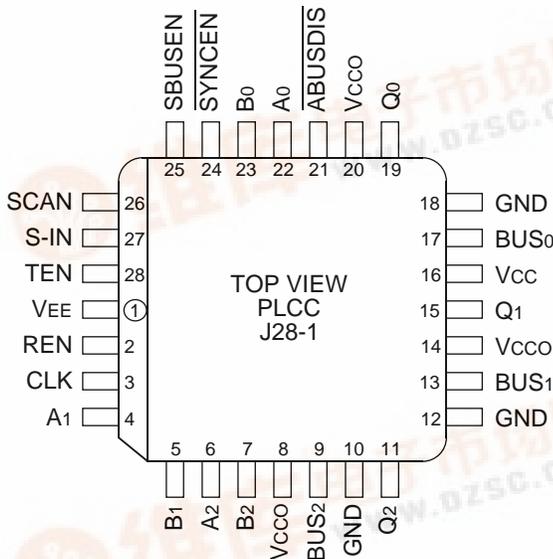
3-BIT SCANNABLE REGISTERED BUS TRANSCEIVER

SY10E337
SY100E337

FEATURES

- 1500ps max. clock to bus (data transmit)
- 1000ps max. clock to Q (data receive)
- Extended 100E VEE range of -4.2V to -5.5V
- 25Ω cutoff bus outputs
- 50Ω receiver outputs
- Scannable implementation of E336
- Synchronous and asynchronous bus enables
- Non-inverting data path
- Bus outputs feature internal edge slow-down capacitors
- Additional package ground pins
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E337
- Available in 28-pin PLCC package

PIN CONFIGURATION



DESCRIPTION

The SY10/100E337 are 3-bit registered bus transceivers with scan designed for use in new, high-performance ECL systems. The bus outputs (BUS₀–BUS₂) are designed to drive a 25Ω bus; the receive outputs (Q₀–Q₂) are designed for 50Ω. The bus outputs feature a normal logic HIGH level (V_{OH}) and a cutoff LOW level of -2.0V and the output emitter-follower is “off”, presenting a high impedance to the bus. The bus outputs also feature edge slow-down capacitors.

Both drive and receive sides feature the same logic, including a loopback path to hold data. The LOAD/HOLD function is controlled by Transmit Enable (TEN) and Receive Enable (REN) on the transmit and receive sides, respectively, with a HIGH selecting LOAD. The implementation of the E337 Receive Enable differs from that of the E336.

A synchronous bus enable (SBUSEN) is provided for normal, non-scan operation. The asynchronous bus disable (ABUSDIS) disables the bus for scan mode.

The SYNCEN input allows either synchronous or asynchronous re-enabling after disabling with ABUSDIS. An alternative use is asynchronous-only operation with ABUSDIS, in which case SYNCEN is tied LOW. SYNCEN is implemented as an overriding SET control to the enable flip-flop.

Scan mode is selected by a logic HIGH at the SCAN input. Scan input data is shifted in through S-IN, and output data appears at the Q₂ output.

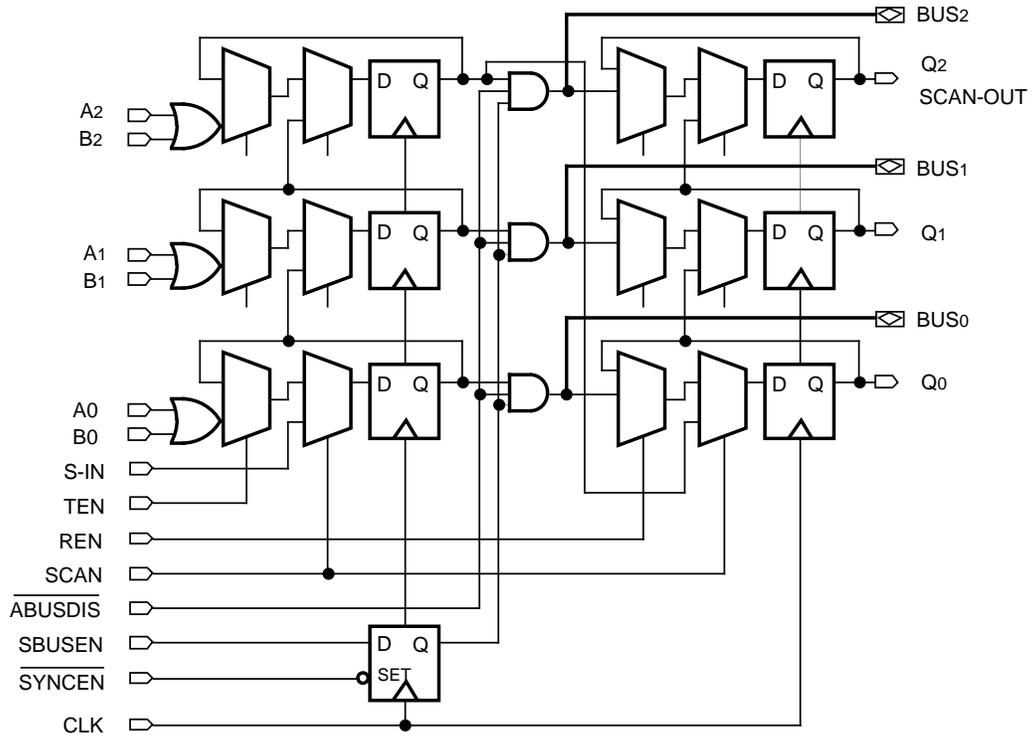
All registers are clocked on the rising edge of CLK. Additional lead-frame grounding is provided through the ground pins (GND) which should be connected to 0V. The GND pins are not electrically connected to the chip.

PIN NAMES

Pin	Function
A ₀ –A ₂	Data Inputs A
B ₀ –B ₂	Data Inputs B
S-IN	Serial (Scan) Data Input
TEN, REN	LOAD/HOLD Controls
SCAN	Scan Control
ABUSDIS	Asynchronous Bus Disable
SBUSEN	Synchronous Bus Enable
SYNCEN	Synchronous Enable Control
CLK	Clock
BUS ₀ –BUS ₂	25Ω Cutoff BUS Outputs
Q ₀ –Q ₂	Receive Data Outputs (Q ₂ serves as SCAN_OUT in scan mode)
VCCO	Vcc to Output



BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CC0} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition	
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
V _{CUT}	Cut-off Output Voltage	-2.10	—	-2.03	-2.10	—	-2.03	-2.10	—	-2.03	V	1	
I _{IH}	Input HIGH Current All Other Inputs	—	—	150	—	—	150	—	—	150	μA	—	
I _{EE}	Power Supply Current	—	145	174	—	145	174	—	145	174	mA	—	
		10E	—	145	174	—	145	174	—	145			174
		100E	—	145	174	—	125	174	—	167			200

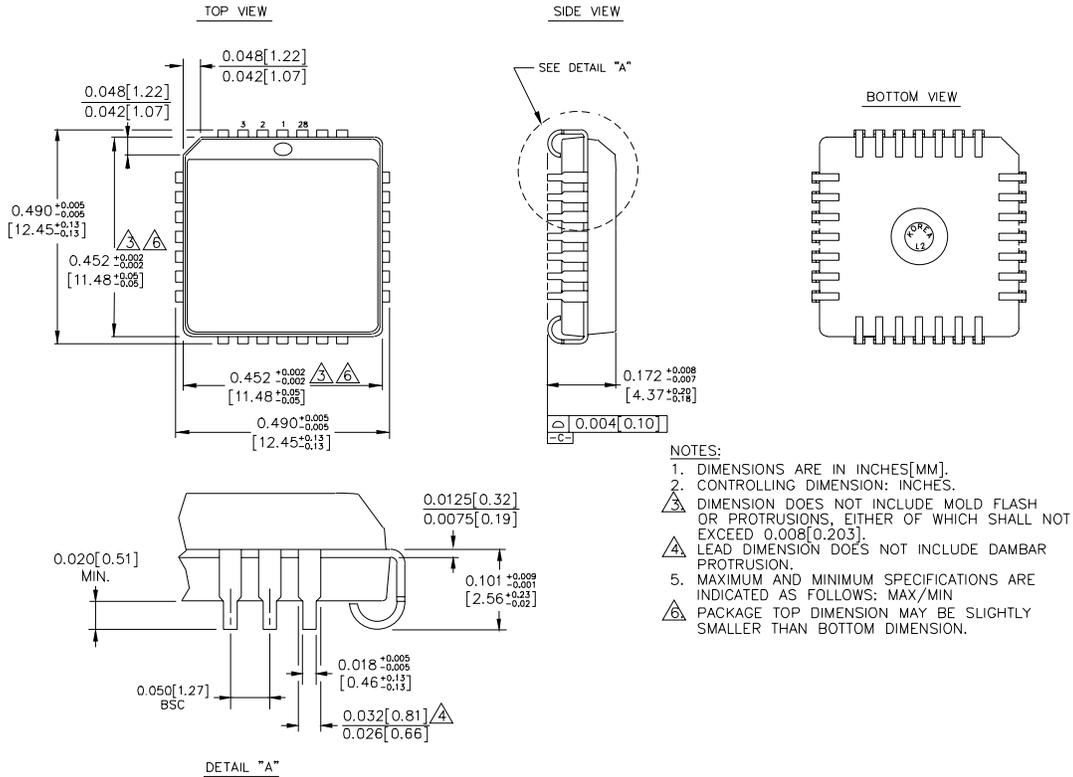
NOTE:1. Applies to BUS outputs only. Measured with V_{TT} = -2.10V.**AC ELECTRICAL CHARACTERISTICS**V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CC0} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{PLH} t _{PHL}	Propagation Delay to Output CLK to Q CLK to BUS ABUSDIS SYNCEN	450 800 500 800	— — — —	1000 1800 1500 1800	450 800 500 800	— — — —	1000 1800 1500 1800	450 800 500 800	— — — —	1000 1800 1500 1800	ps	—
t _s	Set-up Time BUS SBUSEN Data, S-IN TEN, REN, SCAN	350 100 400 550	— — — —	— — — —	350 100 400 550	— — — —	— — — —	350 100 400 550	— — — —	— — — —	ps	—
t _H	Hold Time BUS SBUSEN Data, S-IN TEN, REN, SCAN	350 500 350 200	— — — —	— — — —	350 500 350 200	— — — —	— — — —	350 500 350 200	— — — —	— — — —	ps	—
t _{PW}	Minimum Pulse Width	400	—	—	400	—	—	400	—	—	ps	—
t _r t _f	Rise/Fall Time 20% to 80% (Q _n) 20% to 80% (BUS _n Rise) 20% to 80% (BUS _n Fall)	300 500 300	— — —	800 1000 800	300 500 300	— — —	800 1000 800	300 500 300	— — —	800 1000 800	ps	—

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E337JC	J28-1	Commercial
SY10E337JCTR	J28-1	Commercial
SY100E337JC	J28-1	Commercial
SY100E337JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



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