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NTE9672 Integrated Circuit High Threshold Logic (HTL) Quad, 2-Input NAND Gate

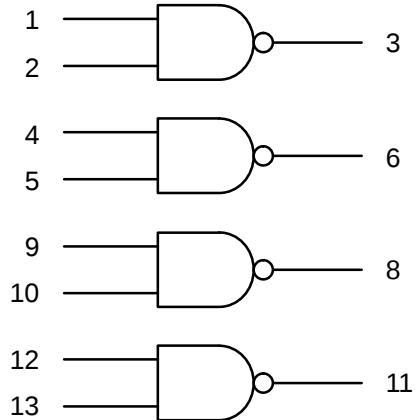
Description:

This NTE9672 is a Quad, 2-Input NAND gate with active output pull-up in a 14-Lead DIP style package. The active output arrangement allows the circuit to handle capacitive loads at a higher speed than is obtainable with a passive pullup configuration. Additionally, the impedance in the high state is considerably less, and consequently makes this device more immune to electrical noise. The active output configuration also allows for a more powerful arrangement to interface with discrete components.

Electrical Characteristics: ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage	V_{OL}	$I_{OL} = 12\text{mA}$, $V_{IH} = 8.5\text{V}$, $V_{CCL} = 14\text{V}$	—	—	1.5	V
	V_{OH}	$I_{OH} = -0.03\text{mA}$, $V_{IL} = 6.5\text{V}$, $V_{CC} = 15\text{V}$, $V_{CCL} = 14\text{V}$	12.5	—	—	V
Short-Circuit Current	I_{SC}	$V_{CCH} = 16\text{V}$	-6.5	—	-15	mA
Reverse Current	I_R	$V_R = 16\text{V}$, $V_{CCL} = 14\text{V}$	—	—	2	μA
Output Leakage Current	I_{CEX}	$V_{CEX} = 16\text{V}$	—	—	100	μA
Forward Current	I_F	$V_F = 1.5\text{V}$, $V_R = 16\text{V}$, $V_{CCH} = 16\text{V}$	—	—	-1.2	mA
Power Drain Current Total Device	I_{CCL}	$V_{CCH} = 16\text{V}$	—	—	6	mA
	I_{CCH}		—	—	20	mA
Switching Times	t_{1-3+}	$I_{OL} = 12\text{mA}$ (Pulse In), $I_{OH} = -0.03\text{mA}$ (Pulse Out), $V_{CC} = 15\text{V}$	—	—	200	ns
	t_{1+3-}		—	—	100	ns

Logic Symbol



Positive Logic: $3 = \overline{1 \bullet 2}$
 Input Loading Factor = 1
 Output Loading Factor = 10
 Propagation Delay Time = 110ns Typ
 Typical Total Power Dissipation
 Input High = 176mW
 Inputs Low = 52mW

Pin Connection Diagram

