

Freescale Semiconductor
 Technical Data

MC100ES6139
 Rev 3, 06/2005

3.3 V ECL/PECL/HSTL/LVDS ÷2/4, ÷4/5/6 Clock Generation Chip

The MC100ES6139 is a low skew ÷2/4, ÷4/5/6 clock generation chip designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, LVPECL input signals. In addition, by using the V_{BB} output, a sinusoidal source can be AC coupled into the device. If a single-ended input is to be used, the V_{BB} output should be connected to the CLK input and bypassed to ground via a 0.01 µF capacitor.

The common enable (\overline{EN}) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple ES6139s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one ES6139, the MR pin need not be exercised as the internal divider design ensures synchronization between the ÷2/4 and the ÷4/5/6 outputs of a single device. All V_{CC} and V_{EE} pins must be externally connected to power supply to guarantee proper operation.

The 100ES Series contains temperature compensation.

Features

- Maximum Frequency >1.0 GHz Typical
- 50 ps Output-to-Output Skew
- PECL Mode Operating Range: V_{CC} = 3.135 V to 3.8 V with V_{EE} = 0 V
- ECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -3.135 V to -3.8 V
- Open Input Default State
- Synchronous Enable/Disable
- Master Reset for Synchronization of Multiple Chips
- V_{BB} Output
- LVDS and HSTL Input Compatible
- 20-Lead Pb-Free Package Available

MC100ES6139



DT SUFFIX
 20-LEAD TSSOP PACKAGE
 CASE 948E-03

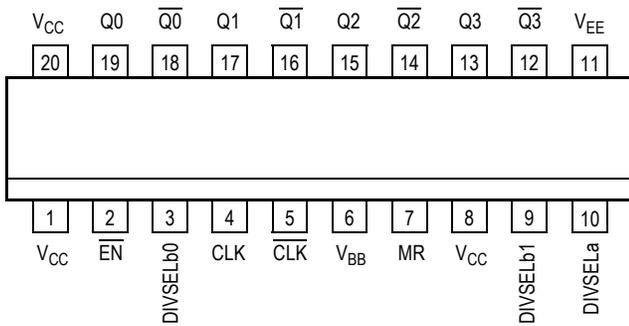


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ORDERING INFORMATION

Device	Package
MC100ES6139DT	TSSOP-20
MC100ES6139DTR2	TSSOP-20
MC100ES6139EJ	TSSOP-20 (Pb-Free)
MC100ES6139EJR2	TSSOP-20 (Pb-Free)





Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

Figure 1. 20-Lead Pinout (Top View)

Table 1. Pin Description

Pin	Function
CLK ⁽¹⁾ , $\overline{\text{CLK}}$ ⁽¹⁾	ECL Diff Clock Inputs
$\overline{\text{EN}}$ ⁽¹⁾	ECL Sync Enable
MR ⁽¹⁾	ECL Master Reset
V_{BB}	ECL Reference Output
Q0, Q1, $\overline{\text{Q0}}$, $\overline{\text{Q1}}$	ECL Diff $\div 2/4$ Outputs
Q2, Q3, $\overline{\text{Q2}}$, $\overline{\text{Q3}}$	ECL Diff $\div 4/5/6$ Outputs
DIVSELa ⁽¹⁾	ECL Freq. Select Input $\div 2/4$
DIVSELb0 ⁽¹⁾	ECL Freq. Select Input $\div 4/5/6$
DIVSELb1 ⁽¹⁾	ECL Freq. Select Input $\div 4/5/6$
V_{CC}	ECL Positive Supply
V_{EE}	ECL Negative Supply

1. Pins will default low when left open.

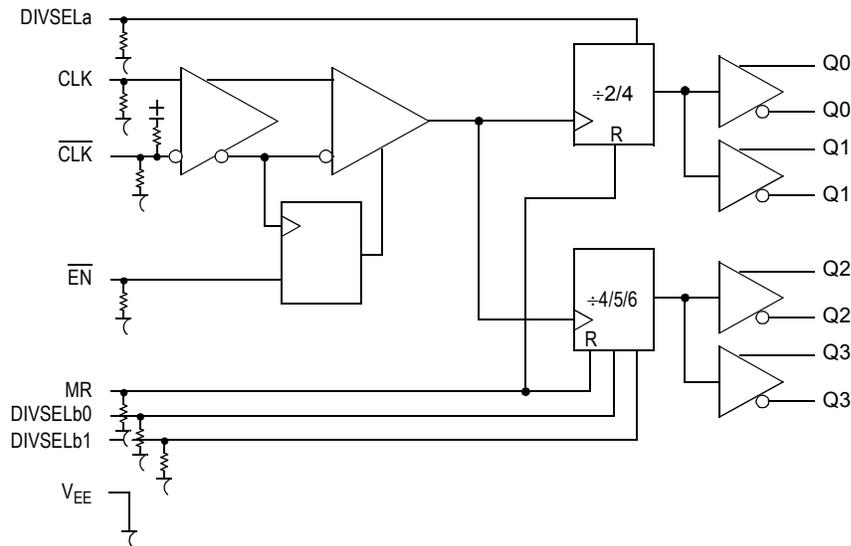


Figure 2. Logic Diagram

Table 2. Function Tables

CLK	EN	MR	Function
Z	L	L	Divide
ZZ	H	L	Hold Q0:3
X	X	H	Reset Q0:3

X = Don't Care
 Z = Low-to-High Transition
 ZZ = High-to-Low Transition

DIVSELa		Q0:1 Outputs
L		Divide by 2
H		Divide by 4
DIVSELb0	DIVSELb1	Q2:3 Outputs
L	L	Divide by 4
H	L	Divide by 6
L	H	Divide by 5
H	H	Divide by 5

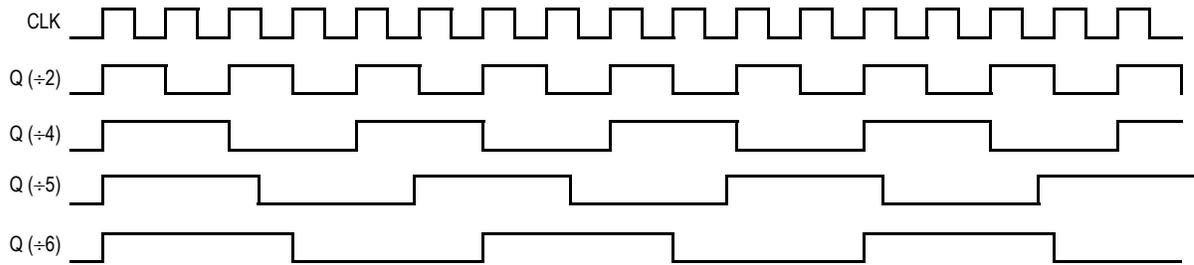


Figure 3. Timing Diagram

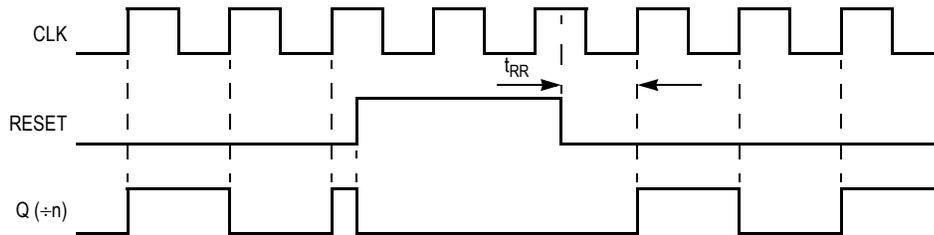


Figure 4. Timing Diagram

Table 3. Attributes

Characteristics		Value
Internal Input Pulldown Resistor		75 k Ω
Internal Input Pullup Resistor		75 k Ω
ESD Protection	Human Body Model	> 4 kV
	Machine Model	> 200 V
	Charged Device Model	> 2 kV

Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test

Table 4. Maximum Ratings⁽¹⁾

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V _{CC}	PECL Mode Power Supply	V _{EE} = 0 V		3.9	V
V _{EE}	ECL Mode Power Supply	V _{CC} = 0 V		-3.9	V
V _I	PECL Mode Input Voltage ECL Mode Input Voltage	V _{EE} = 0 V V _{CC} = 0 V	V _I ≤ V _{CC} V _I ≥ V _{EE}	3.9 -3.9	V V
I _{out}	Output Current	Continuous Surge		50 100	mA mA
I _{BB}	V _{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	20 TSSOP 20 TSSOP	74 64	°C/W °C/W

1. Maximum Ratings are those values beyond which device damage may occur.

Table 5. DC Characteristics (V_{CC} = 0 V, V_{EE} = -3.8 V to -3.135 V or V_{CC} = 3.135 V to 3.8 V, V_{EE} = 0 V)⁽¹⁾

Symbol	Characteristic	-40°C			0°C to 85°C			Unit
		Min	Typ	Max	Min	Typ	Max	
I _{EE}	Power Supply Current		35	60		35	60	mA
V _{OH}	Output HIGH Voltage ⁽²⁾	V _{CC} -1150	V _{CC} -1020	V _{CC} -800	V _{CC} -1200	V _{CC} -970	V _{CC} -750	mV
V _{OL}	Output LOW Voltage ⁽²⁾	V _{CC} -1950	V _{CC} -1620	V _{CC} -1250	V _{CC} -2000	V _{CC} -1680	V _{CC} -1300	mV
V _{IH}	Input HIGH Voltage (Single-Ended)	V _{CC} -1165		V _{CC} -880	V _{CC} -1165		V _{CC} -880	mV
V _{IL}	Input LOW Voltage (Single-Ended)	V _{CC} -1810		V _{CC} -1475	V _{CC} -1810		V _{CC} -1475	mV
V _{BB}	Output Reference Voltage	V _{CC} -1400		V _{CC} -1200	V _{CC} -1400		V _{CC} -1200	mV
V _{PP}	Differential Input Voltage ⁽³⁾	0.12		1.3	0.12		1.3	V
V _{CMR}	Differential Cross Point Voltage ⁽⁴⁾	V _{EE} +0.2		V _{CC} -1.1	V _{EE} +0.2		V _{CC} -1.1	V
I _{IH}	Input HIGH Current			150			150	μA
I _{IL}	Input LOW Current	0.5			0.5			μA

- MC100ES6139 circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfm is maintained.
- All loading with 50 Ω to V_{CC}-2.0 volts.
- V_{PP} (DC) is the minimum differential input voltage swing required to maintain device functionality.
- V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 6. AC Characteristics ($V_{CC} = 0\text{ V}$, $V_{EE} = -3.8\text{ V}$ to -3.135 V or $V_{CC} = 3.135\text{ V}$ to 3.8 V , $V_{EE} = 0\text{ V}$)⁽¹⁾

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{\max}	Maximum Frequency		> 1			> 1			> 1		GHz
t_{PLH} , t_{PHL}	Propagation Delay CLK, Q (Diff) MR, Q	550 400		850 850	550 400		850 850	550 400		850 850	ps
t_{RR}	Reset Recovery	200	100		200	100		200	100		ps
t_s	Setup Time \overline{EN} , CLK DIVSEL, CLK	200	120		200	120		200	120		ps
		400	180		400	180		400	180		ps
t_h	Hold Time CLK, \overline{EN} CLK, DIVSEL	100	50		100	50		100	50		ps
		200	140		200	140		200	140		ps
t_{PW}	Minimum Pulse Width MR	550	450		550	450		550	450		ps
t_{SKEW}	Within Device Skew Q, \overline{Q} Q, \overline{Q} @ Same Frequency Device-to-Device Skew ⁽²⁾			100			100			100	ps
				50			50			50	ps
				300			300			300	ps
t_{JITTER}	Cycle-to-Cycle Jitter (RSM 1σ)			1			1			1	ps
V_{PP}	Input Voltage Swing (Differential)	200		1200	200		1200	200		1200	mV
V_{CMR}	Differential Cross Point Voltage	$V_{EE}+0.2$		$V_{CC}-1.2$	$V_{EE}+0.2$		$V_{CC}-1.2$	$V_{EE}+0.2$		$V_{CC}-1.2$	V
t_r t_f	Output Rise/Fall Times (20% – 80%) Q, \overline{Q}	50		300	50		300	50		300	ps

1. Measured using a 750 mV source, 50% duty cycle clock source. All loading with $50\ \Omega$ to $V_{CC} - 2.0\text{ V}$.
2. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

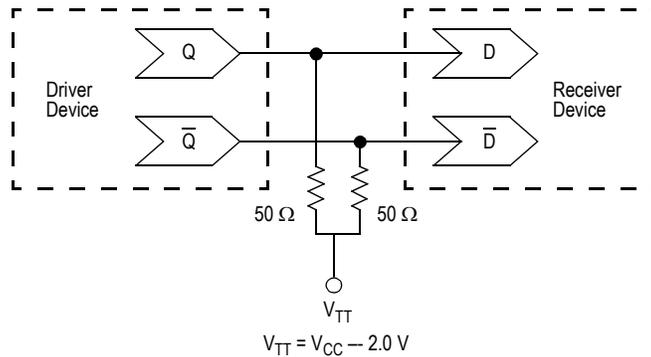
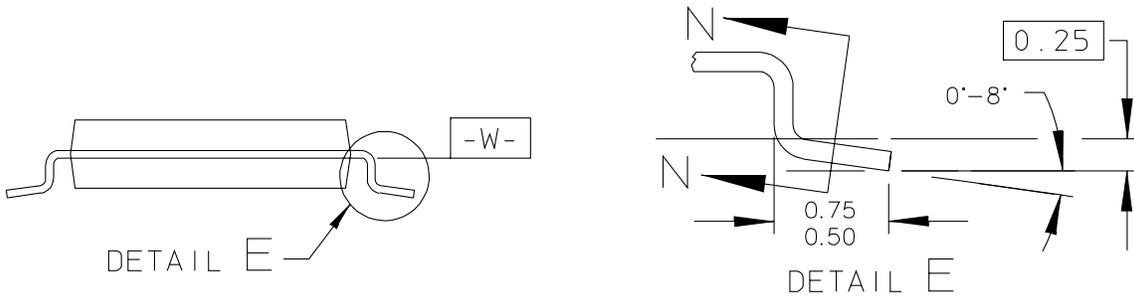
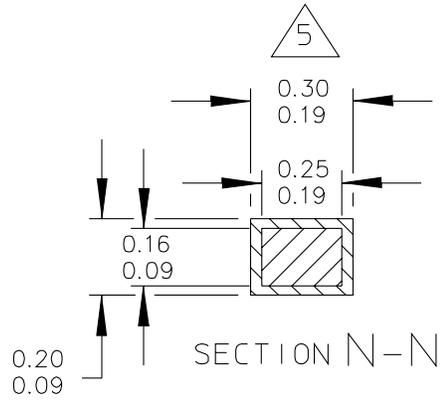


Figure 5. Typical Termination for Output Driver and Device Evaluation

PACKAGE DIMENSIONS



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	STANDARD: JEDEC	

CASE 948E-03
ISSUE B
20-LEAD TSSOP PACKAGE

PACKAGE DIMENSIONS

NOTES:

1. CONTROLLING DIMENSION: MILLIMETER
2. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M-1982.
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE.
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 PER SIDE.
5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDITION.
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