EL2001C
Low Power, 70 MHz Buffer Amplifier

Features

- 1.3 mA supply current
- 70 MHz bandwidth
- 2000 V/μs slew rate
- Low bias current, 1 μA typical
- 100 mA output current
- Short circuit protected
- Low cost
- Stable with capacitive loads
- Wide supply range $\pm$5V to $\pm$15V
- No thermal runaway

Applications

- Op amp output current booster
- Cable/line driver
- A/D input buffer
- Low standby current systems

Ordering Information

Part No.	Temp. Range	Pkg.	Outline#
EL2001ACN	0°C to +75°C	P-DIP	MDP0031
EL2001CM	0°C to +75°C	20-Lead SOL	MDP0027
EL2001CN	0°C to +75°C	P-DIP	MDP0031

General Description

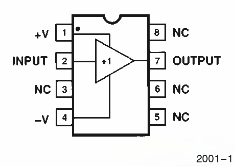
The EL2001 is a low cost monolithic, high slew rate, buffer amplifier. Built using the Elantec monolithic Complementary Bipolar process, this patented buffer has a −3 dB bandwidth of 70 MHz, and delivers 100 mA, yet draws only 1.3 mA of supply current. It typically operates from $\pm$15V power supplies but will work with as little as $\pm$5V.

This high speed buffer may be used in a wide variety of applications in military, video and medical systems. A typical example is a general purpose op amp output current booster where the buffer must have sufficiently high bandwidth and low phase shift at the maximum frequency of the op amp.

Elantec's products and facilities comply with MIL-I-45208A, and other applicable quality specifications. For information on Elantec's processing, see the Elantec document, QRA-1: *Elantec's Processing, Monolithic Integrated Circuits*.

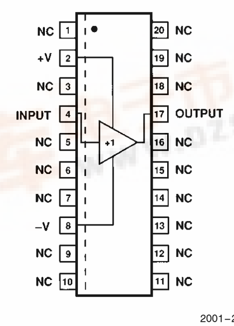
Connection Diagrams

EL2001 DIP Pinout



Top View

EL2001 SOL Pinout



Top View

Note: Non-designated pins are no connects and are not electrically connected internally.

Manufactured under U.S. Patent No. 4,833,424, 4,827,223 U.K. Patent No. 2217134

Absolute Maximum Ratings

V_S	Supply Voltage (V+ − V−)	±18V or 36V	T_A	Operating Temperature Range	
V_{IN}	Input Voltage (Note 1)	±15V or V_S		EL2001AC/EL2001C	0°C to +75°C
I_{IN}	Input Current (Note 1)	±50 mA	T_J	Operating Junction Temperature	150°C
P_D	Power Dissipation (Note 2)	See Curves	T_{ST}	Storage Temperature	−65°C to +150°C
	Output Short Circuit Duration (Note 3)	Continuous			

Important Note:
All parameters having Min/Max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality inspection. Elantec performs most electrical tests using modern high-speed automatic test equipment, specifically the LTX77 Series system. Unless otherwise noted, all tests are pulsed tests, therefore $T_J = T_C = T_A$.

Test Level	Test Procedure
I	100% production tested and QA sample tested per QA test plan QCX0002.
II	100% production tested at T_A = 25°C and QA sample tested at T_A = 25°C, T_{MAX} and T_{MIN} per QA test plan QCX0002.
III	QA sample tested per QA test plan QCX0002.
IV	Parameter is guaranteed (but not tested) by Design and Characterization Data.
V	Parameter is typical value at T_A = 25°C for information purposes only.

Electrical Characteristics V_S = ±15V, R_S = 50Ω, unless otherwise specified

Parameter	Description	Test Conditions			Limits			EL2001AC EL2001C	Units
		V_{IN}	Load	Temp	Min	Typ	Max	Test Level	
V_{OS}	Offset Voltage EL2001A/EL2001AC	0	∞	25°C	−10	2	I	I	mV
				T_{MIN}, T_{MAX}	−15		+15	III	mV
	EL2001/EL2001C	0	∞	25°C	−30	2	+30	I	mV
				T_{MIN}, T_{MAX}	−40		+40	III	mV
I_{IN}	Input Current EL2001A/EL2001AC	0	∞	25°C	−3	1	+3	I	μA
				T_{MIN}, T_{MAX}	−6		+6	III	μA
	EL2001/EL2001C	0	∞	25°C	−5	1	+5	I	μA
				T_{MIN}, T_{MAX}	−10		+10	III	μA
R_{IN}	Input Resistance	±12V	100Ω	25°	1	8		I	MΩ
				T_{MIN}, T_{MAX}	0.5			III	MΩ

TD is 2.5in

Electrical Characteristics $V_S = \pm 15V$, $R_S = 50\Omega$, unless otherwise specified — Contd.

Parameter	Description	Test Conditions			Limits			EL2001AC EL2001C	Units
		V_{in}	Load	Temp	Min	Typ	Max	Test Level	
A_{V1}	Voltage Gain	±12V	∞	25°C	0.990	0.998		I	V/V
				T_{MIN}, T_{MAX}	0.985			III	V/V
A_{V2}	Voltage Gain	±10V	100Ω	25°C	0.83	0.93		I	V/V
				T_{MIN}, T_{MAX}	0.80			III	V/V
A_{V3}	Voltage Gain with $V_S = \pm 5V$	±3V	100Ω	25°C	0.82	0.89		I	V/V
				T_{MIN}, T_{MAX}	0.79			III	V/V
V_O	Output Voltage Swing	±12V	100Ω	25°C	±10	±11		I	V
				T_{MIN}, T_{MAX}	±9.5			III	V
R_{OUT}	Output Resistance	±2V	100Ω	25°C		10	15	I	Ω
				T_{MIN}, T_{MAX}			18	III	Ω
I_{OUT}	Output Current	±12V	(Note 4)	25°C	±100	±160		I	mA
				T_{MIN}, T_{MAX}	±95			III	mA
I_S	Supply Current	0	∞	25°C		1.3	2.0	I	mA
				T_{MIN}, T_{MAX}			2.5	III	mA
PSRR	Supply Rejection, (Note 5)	0	∞	25°C	60	75		I	dB
				T_{MIN}, T_{MAX}	50			III	dB
t_r	Rise Time	0.5V	100Ω	25°C		4.2		V	ns
t_d	Propagation Delay	0.5V	100Ω	25°C		2.0		V	ns
SR	Slew Rate, (Note 6)	±10V	100Ω	25°C	1200	2000		IV	V/μs

Note 1: If the input exceeds the ratings shown (or the supplies) or if the input to output voltage exceeds ±7.5V then the input current must be limited to ±50 mA. See the applications section for more information.

Note 2: The maximum power dissipation depends on package type, ambient temperature and heat sinking. See the characteristic curves for more details.

Note 3: A heat sink is required to keep the junction temperature below the absolute maximum when the output is short circuited.

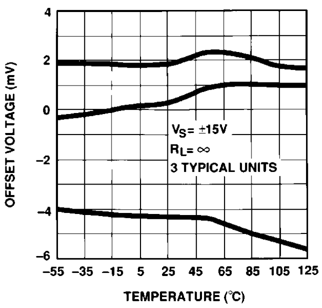
Note 4: Force the input to +12V and the output to +10V and measure the output current. Repeat with −12 V_{IN} and −10V on the output.

Note 5: V_{OS} is measured at $V_S+ = +4.5V$, $V_S- = -4.5V$ and at $V_S+ = +18V$, $V_S- = -18V$. Both supplies are changed simultaneously.

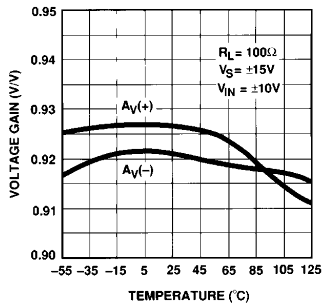
Note 6: Slew rate is measured between $V_{OUT} = +5V$ and $-5V$.

Typical Performance Curves

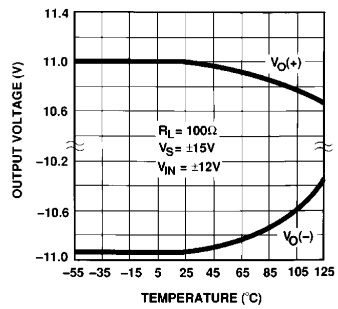
Offset Voltage vs Temperature



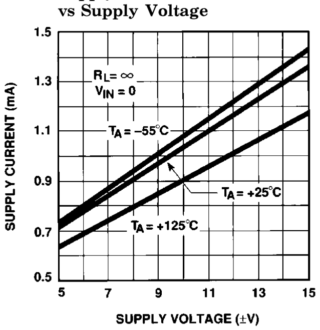
Voltage Gain vs Temperature



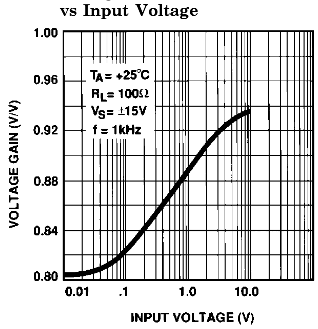
Output Voltage Swing vs Temperature



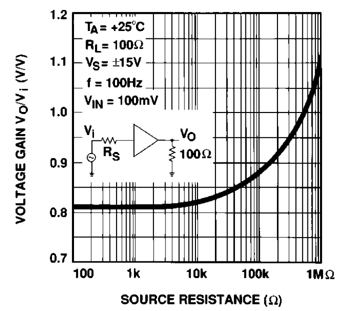
Supply Current vs Supply Voltage



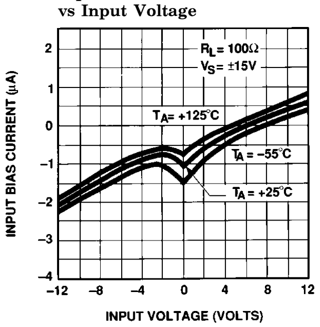
Voltage Gain vs Input Voltage



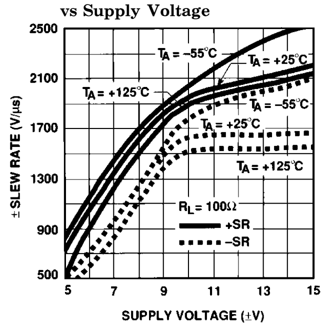
Voltage Gain vs Source Resistance



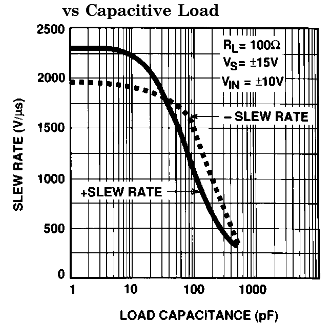
Input Bias Current vs Input Voltage



±Slew Rate vs Supply Voltage



±Slew Rate vs Capacitive Load



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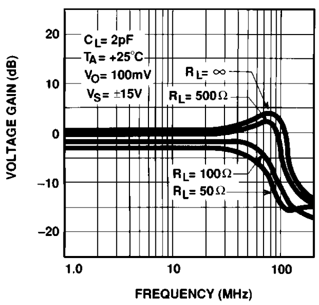
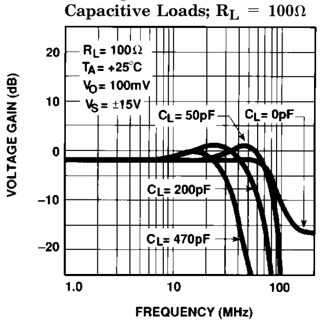
Typical Performance Curves — Contd.

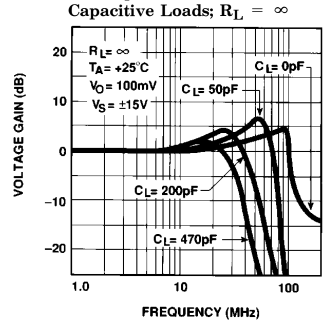
Voltage Gain vs Frequency for Various Resistive Loads



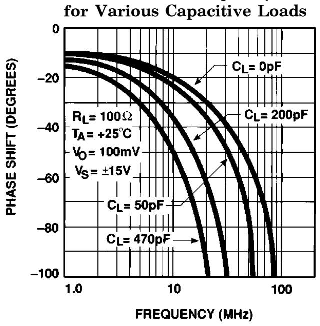
Voltage Gain vs Frequency for Various Capacitive Loads; R_L = 100Ω



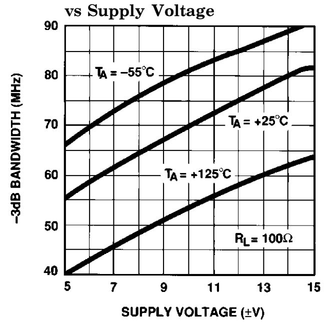
Voltage Gain vs Frequency for Various Capacitive Loads; R_L = ∞



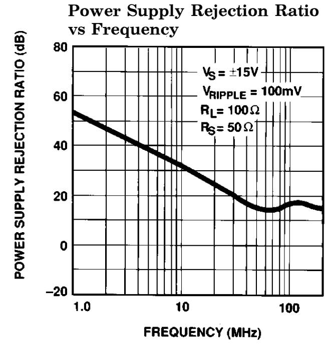
Phase Shift vs Frequency for Various Capacitive Loads



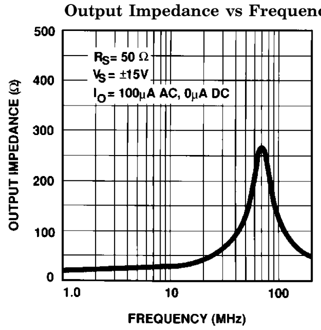
−3 dB Bandwidth vs Supply Voltage



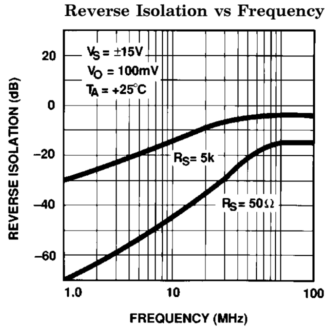
Power Supply Rejection Ratio vs Frequency



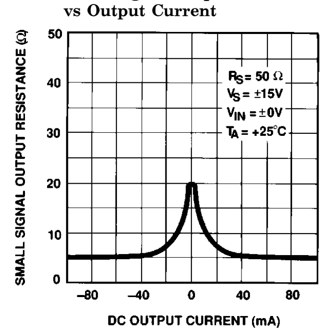
Output Impedance vs Frequency



Reverse Isolation vs Frequency



Small Signal Output Resistance vs Output Current



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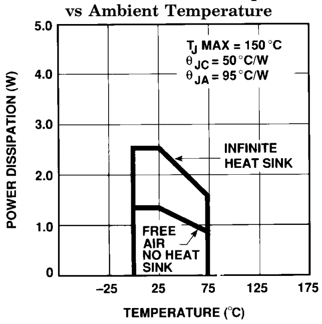
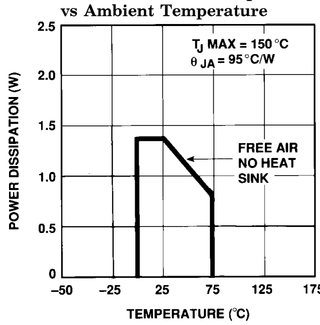
Typical Performance Curves — Contd.

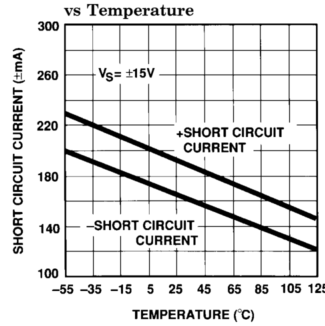
8-Lead Plastic DIP Maximum Power Dissipation vs Ambient Temperature



20-Lead SOL Maximum Power Dissipation vs Ambient Temperature



Short Circuit Current vs Temperature



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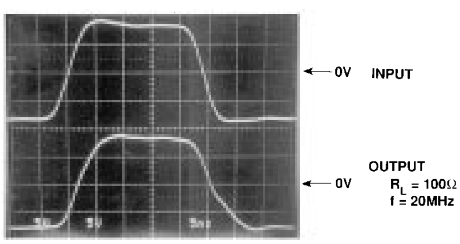
Large Signal Response



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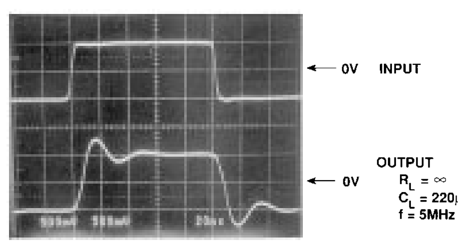
Small Signal Response



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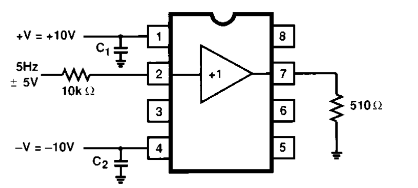
Burn-In Circuit



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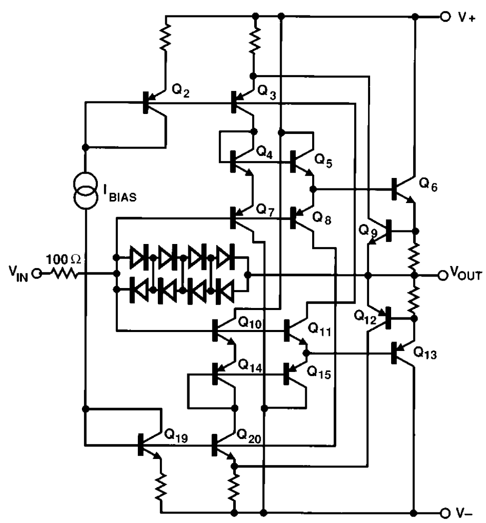
Simplified Schematic



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Application Information

The EL2001 is a monolithic buffer amplifier built on Elantec's proprietary dielectric isolation process that produces NPN and PNP transistors with essentially identical DC and AC characteristics. The EL2001 takes full advantage of the complementary process with a unique circuit topology.

Elantec has applied for two patents based on the EL2001's topology. The patents relate to the base drive and feedback mechanism in the buffer. This feedback makes 2000 V/μs slew rates with 100Ω loads possible with very low supply current.

Power Supplies

The EL2001 may be operated with single or split supplies with total voltage difference between 10V (±5V) and 36V (±18V). It is not necessary to use equal split value supplies. For example −5V and +12V would be excellent for signals from −2V to +9V.

Bypass capacitors from each supply pin to ground are highly recommended to reduce supply ringing and the interference it can cause. At a minimum, 1 μF tantalum capacitor with short leads should be used for both supplies.

Input Characteristics

The input to the EL2001 looks like a resistance in parallel with about 3.5 picofarads in addition to a DC bias current. The DC bias current is due to the miss-match in beta and collector current between the NPN and PNP transistors connected to the input pin. The bias current can be either positive or negative. The change in input current with input voltage (R_{IN}) is affected by the output load, beta and the internal boost. R_{IN} can actually appear negative over portions of the input range; typical input current curves are shown in the characteristic curves. Internal clamp diodes from the input to the output are provided. These diodes protect the transistor base emitter junctions and limit the boost current during slew to avoid saturation of internal transistors. The diodes begin conduction at about ±2.5V input to output differential. When that happens the input resistance drops dramatically. The diodes are rated at 50 mA. When conducting they have a series resistance of about 20Ω. There is also 100Ω in series with the input that limits input current. Above ±7.5V differential input to output, additional series resistance should be added.

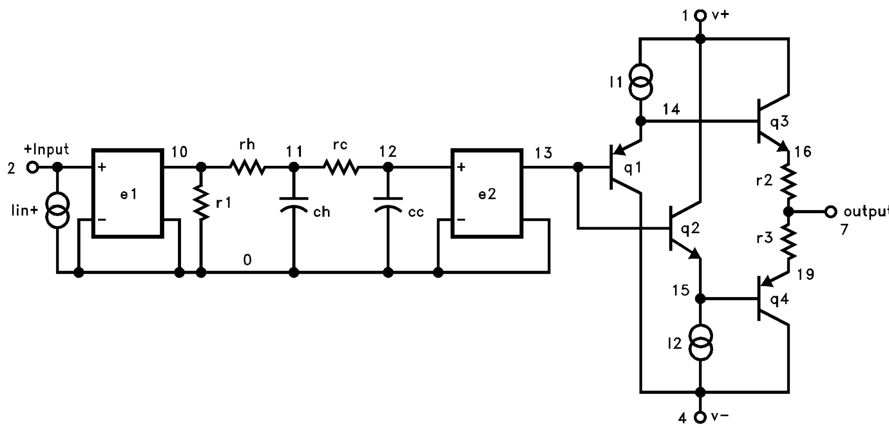
Source Impedance

The EL2001 has good input to output isolation. When the buffer is not used in a feedback loop, capactive and resistive sources up to 1 Meg present no oscillation problems. Care must be used in board layout to minimize output to input coupling. CAUTION: When using high source impedances (R_S > 100 kΩ), significant gain errors can be observed due to output offset, load resistor, and the action of the boost circuit. See typical performance curves.

EL2001C Macromodel

```
*Connections:   +input
*                |      +Vsupply
*                |      |      -Vsupply
*                |      |      |      output
*                |      |      |      |
.subckt M2001    2      1      4      7
* Input Stage
el 10 0 2 0 1.0
r1 10 0 1K
rh 10 11 150
ch 11 0 9pF
rc 11 12 100
cc 12 0 4pF
e2 13 0 12 0 1.0
* Output stage
q1 4 13 14 qp
q2 1 13 15 qn
q3 1 14 16 qn
q4 4 15 19 qp
r2 16 7 1
r3 19 7 1
i1 1 14 0.9mA
i2 15 4 0.9mA
* Bias Current
iin+ 2 0 1uA
* Models
.model qn npn(is=5e-15 bf=150 rb=200 ptf=45 tf=0.1nS)
.model qp pnp(is=5e-15 bf=150 rb=200 ptf=45 tf=0.1nS)
.ends
```

EL2001C Macromodel — Contd.



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EL2001C
Low Power, 70 MHz Buffer Amplifier

General Disclaimer

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élantec
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December 1995 Rev G

Printed in U.S.A.