MSP430x21x1
MIXED SIGNAL MICROCONTROLLER

SLAS439 − SEPTEMBER 2004

- **Low Supply Voltage Range 1.8 V to 3.6 V**
- **Ultralow-Power Consumption**
  - **Active Mode: 200 µA at 1 MHz, 2.2 V**
  - **Standby Mode: 0.7 µA**
  - **Off Mode (RAM Retention): 0.1 µA**
- **Ultrafast Wake-Up From Standby Mode in less than 1 µs**
- **16-Bit RISC Architecture, 65 ns Instruction Cycle Time**
- **Basic Clock Module Configurations:**
  - **Internal Frequencies up to 16MHz**
  - **32-kHz Crystal**
  - **High-Frequency Crystal up to 16MHz**
  - **Resonator**
  - **External Clock Source**
- **16-Bit Timer_A With Three Capture/Compare Registers**
- **On-Chip Comparator for Analog Signal Compare Function or Slope A/D Conversion**
- **Serial Onboard Programming, No External Programming Voltage Needed Programmable Code Protection by Security Fuse**
- **Bootstrap Loader in Flash Devices**
- **Family Members Include:**
  MSP430F2101: 1KB + 256B Flash Memory, 128B RAM
  MSP430F2111: 2KB + 256B Flash Memory, 128B RAM
  MSP430F2121: 4KB + 256B Flash Memory, 256B RAM
  MSP430F2131: 8KB + 256B Flash Memory, 256B RAM
- **Available in a 20-Pin Plastic Small-Outline Wide Body (SOWB) Package, 20-Pin Plastic Small-Outline Thin (TSSOP) Package, 20-Pin TVSOP and 24-Pin QFN**
- **For Complete Module Descriptions, Refer to the *MSP430x2xx Family User's Guide***

PRODUCT PREVIEW

description

The Texas Instruments MSP430 family of ultralow power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that attribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1µs.

The MSP430x21x1 series is an ultralow-power mixed signal microcontroller with a built-in 16-bit timer, versatile analog comparator and sixteen I/O pins.

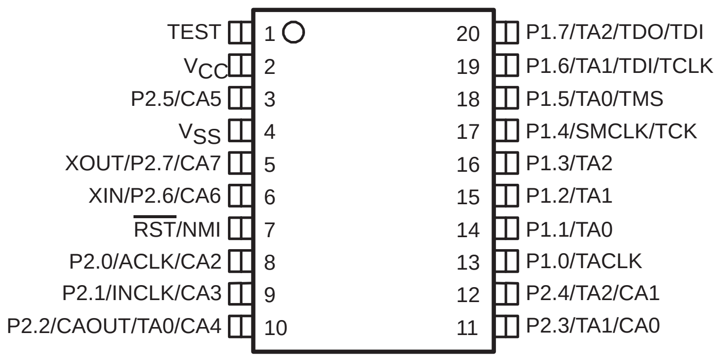
Typical applications include sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system. Stand alone RF sensor front end is another area of application. The analog comparator provides slope A/D conversion capability.

AVAILABLE OPTIONS

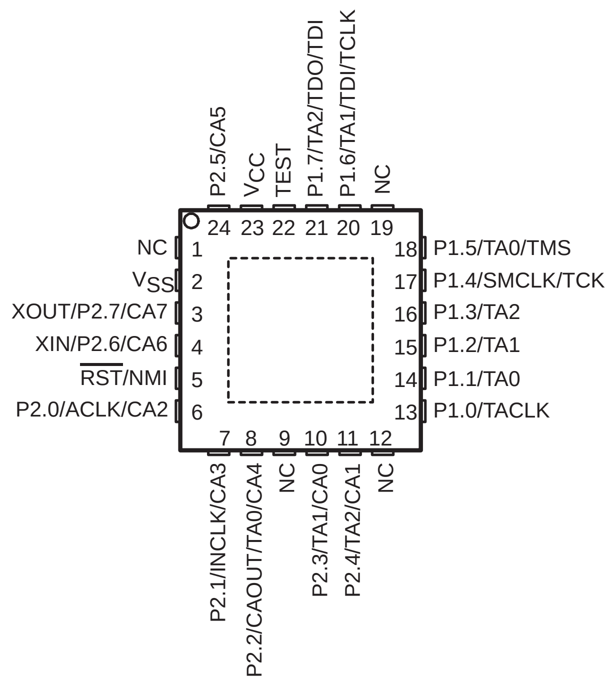
T_A	PACKAGED DEVICES			
	PLASTIC 20-PIN SOWB (DW)	PLASTIC 20-PIN TSSOP (PW)	PLASTIC 20-PIN TVSOP (DGV)	PLASTIC 24-PIN QFN (RGE)
−40°C to 85°C	MSP430F2101IDW MSP430F2111IDW MSP430F2121IDW MSP430F2131IDW	MSP430F2101IPW MSP430F2111IPW MSP430F2121IPW MSP430F2131IPW	MSP430F2101IDGV MSP430F2111IDGV MSP430F2121IDGV MSP430F2131IDGV	MSP430F2101IRGE MSP430F2111IRGE MSP430F2121IRGE MSP430F2131IRGE

device pinout

DW, PW, or DGV PACKAGE
(TOP VIEW)

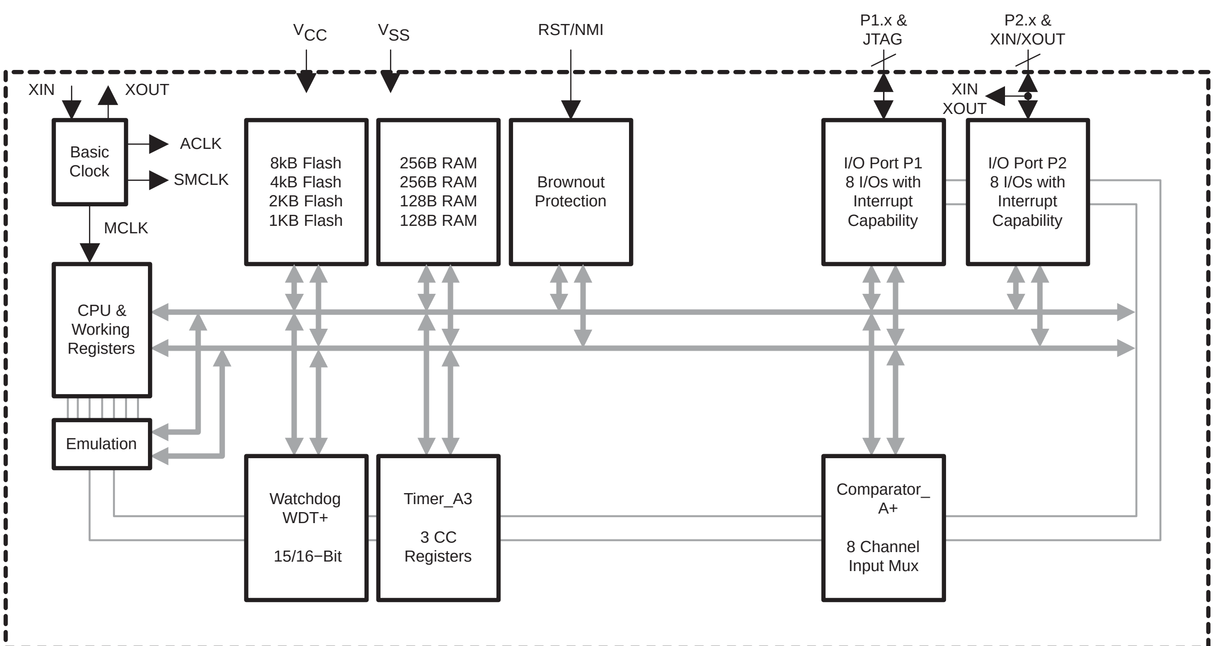


RGE PACKAGE
(TOP VIEW)



Note: NC pins not internally connected
Power Pad connection to V_{SS} recommended

functional block diagram



Note: See port schematics section for detailed I/O information

Terminal Functions

TERMINAL				DESCRIPTION
NAME	DW, PW, or DGV NO.	RGE NO.	I/O	
P1.0/TACLK	13	13	I/O	General-purpose digital I/O pin/Timer_A, clock signal TACLK input
P1.1/TA0	14	14	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0A input, compare: Out0 output/BSL transmit
P1.2/TA1	15	15	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	16	16	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK/TCK	17	17	I/O	General-purpose digital I/O pin/SMCLK signal output/test clock, input terminal for device programming and test
P1.5/TA0/TMS	18	18	I/O	General-purpose digital I/O pin/Timer_A, compare: Out0 output/test mode select, input terminal for device programming and test
P1.6/TA1/TDI/TCLK	19	20	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/test data input or test clock input during programming and test
P1.7/TA2/TDO/TDI†	20	21	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/test data output terminal or test data input during programming and test
P2.0/ACLK/CA2	8	6	I/O	General-purpose digital I/O pin/ACLK output/comparator_A+, CA2 input
P2.1/INCLK/CA3	9	7	I/O	General-purpose digital I/O pin/Timer_A, clock signal at INCLK/comparator_A+, CA3 input
P2.2/CAOUT/ TA0/CA4	10	8	I/O	General-purpose digital I/O pin/Timer_A, capture: CCI0B input/ comparator_A+, output/comparator_A+, CA4 input/BSL receive
P2.3/CA0/TA1	11	10	I/O	General-purpose digital I/O pin/Timer_A, compare: Out1 output/ comparator_A+, CA0 input
P2.4/CA1/TA2	12	11	I/O	General-purpose digital I/O pin/Timer_A, compare: Out2 output/ comparator_A+, CA1 input
P2.5/CA5	3	24	I/O	General-purpose digital I/O pin/ comparator_A+, CA5 input
XIN/P2.6/CA6	6	4	I/O	Input terminal of crystal oscillator/general-purpose digital I/O pin/ comparator_A+, CA6 input
XOUT/P2.7/CA7	5	3	I/O	Output terminal of crystal oscillator/general-purpose digital I/O pin/ comparator_A+, CA7 input
$\overline{RST}$/NMI	7	5	I	Reset or nonmaskable interrupt input
TEST	1	22	I	Selects test mode for JTAG pins on Port1. The device protection fuse is connected to TEST.
V_{CC}	2	23		Supply voltage
V_{SS}	4	2		Ground reference
QFN Pad	NA	Package Pad	NA	QFN package pad connection to V_{SS} recommended.

† TDO or TDI is selected via JTAG instruction.

NOTE: If XOUT/P2.7/CA7 is used as an input, excess current will flow until P2SEL.7 is cleared. This is due to the oscillator output driver connection to this pad after reset.

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short-form description

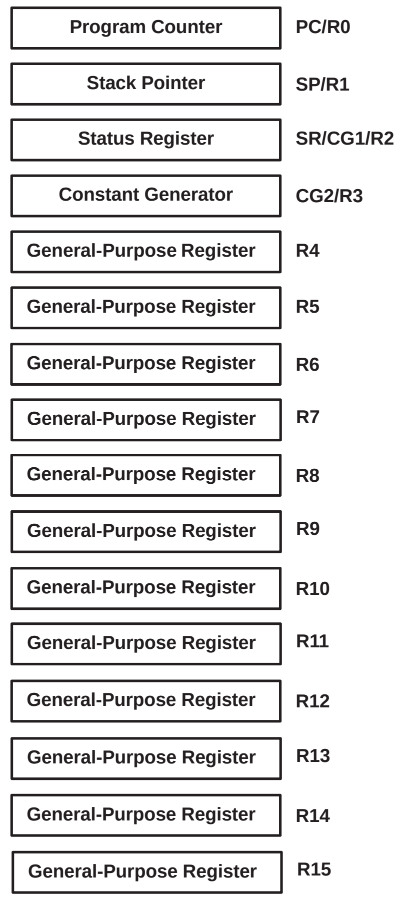
CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.



instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 1 shows examples of the three types of instruction formats; the address modes are listed in Table 2.

Table 1. Instruction Word Formats

Dual operands, source-destination	e.g. ADD R4,R5	R4 + R5 −−−> R5
Single operands, destination only	e.g. CALL R8	PC −−>(TOS), R8−−> PC
Relative jump, un/conditional	e.g. JNE	Jump-on-equal bit = 0

Table 2. Address Mode Descriptions

ADDRESS MODE	S	D	SYNTAX	EXAMPLE	OPERATION
Register	●	●	MOV Rs,Rd	MOV R10,R11	R10 −−> R11
Indexed	●	●	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5)−−> M(6+R6)
Symbolic (PC relative)	●	●	MOV EDE,TONI		M(EDE) −−> M(TONI)
Absolute	●	●	MOV &MEM,&TCDAT		M(MEM) −−> M(TCDAT)
Indirect	●		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) −−> M(Tab+R6)
Indirect autoincrement	●		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) −−> R11 R10 + 2−−> R10
Immediate	●		MOV #X,TONI	MOV #45,TONI	#45 −−> M(TONI)

NOTE: S = source D = destination

operating modes

The MSP430 has one active mode and five software selectable low-power modes of operation. An interrupt event can wake up the device from any of the five low-power modes, service the request and restore back to the low-power mode on return from the interrupt program.

The following six operating modes can be configured by software:

- Active mode AM;
  - All clocks are active
- Low-power mode 0 (LPM0);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
- Low-power mode 1 (LPM1);
  - CPU is disabled
    ACLK and SMCLK remain active. MCLK is disabled
    DCO's dc-generator is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2);
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator remains enabled
    ACLK remains active
- Low-power mode 3 (LPM3);
  - CPU is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator is disabled
    ACLK remains active
- Low-power mode 4 (LPM4);
  - CPU is disabled
    ACLK is disabled
    MCLK and SMCLK are disabled
    DCO's dc-generator is disabled
    Crystal oscillator is stopped

interrupt vector addresses

The interrupt vectors and the power-up starting address are located in the address range of 0FFFFh−0FFE0h. The vector contains the 16-bit address of the appropriate interrupt handler instruction sequence.

If the reset vector (located at address 0FFFEh) contains 0FFFFh (e.g. flash is not programmed) the CPU will go into LPM4 immediately.

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power-up External reset Watchdog Flash key violation PC out-of-range (see Note 1)	PORIFG RSTIFG WDTIFG KEYV (see Note 2)	Reset	0FFFEh	15, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG (see Notes 2 & 4)	(non)-maskable, (non)-maskable, (non)-maskable	0FFFCh	14
			0FFFAh	13
			0FFF8h	12
Comparator_A+	CAIFG	maskable	0FFF6h	11
Watchdog Timer	WDTIFG	maskable	0FFF4h	10
Timer_A3	TACCR0 CCIFG (see Note 3)	maskable	0FFF2h	9
Timer_A3	TACCR1 CCIFG. TACCR2 CCIFG TAIFG (see Notes 2 & 3)	maskable	0FFF0h	8
			0FFEEh	7
			0FFECh	6
			0FFEAh	5
			0FFE8h	4
I/O Port P2 (eight flags)	P2IFG.0 to P2IFG.7 (see Notes 2 & 3)	maskable	0FFE6h	3
I/O Port P1 (eight flags)	P1IFG.0 to P1IFG.7 (see Notes 2 & 3)	maskable	0FFE4h	2
			0FFE2h	1
			0FFE0h	0, lowest

NOTES: 1. A reset is generated if the CPU tries to fetch instructions from within the module register memory address range (0h−01FFh).
2. Multiple source flags
3. Interrupt flags are located in the module
4. (non)-maskable: the individual interrupt-enable bit can disable an interrupt event, but the general interrupt enable cannot. Nonmaskable: neither the individual nor the general interrupt-enable bit will disable an interrupt event.

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special function registers

Most interrupt and module enable bits are collected into the lowest address space. Special function register bits not allocated to a functional purpose are not physically present in the device. Simple software access is provided with this arrangement.

interrupt enable 1 and 2

Address	7	6	5	4	3	2	1	0
0h			ACCVIE	NMIIE			OFIE	WDTIE
			rw-0	rw-0			rw-0	rw-0

WDTIE: Watchdog Timer interrupt enable. Inactive if watchdog mode is selected. Active if Watchdog Timer is configured in interval timer mode.
OFIE: Oscillator fault enable
NMIIE: (Non)maskable interrupt enable
ACCVIE: Flash access violation interrupt enable

Address	7	6	5	4	3	2	1	0
01h								

interrupt flag register 1 and 2

Address	7	6	5	4	3	2	1	0
02h				NMIIFG	RSTIFG	PORIFG	OFIFG	WDTIFG
				rw-0	rw-(0)	rw-(1)	rw-1	rw-(0)

WDTIFG: Set on Watchdog Timer overflow (in watchdog mode) or security key violation.
Reset on V_{CC} power-up or a reset condition at $\overline{RST}$/NMI pin in reset mode.
OFIFG: Flag set on oscillator fault
RSTIFG: External reset interrupt flag. Set on a reset condition at $\overline{RST}$/NMI pin in reset mode. Reset on V_{CC} power−up
PORIFG: Power−On interrupt flag. Set on V_{CC} power−up.
NMIIFG: Set via $\overline{RST}$/NMI-pin

Address	7	6	5	4	3	2	1	0
03h								

Legend

rw:	Bit can be read and written.
rw-0,1:	Bit can be read and written. It is Reset or Set by PUC.
rw-(0,1):	Bit can be read and written. It is Reset or Set by POR.
(shaded box)	SFR bit is not present in device

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memory organization

		MSP430F2101	MSP430F2111	MSP430F2121	MSP430F2131
Memory Main: interrupt vector Main: code memory	Size Flash Flash	1KB Flash 0FFFFh−0FFE0h 0FFFFh−0FC00h	2KB Flash 0FFFFh−0FFE0h 0FFFFh−0F800h	4KB Flash 0FFFFh−0FFE0h 0FFFFh−0F000h	8KB Flash 0FFFFh−0FFE0h 0FFFFh−0E000h
Information memory	Size Flash	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h	256 Byte 010FFh − 01000h
Boot memory	Size ROM	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h	1KB 0FFFh − 0C00h
RAM	Size	128 Byte 027Fh − 0200h	128 Byte 027Fh − 0200h	256 Byte 02FFh − 0200h	256 Byte 02FFh − 0200h
Peripherals	16-bit 8-bit 8-bit SFR	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h	01FFh − 0100h 0FFh − 010h 0Fh − 00h

bootstrap loader (BSL)

The MSP430 bootstrap loader (BSL) enables users to program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory via the BSL is protected by user-defined password. For complete description of the features of the BSL and its implementation, see the Application report *Features of the MSP430 Bootstrap Loader*, Literature Number SLAA089.

BSL Function	DW, PW & DGV Package Pins	RGE Package Pins
Data Transmit	14 - P1.1	14 - P1.1
Data Receive	10 - P2.2	8 - P2.2

flash memory

The flash memory can be programmed via the JTAG port, the bootstrap loader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 64 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0−n.
  Segments A to D are also called *information memory.*
- Segment A contains calibration data. After reset segment A is protected against programming or erasing. It can be unlocked but care should be taken not to erase this segment if the calibration data is required.

peripherals

Peripherals are connected to the CPU through data, address, and control busses and can be handled using all instructions. For complete module descriptions, refer to the *MSP430x2xx Family User's Guide.*

oscillator and system clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally-controlled oscillator (DCO) and a high frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low-power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 1 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high frequency crystal.
- Main clock (MCLK), the system clock used by the CPU.
- Sub-Main clock (SMCLK), the sub-system clock used by the peripheral modules.

DCO Calibration Data (provided from factory in flash info memory segment A)			
DCO Frequency	**Calibration Register**	**Size**	**Address**
1 MHz	CALBC1_1MHz	byte	010FFh
	CALDCO_1MHz	byte	010FEh
8 MHz	CALBC1_8MHz	byte	010FDh
	CALDCO_8MHz	byte	010FCh
12 MHz	CALBC1_12MHz	byte	010FBh
	CALDCO_12MHz	byte	010FAh
16 MHz	CALBC1_16MHz	byte	010F9h
	CALDCO_16MHz	byte	010F8h

brownout

The brownout circuit is implemented to provide the proper internal reset signal to the device during power on and power off.

digital I/O

There are two 8-bit I/O ports implemented—ports P1 and P2:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of port P1 and P2.
- Read/write access to port-control registers is supported by all instructions.
- Each I/O has an individually programmable pull−up/pull−down resistor.

WDT+ watchdog timer

The primary function of the watchdog timer (WDT+) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

comparator_A+

The primary function of the comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing. Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Timer_A3 Signal Connections

Input Pin Number		Device Input Signal	Module Input Name	Module Block	Module Output Signal	Output Pin Number	
DW, PW, DGV	RGE					DW, PW DGV	RGE
13 - P1.0	13 - P1.0	TACLK	TACLK	Timer	NA		
		ACLK	ACLK				
		SMCLK	SMCLK				
9 - P2.1	7 - P2.1	INCLK	INCLK				
14 - P1.1	14 - P1.1	TA0	CCI0A	CCR0	TA0	14 - P1.1	14 - P1.1
10 - P2.2	8 - P2.2	TA0	CCI0B			18 - P1.5	18 - P1.5
		V_{SS}	GND				
		V_{CC}	V_{CC}				
15 - P1.2	15 - P1.2	TA1	CCI1A	CCR1	TA1	11 - P2.3	10 - P2.3
		CAOUT (internal)	CCI1B			15 - P1.2	15 - P1.2
		V_{SS}	GND			19 - P1.6	20 - P1.6
		V_{CC}	V_{CC}				
16 - P1.3	16 - P1.3	TA2	CCI2A	CCR2	TA2	12 - P2.4	11 - P2.4
		ACLK (internal)	CCI2B			16 - P1.3	16 - P1.3
		V_{SS}	GND			20 - P1.7	21 - P1.7
		V_{CC}	V_{CC}				

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peripheral file map

PERIPHERALS WITH WORD ACCESS			
Timer_A	Reserved Reserved Reserved Reserved Capture/compare register Capture/compare register Capture/compare register Timer_A register Reserved Reserved Reserved Reserved Capture/compare control Capture/compare control Capture/compare control Timer_A control Timer_A interrupt vector	 TACCR2 TACCR1 TACCR0 TAR TACCTL2 TACCTL1 TACCTL0 TACTL TAIV	017Eh 017Ch 017Ah 0178h 0176h 0174h 0172h 0170h 016Eh 016Ch 016Ah 0168h 0166h 0164h 0162h 0160h 012Eh
Flash Memory	Flash control 3 Flash control 2 Flash control 1	FCTL3 FCTL2 FCTL1	012Ch 012Ah 0128h
Watchdog	Watchdog/timer control	WDTCTL	0120h
PERIPHERALS WITH BYTE ACCESS			
Comparator_A	Comparator_A port disable Comparator_A control 2 Comparator_A control 1	CAPD CACTL2 CACTL1	05Bh 05Ah 059h
Basic Clock	Basic clock system control 3 Basic clock system control 2 Basic clock system control 1 DCO clock frequency control	BCSCTL3 BCSCTL2 BCSCTL1 DCOCTL	053h 058h 057h 056h
Port P2	Port P2 resistor enable Port P2 selection Port P2 interrupt enable Port P2 interrupt edge select Port P2 interrupt flag Port P2 direction Port P2 output Port P2 input	P2REN P2SEL P2IE P2IES P2IFG P2DIR P2OUT P2IN	02Fh 02Eh 02Dh 02Ch 02Bh 02Ah 029h 028h
Port P1	Port P1 resistor enable Port P1 selection Port P1 interrupt enable Port P1 interrupt edge select Port P1 interrupt flag Port P1 direction Port P1 output Port P1 input	P1REN P1SEL P1IE P1IES P1IFG P1DIR P1OUT P1IN	027h 026h 025h 024h 023h 022h 021h 020h
Special Function	SFR interrupt flag 2 SFR interrupt flag 1 SFR interrupt enable 2 SFR interrupt enable 1	IFG2 IFG1 IE2 IE1	003h 002h 001h 000h

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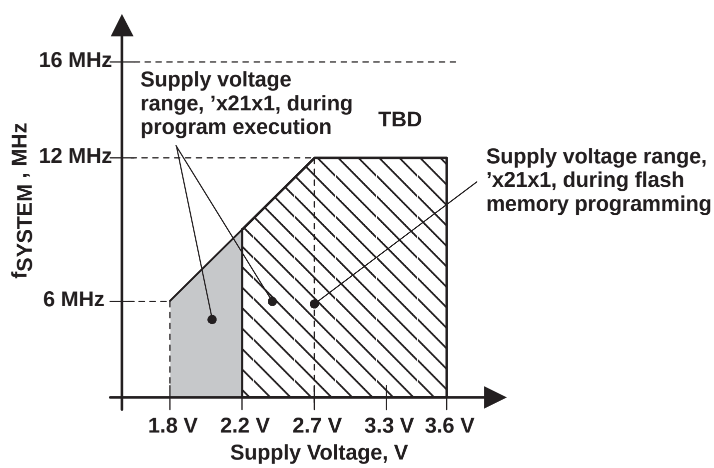
absolute maximum ratings†

Voltage applied at V_{CC} to V_{SS} . . . . −0.3 V to 4.1 V
Voltage applied to any pin (see Note 2) . . . . −0.3 V to V_{CC}+0.3 V
Diode current at any device terminal . . . . ±2 mA
Storage temperature, T_{stg} (unprogrammed device, see Note 3) . . . . −55°C to 150°C
Storage temperature, T_{stg} (programmed device, see Note 3) . . . . −40°C to 85°C

NOTES: 1. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltages referenced to V_{SS}. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TEST pin when blowing the JTAG fuse.
3. Higher temperature may be applied during board soldering process according to the current JEDEC J−STD−020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

recommended operating conditions

		MIN	NOM	MAX	UNITS
Supply voltage during program execution, V_{CC}	MSP430F21x1	1.8		3.6	V
Supply voltage during program/erase flash memory, V_{CC}	MSP430F21x1	2.2		3.6	V
Supply voltage, V_{SS}			0		V
Operating free-air temperature range, T_A	MSP430F21x1	−40		85	°C
Processor frequency f_{SYSTEM} (Maximum MCLK frequency)	V_{CC} = 1.8 V, Duty Cycle = 50% ±10%	dc		6	MHz
	V_{CC} = 2.2 V, Duty Cycle = 50% ±10%	dc		8	
	V_{CC} = 2.7 V, Duty Cycle = 50% ±10%	dc		12	
	V_{CC} = 3.0 V, Duty Cycle = 50% ±10%	dc		TBD, >12MHz	
	V_{CC} = 3.3 V, Duty Cycle = 50% ±10%	dc		TBD, >12MHz	
	V_{CC} = 3.6 V, Duty Cycle = 50% ±10%	dc		TBD, >12MHz	



NOTE: Minimum processor frequency is defined by system clock. Flash program or erase operations require a minimum V_{CC} of 2.2 V.

Figure 1. Frequency vs Supply Voltage, MSP430x21x1

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

supply current (into V_{CC}) excluding external current (see Notes 1 and 2)

PARAMETER		TEST CONDITIONS		VCC	MIN	TYP	MAX	UNIT
I_{ACTIVE}	Active mode current	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 1MHz, f_{ACLK} = 32,768Hz, Program executes in flash CPUOFF = 0, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		200	250	μA
				3 V		300	350	
I_{LPM0}	Low-power mode 0 current, (LPM0) see Note 3	f_{MCLK} = 0MHz, $f_{DCO} = f_{SMCLK}$ = 1MHz, f_{ACLK} = 32,768Hz, CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0		2.2 V		32	45	μA
				3 V		55	70	
I_{LPM2}	Low-power mode 1 current, (LPM2) see Note 4	$f_{MCLK} = f_{SMCLK}$ = 0MHz, f_{DCO} = 1MHz, f_{ACLK} = 32,768Hz, CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0		2.2 V		11	14	μA
				3 V		17	22	
I_{LPM3}	Low-power mode 2 current, (LPM3) see Note 4	T_A = −40°C	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0MHz, f_{ACLK} = 32,768Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0	2.2 V		0.7	TBD	μA
		T_A = 25°C				0.7	TBD	
		T_A = 85°C				1.0	TBD	
		T_A = −40°C		3 V		0.9	TBD	
		T_A = 25°C				0.9	TBD	
		T_A = 85°C				1.5	TBD	
I_{LPM4}	Low-power mode 4 current, (LPM4) see Note 5	T_A = −40°C	$f_{DCO} = f_{MCLK} = f_{SMCLK}$ = 0MHz, f_{ACLK} = 32,768Hz, CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1	2.2 V/3 V		0.1	TBD	μA
		T_A = 25°C				0.1	TBD	
		T_A = 85°C				0.8	TBD	

NOTES:
1. All inputs are tied to 0 V or V_{CC}. Outputs do not source or sink any current.
2. The currents are characterized with a KDS Daishinku DT−38 (6 pF) crystal and CAPx = 1.
3. Current for brownout and WDT clocked by SMCLK included.
4. Current for brownout and WDT clocked by ACLK included.
5. Current for brownout included.

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typical supply current (into V_{CC}) characteristics

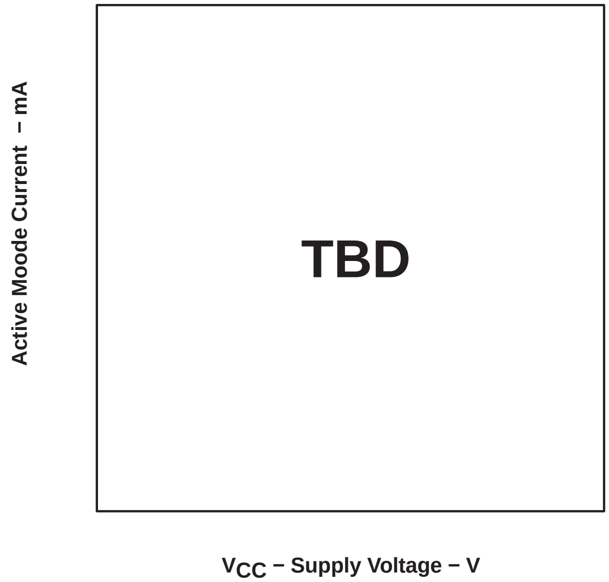

Figure 2. Active mode current vs V_{CC}

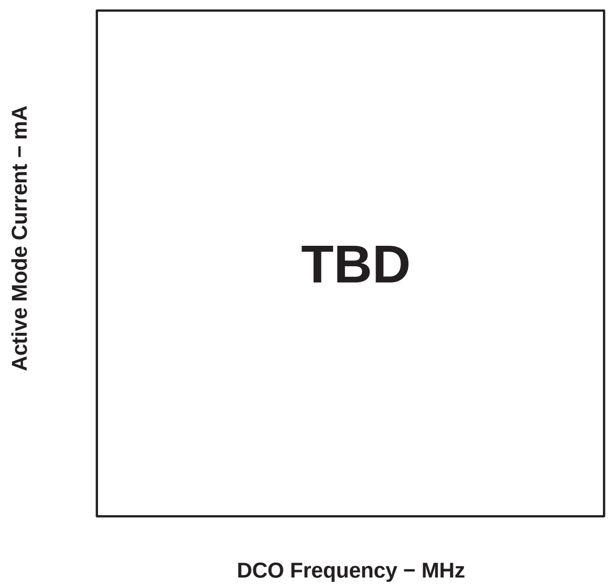

Figure 3. Active mode current vs DCO frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Schmitt-trigger inputs − Ports P1 and P2

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		0.45		0.75	V_{CC}
		V_{CC} = 2.2 V	1.00		1.65	V
		V_{CC} = 3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage		0.25		0.55	V_{CC}
		V_{CC} = 2.2 V	0.55		1.20	V
		V_{CC} = 3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	V_{CC} = 2.2 V	0.2		1.0	V
		V_{CC} = 3 V	0.3		1.0	
R_{Pull}	Pull−up/pull−down resistor	For pull−up: $V_{IN} = V_{SS}$; For pull−down: $V_{IN} = V_{CC}$	TBD		TBD	Ω
C_I	Input Capacitance	$V_{IN} = V_{SS}$ or V_{CC}		TBD		pF

inputs − Ports P1 and P2

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1, P2: P1.x to P2.x, External trigger puls width to set interrupt flag, (see Note 1)	2.2 V	50			ns
			3 V	30			

NOTES: 1. An external signal sets the interrupt flag every time the minimum interrupt puls width $t_{(int)}$ is met. It may be set even with trigger signals shorter than $t_{(int)}$.

leakage current − Ports P1 and P2

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$I_{lkg(Px.x)}$	High-impedance leakage current	see Notes 1 and 2	2.2 V/3 V			±50	nA

NOTES: 1. The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
2. The leakage of the digital port pins is measured individually. The port pin is selected for input and the pull−up/pull−down resistor is disabled.

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

outputs − Ports P1 and P2

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = −1.5 mA (see Notes 1 and 3)	2.2 V	V_{CC}−0.25		V_{CC}	V
		$I_{(OHmax)}$ = −6 mA (see Notes 2 and 3)	2.2 V	V_{CC}−0.6		V_{CC}	
		$I_{(OHmax)}$ = −1.5 mA (see Notes 1 and 3)	3 V	V_{CC}−0.25		V_{CC}	
		$I_{(OHmax)}$ = −6 mA (see Notes 2 and 3)	3 V	V_{CC}−0.6		V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1.5 mA (see Notes 1 and 3)	2.2 V	V_{SS}		V_{SS}+0.25	V
		$I_{(OLmax)}$ = 6 mA (see Notes 2 and 3)	2.2 V	V_{SS}		V_{SS}+0.6	
		$I_{(OLmax)}$ = 1.5 mA (see Notes 1 and 3)	3 V	V_{SS}		V_{SS}+0.25	
		$I_{(OLmax)}$ = 6 mA (see Notes 2 and 3)	3 V	V_{SS}		V_{SS}+0.6	
C_O	Output capacitance				TBD		pF

NOTES: 1. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±12 mA to hold the maximum voltage drop specified.
2. The maximum total current, I_{OHmax} and I_{OLmax}, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
3. One output loaded at a time.

output frequency − Ports P1 and P2

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	Px.y (TBD), C_L = 20 pF, R_L = 1 kOhm (see Note 1 and 2)	2.2 V			10	MHz
			3 V			12	MHz
f_{Port_CLK}	Clock output frequency	P2.0/ACLK, P1.4/SMCLK, C_L = 20 pF (see Note 2)	2.2 V			12	MHz
			3 V			16	MHz

NOTES: 1. A resistive divider with 2 times 0.5 kΩ between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider.
2. The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

outputs − Ports P1 and P2 (continued)

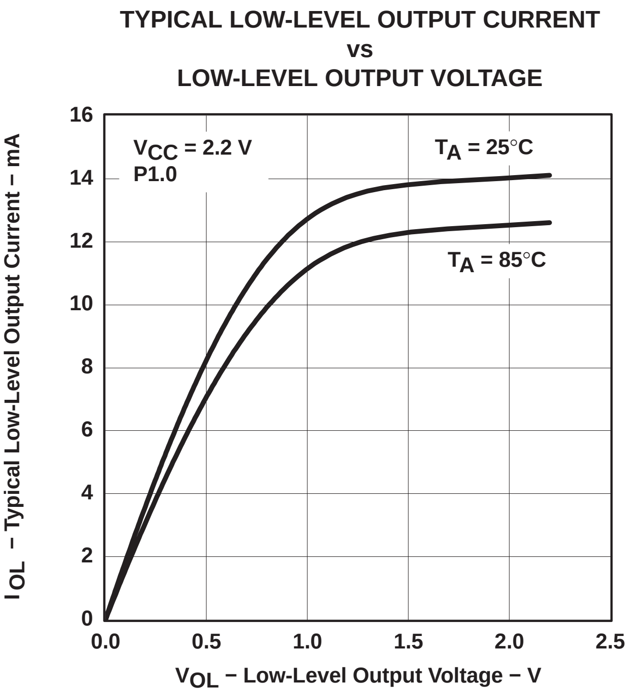

Figure 4

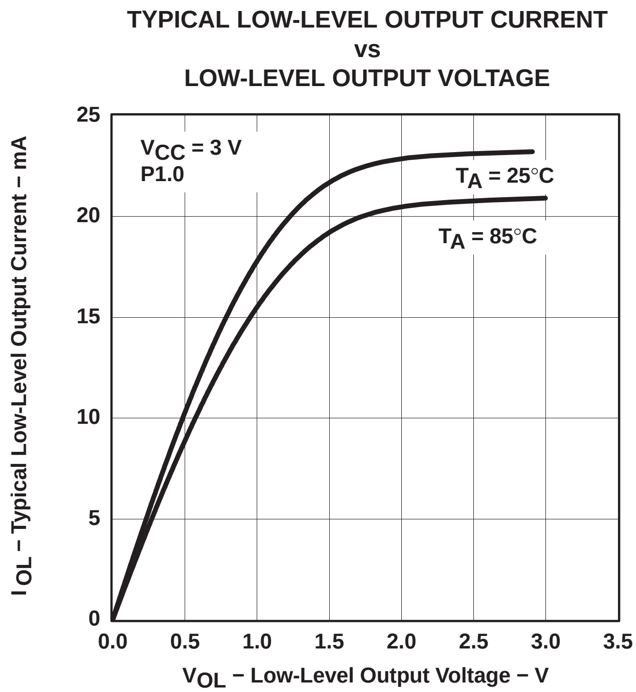

Figure 5

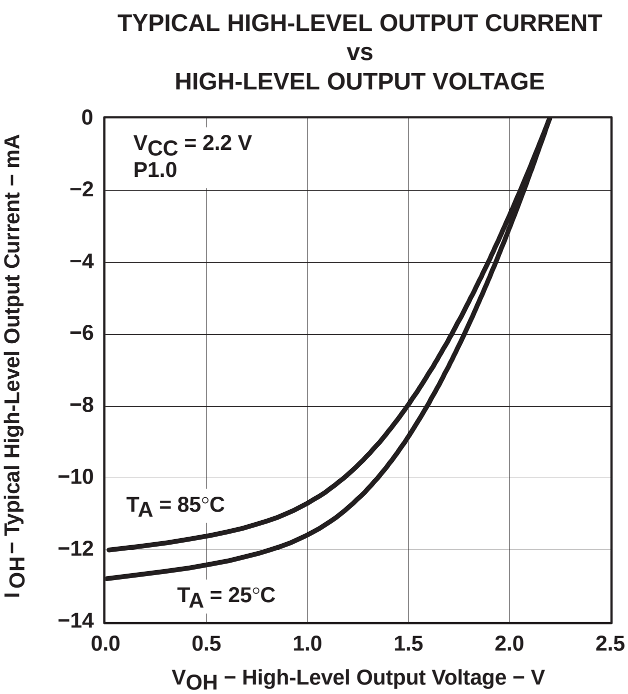

Figure 6

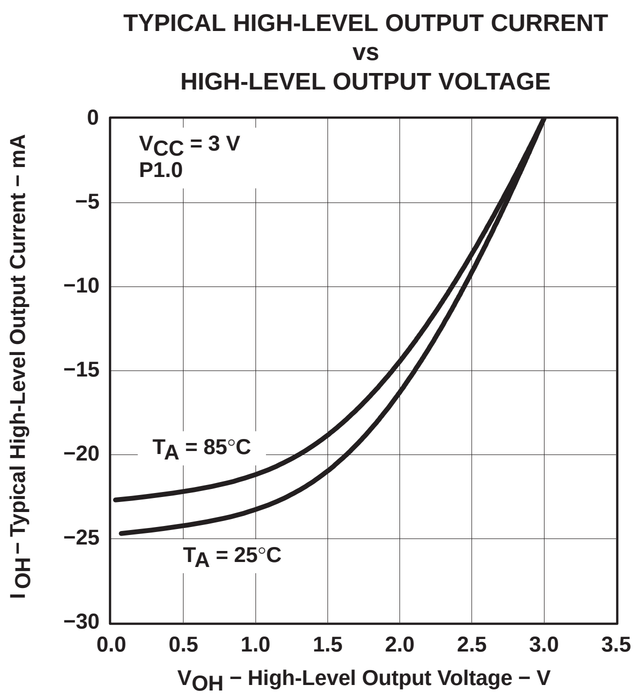

Figure 7

NOTE: One output loaded at a time.

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Timer_A

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A clock frequency	Internal: SMCLK, ACLK; External: TACLK, INCLK; Duty Cycle = 50% ±10%	2.2 V			10	MHz
			3 V			16	
$t_{TA,cap}$	Timer_A, capture timing	TA0, TA1, TA2	2.2 V	50			ns
			3 V	30			

Comparator_A+ (see Note 1)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$I_{(DD)}$		CAON=1, CARSEL=0, CAREF=0	2.2 V		25	40	µA
			3 V		45	60	
$I_{(Refladder/RefDiode)}$		CAON=1, CARSEL=0, CAREF=1/2/3, no load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V		30	50	µA
			3 V		45	71	
$V_{(IC)}$	Common-mode input voltage	CAON =1	2.2 V/3 V	0		$V_{CC}-1$	V
$V_{(Ref025)}$	$\frac{\text{Voltage @ 0.25 } V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=1, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	$\frac{\text{Voltage @ 0.5} V_{CC} \text{ node}}{V_{CC}}$	PCA0=1, CARSEL=1, CAREF=2, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V/3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	(see Figure 8 and Figure 9)	PCA0=1, CARSEL=1, CAREF=3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2, T_A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
$V_{(offset)}$	Offset voltage	See Note 2	2.2 V/3 V	−30		30	mV
V_{hys}	Input hysteresis	CAON=1	2.2 V/3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$		T_A = 25°C, Overdrive 10 mV, Without filter: CAF=0	2.2 V	160	210	300	ns
			3 V	90	150	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF=1	2.2 V	1.4	1.9	3.4	µs
			3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$		T_A = 25°C, Overdrive 10 mV, Without filter: CAF=0	2.2 V	130	210	300	ns
			3 V	80	150	240	
		T_A = 25°C, Overdrive 10 mV, With filter: CAF=1	2.2 V	1.4	1.9	3.4	µs
			3 V	0.9	1.5	2.6	

NOTES: 1. The leakage current for the Comparator_A terminals is identical to $I_{lkg(Px.x)}$ specification.
2. The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements. The two successive measurements are then summed together.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics

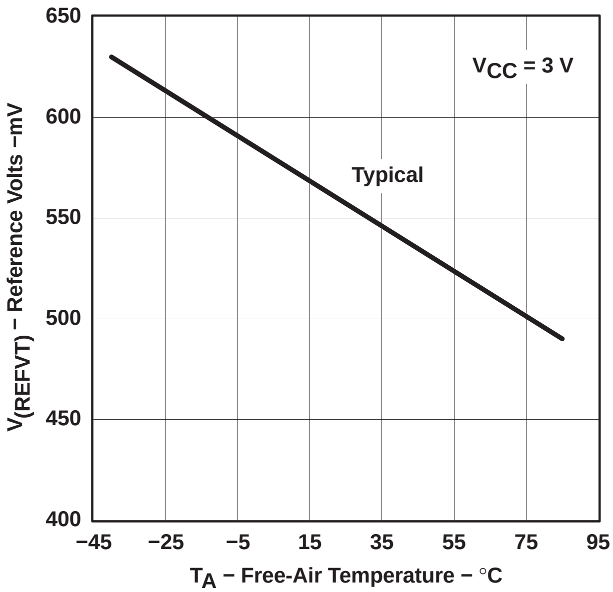

Figure 8. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

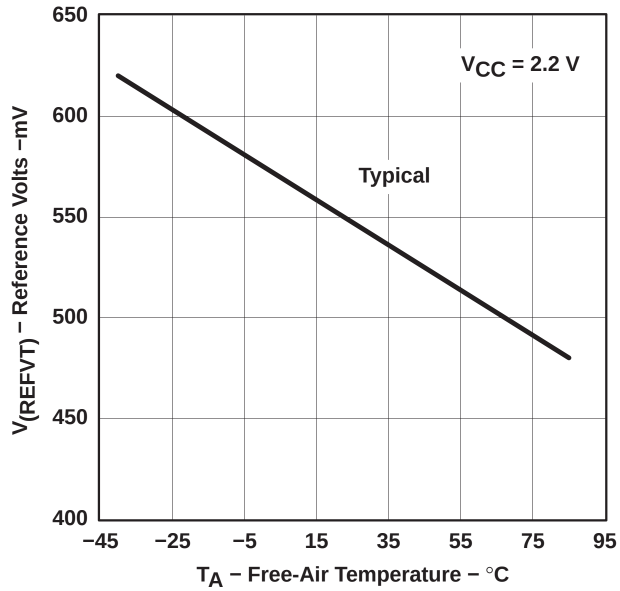

Figure 9. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

typical resistance between CA+ and CA− with CASHORT = 1

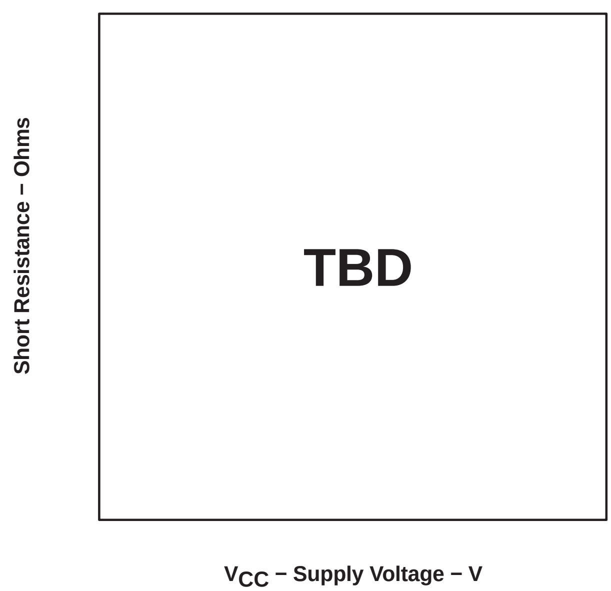

Figure 10. Short resistance vs V_{CC}

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

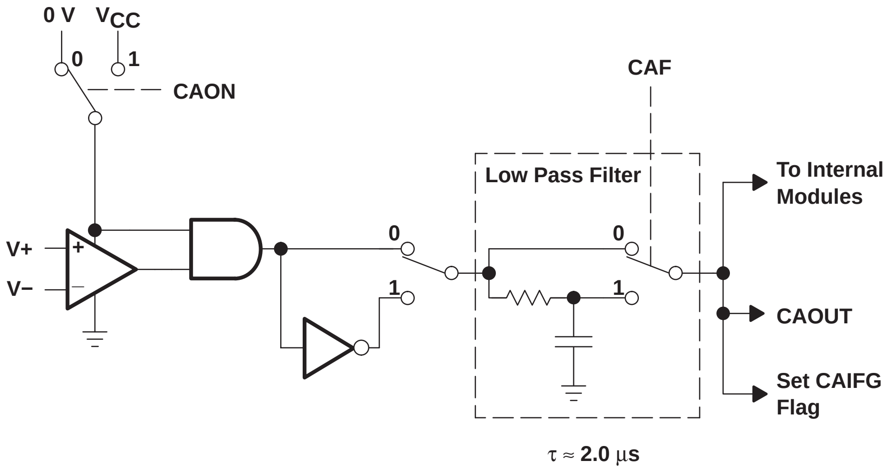

Figure 11. Block Diagram of Comparator_A Module

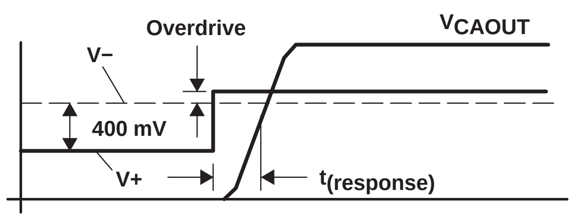

Figure 12. Overdrive Definition

POR/brownout reset (BOR) (see Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(BOR)}$	Brownout (see Note 2)				2000	μs
$V_{CC(start)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 13)		$0.7 \times V_{(B\_IT-)}$		V
$V_{(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 13 through Figure 15)			1.71	V
$V_{hys(B\_IT-)}$		$dV_{CC}/dt \le 3$ V/s (see Figure 13)	70	130	180	mV
$t_{(reset)}$		Pulse length needed at $\overline{RST}$/NMI pin to accepted reset internally, V_{CC} = 2.2 V/3 V	2			μs

NOTES: 1. The current consumption of the brownout module is already included in the I_{CC} current consumption data. The voltage level $V_{(B\_IT-)} + V_{hys(B\_IT-)}$ is ≤ 1.8V.

2. During power up, the CPU begins code execution following a period of $t_{d(BOR)}$ after $V_{CC} = V_{(B\_IT-)} + V_{hys(B\_IT-)}$. The default DCO settings must not be changed until $V_{CC} \ge V_{CC(min)}$, where $V_{CC(min)}$ is the minimum supply voltage for the desired operating frequency.

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical characteristics

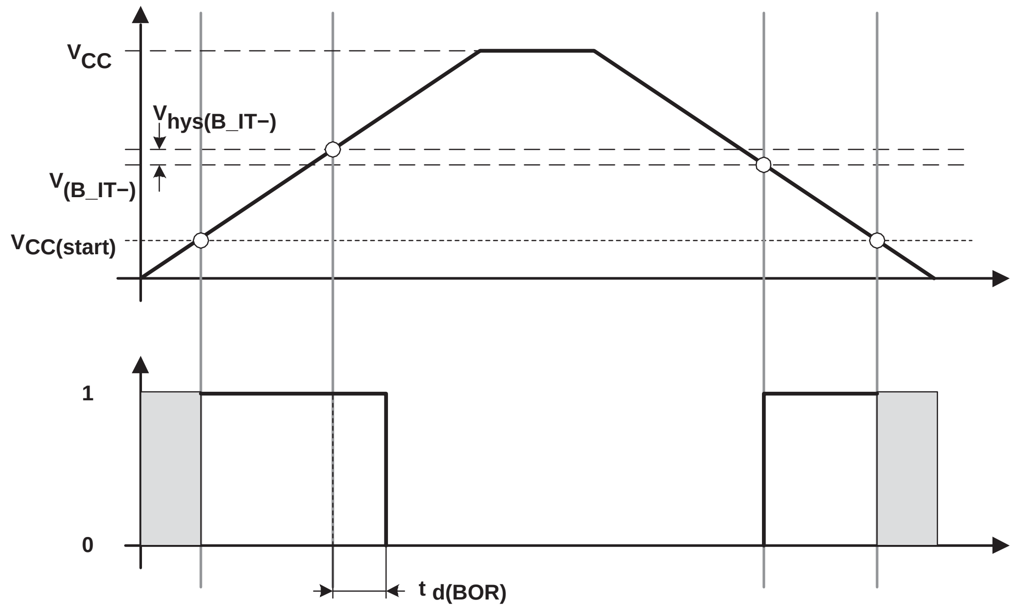

Figure 13. POR/Brownout Reset (BOR) vs Supply Voltage

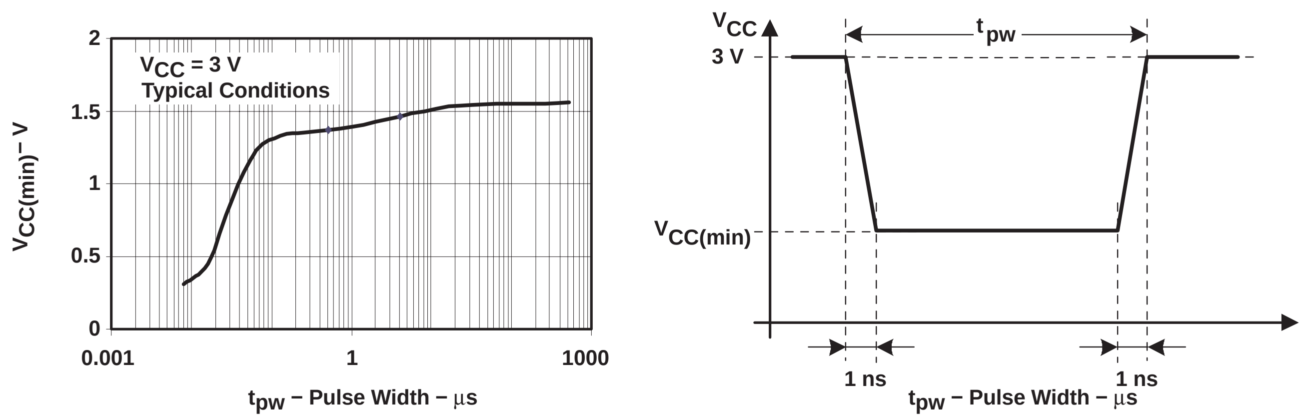

Figure 14. $V_{(CC)min}$ Level With a Square Voltage Drop to Generate a POR/Brownout Signal

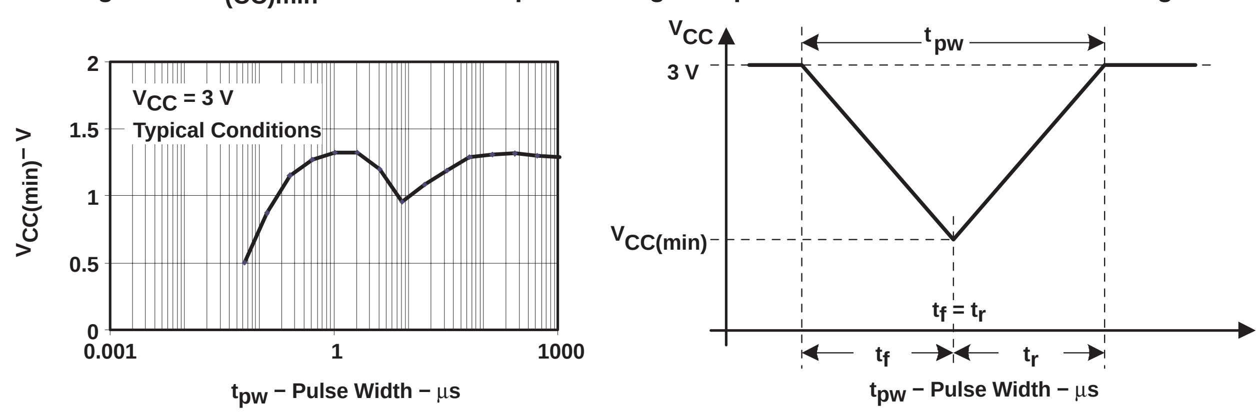

Figure 15. $V_{CC(min)}$ Level With a Triangle Voltage Drop to Generate a POR/Brownout Signal

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

main DCO characteristics

- All ranges selected by RSELx overlap with RSELx + 1: RSELx = 0 overlaps RSELx = 1, ... RSELx = 14 overlaps RSELx = 15.
- DCO control bits DCOx have a step size as defined by parameter S_{DCO}.
- Modulation control bits MODx select how often $f_{DCO(RSEL,DCO+1)}$ is used within the period of 32 DCOCLK cycles. The frequency $f_{DCO(RSEL,DCO)}$ is used for the remaining cycles. The frequency is an average equal to:

$$f_{average} = \frac{32 \times f_{DCO(RSEL,DCO)} \times f_{DCO(RSEL,DCO+1)}}{MOD \times f_{DCO(RSEL,DCO)} + (32 - MOD) \times f_{DCO(RSEL,DCO+1)}}$$

DCO frequency

PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$f_{DCO(0,3)}$	RSELx = 0, DCOx = 3, MODx = 0	2.2 V/3 V	0.08		0.12	MHz
$f_{DCO(1,3)}$	RSELx = 1, DCOx = 3, MODx = 0	2.2 V/3 V	0.10		0.15	MHz
$f_{DCO(2,3)}$	RSELx = 2, DCOx = 3, MODx = 0	2.2 V/3 V	0.14		0.20	MHz
$f_{DCO(3,3)}$	RSELx = 3, DCOx = 3, MODx = 0	2.2 V/3 V	0.21		0.29	MHz
$f_{DCO(4,3)}$	RSELx = 4, DCOx = 3, MODx = 0	2.2 V/3 V	0.29		0.40	MHz
$f_{DCO(5,3)}$	RSELx = 5, DCOx = 3, MODx = 0	2.2 V/3 V	0.41		0.56	MHz
$f_{DCO(6,3)}$	RSELx = 6, DCOx = 3, MODx = 0	2.2 V/3 V	0.58		0.77	MHz
$f_{DCO(7,3)}$	RSELx = 7, DCOx = 3, MODx = 0	2.2 V/3 V	0.81		1.07	MHz
$f_{DCO(8,3)}$	RSELx = 8, DCOx = 3, MODx = 0	2.2 V/3 V	1.14		1.54	MHz
$f_{DCO(9,3)}$	RSELx = 9, DCOx = 3, MODx = 0	2.2 V/3 V	1.67		2.27	MHz
$f_{DCO(10,3)}$	RSELx = 10, DCOx = 3, MODx = 0	2.2 V/3 V	2.35		3.25	MHz
$f_{DCO(11,3)}$	RSELx = 11, DCOx = 3, MODx = 0	2.2 V/3 V	2.94		4.07	MHz
$f_{DCO(12,3)}$	RSELx = 12, DCOx = 3, MODx = 0	2.2 V/3 V	4.15		5.67	MHz
$f_{DCO(13,3)}$	RSELx = 13, DCOx = 3, MODx = 0	2.2 V/3 V	5.70		7.45	MHz
$f_{DCO(14,3)}$	RSELx = 14, DCOx = 3, MODx = 0	2.2 V/3 V	8.25		11.3	MHz
$f_{DCO(15,3)}$	RSELx = 15, DCOx = 3, MODx = 0	2.2 V/3 V	10.9		16.5	MHz
$f_{DCO(15,7)}$	RSELx = 15, DCOx = 7, MODx = 0	2.2 V/3 V	16.0		23.0	MHz
S_{RSEL}	$S_{RSEL} = f_{DCO(RSEL+1,DCO)}/f_{DCO(RSEL,DCO)}$	2.2 V/3 V			1.4	ratio
S_{DCO}	$S_{DCO} = f_{DCO(RSEL,DCO+1)}/f_{DCO(RSEL,DCO)}$	2.2 V/3 V	1.05	1.10	1.12	ratio
Duty Cycle	Measured at P1.4/SMCLK	2.2 V/3 V	45	50	55	%

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

DCO drift

$D_{T(0,3)}$	Temperature drift (Box Method), RSELx = 0, DCOx = 3, MODx = 0 T_A = −40°C − +85°C (see Note 1)	2.2 V/3 V	TBD	%
$D_{T(7,3)}$	Temperature drift (Box Method), RSELx = 7, DCOx = 3, MODx = 0 T_A = −40°C − +85°C (see Note 1)	2.2 V/3 V	TBD	%
$D_{T(15,3)}$	Temperature drift (Box Method), RSELx = 15, DCOx = 3, MODx = 0 T_A = −40°C − +85°C (see Note 1)	2.2 V/3 V	TBD	%
$D_{V(0,3)}$	Supply voltage drift (Box Method), RSELx = 0, DCOx = 3, MODx = 0 T_A = 25°C (see Note 1)	1.8 V − 3.6 V	TBD	%
$D_{T(7,3)}$	Supply voltage drift (Box Method), RSELx = 7, DCOx = 3, MODx = 0 T_A = 25°C (see Note 1)	1.8 V − 3.6 V	TBD	%
$D_{T(15,3)}$	Supply voltage drift (Box Method), RSELx = 15, DCOx = 3, MODx = 0 T_A = 25°C (see Note 1)	1.8 V − 3.6 V	TBD	%
$D_{T(0,3)}$	Total drift (Box Method), RSELx = 0, DCOx = 3, MODx = 0 T_A = −40°C − +85°C (see Note 1)	1.8 V − 3.6 V	TBD	%
$D_{T(7,3)}$	Total drift (Box Method), RSELx = 7, DCOx = 3, MODx = 0 T_A = −40°C − +85°C (see Note 1)	1.8 V − 3.6 V	TBD	%
$D_{T(15,3)}$	Total drift (Box Method), RSELx = 15, DCOx = 3, MODx = 0 T_A = −40°C − +85°C (see Note 1)	1.8 V − 3.6 V	TBD	%

NOTE 1: These parameters are not production tested.

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

wake-up from lower power modes (LPM3/4)

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$t_{Clock,LPM3/4}$	DCO clock wake−up time from LPM3/4 (see Note 1)	$f_{DCO} = f_{DCO(3,3)}$, RSELx = 3, DCOx = 3	2.2 V/3 V			7	µs
		$f_{DCO} = f_{DCO(7,3)}$, RSELx = 7, DCOx = 3	2.2 V/3 V			2	
		$f_{DCO} = f_{DCO(11,3)}$, RSELx = 11, DCOx = 3	2.2 V/3 V			1.5	
		$f_{DCO} = f_{DCO(15,3)}$, RSELx = 15, DCOx = 3	2.2 V/3 V			1.0	
$t_{CPU,LPM3/4}$	CPU wake−up time from LPM3/4 (see Note 2)				$1/f_{MCLK} + t_{Clock,LPM3/4}$		

NOTES: 1. The DCO clock wake−up time is measured from the edge of an external wake−up signal (e.g. port interrupt) to the first clock edge observable externally on a clock pin (MCLK or SMCLK).
2. Parameter applicable only if DCOCLK is used for MCLK.

typical wake−up time characteristics

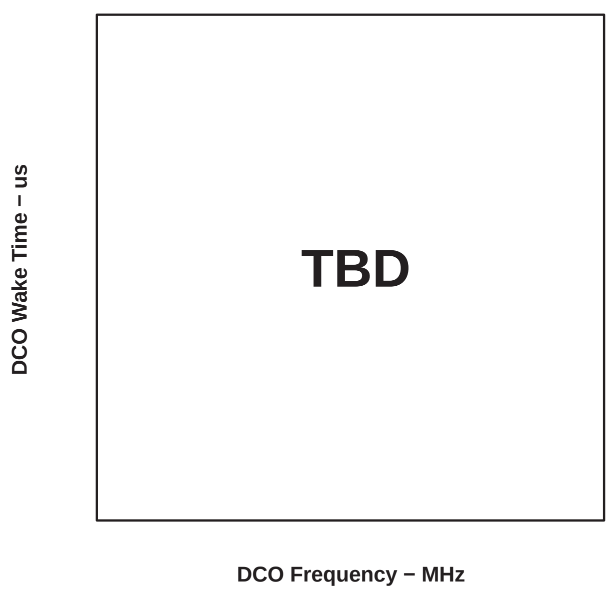


Figure 16. Clock wake−up time vs DCO frequency

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

crystal oscillator, LFXT1

PARAMETER		TEST CONDITIONS	VCC	MIN	TYP	MAX	UNIT
$f_{LFXT1,LF}$	LFXT1 oscillator crystal frequency, LF mode 0, 1	XTS = 0, LFXT1Sx = 0 or 1			32,768		Hz
$f_{LFXT1,HF0}$	LFXT1 oscillator crystal frequency, HF mode 0	XTS = 1, LFXT1Sx = 0		0.4		1	MHz
$f_{LFXT1,HF1}$	LFXT1 oscillator crystal frequency, HF mode 1	XTS = 1, LFXT1Sx = 1		1		4	MHz
$f_{LFXT1,HF2}$	LFXT1 oscillator crystal frequency, HF mode 2	XTS = 1, LFXT1Sx = 2		2		16	MHz
$f_{LFXT1,LF,logic}$	LFXT1 oscillator logic level square wave input frequency, LF mode	XTS = 0, LFXT1Sx = 3		10,000	32,768	50,000	Hz
$f_{LFXT1,HF,logic}$	LFXT1 oscillator logic level square wave input frequency, HF mode	XTS = 1, LFXT1Sx = 3		0.4		16	MHz
ESR_{LF}	Supported ESR for LF crystals	XTS = 0, LFXT1Sx = 0 or 1		20		100	kΩ
ESR_{HF}	Supported ESR for HF crystals (refer to Figure 17 and Figure 18)	XTS = 0, LFXT1Sx = 0, $f_{LFXT1,HF}$ = 1 MHz, C_L = 32 pF			500		Ω
		XTS = 0, LFXT1Sx = 1 $f_{LFXT1,HF}$ = 4 MHz, C_L = 32 pF			100		Ω
		XTS = 0, LFXT1Sx = 2 $f_{LFXT1,HF}$ = 16 MHz, C_L = 32 pF			50		Ω
C_{XIN}	Input capacitance (see Note 1)	XTS = 0, XCAPx = 0			2		pF
		XTS = 0, XCAPx = 1			11		pF
		XTS = 0, XCAPx = 2			17		pF
		XTS = 0, XCAPx = 3			22		pF
		XTS = 1 (see Note 2)			2		pF
C_{XOUT}	Output capacitance (see Note 1)	XTS = 0, XCAPx = 0			2		pF
		XTS = 0, XCAPx = 1			11		pF
		XTS = 0, XCAPx = 2			17		pF
		XTS = 0, XCAPx = 3			22		pF
		XTS = 1 (see Note 2)			2		pF
Duty Cycle	LF mode	XTS = 0, Measured at P1.4/ACLK, $f_{LFXT1,LF}$ = 32,768 Hz	2.2 V/ 3 V	30	50	70	%
	HF mode	XTS = 1, Measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 10 MHz	2.2 V/ 3 V	35	50	65	%
		XTS = 1, Measured at P1.4/ACLK, $f_{LFXT1,HF}$ = 16 MHz	2.2 V/ 3 V	40	50	60	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode	XTS = 0, LFXT1Sx = 3 (see Note 3)	2.2 V/ 3 V	TBD		10,000	Hz
$f_{Fault,HF}$	Oscillator fault frequency, HF mode	XTS = 1, LFXT1Sx = 3 (see Note 3)	2.2 V/ 3 V	0.05		0.25	MHz

NOTES: 1. Includes parasitic bond and package capacitance (approximately 2pF).
2. Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
3. Measured with logic level input frequency but also applies to operation with crystals.

PRODUCT PREVIEW

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

typical operating areas for oscillator LFXT1 in HF mode (XTS = 1)

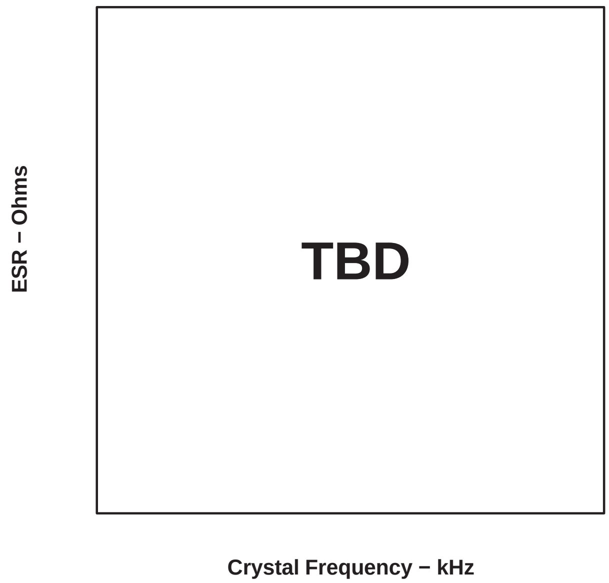


Figure 17. ESR with Safety Factor (SF) = 3 vs Crystal Frequency, C_L = 32 pF

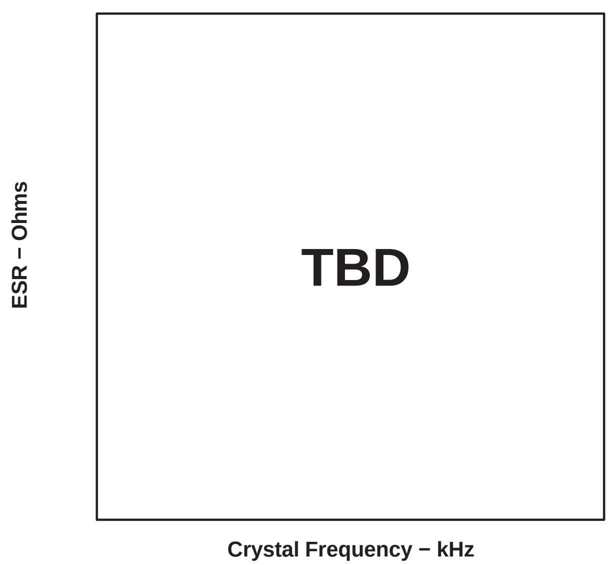


Figure 18. ESR with Safety Factor (SF) = 3 vs Crystal Frequency, C_L = 15 pF

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

Flash Memory

PARAMETER		TEST CONDITIONS	VCC	MIN	NOM	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and Erase supply voltage			2.2		3.6	V
f_{FTG}	Flash Timing Generator frequency			257		476	kHz
I_{PGM}	Supply current from V_{CC} during program		2.7 V/ 3.6 V		3	5	mA
I_{ERASE}	Supply current from V_{CC} during erase		2.7 V/ 3.6 V		3	7	mA
t_{CPT}	Cumulative program time	see Note 1	2.7 V/ 3.6 V			4	ms
$t_{CMErase}$	Cumulative mass erase time		2.7 V/ 3.6 V	20			ms
	Program/Erase endurance			10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C		100			years
t_{Word}	Word or byte program time	see Note 2			30		t_{FTG}
$t_{Block, 0}$	Block program time for 1st byte or word				25		
$t_{Block, 1-63}$	Block program time for each additional byte or word				18		
$t_{Block, End}$	Block program end-sequence wait time				6		
$t_{Mass Erase}$	Mass erase time				10593		
$t_{Seg Erase}$	Segment erase time				4819		

NOTES: 1. The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word/byte write and block write modes.
2. These values are hardwired into the Flash Controller's state machine ($t_{FTG} = 1/f_{FTG}$).

RAM

PARAMETER		MIN	NOM	MAX	UNIT
$V_{(RAMh)}$	CPU halted (see Note 1)	1.6			V

NOTE 1: This parameter defines the minimum supply voltage V_{CC} when the data in the program memory RAM remains unchanged. No program execution should happen during this supply voltage condition.

JTAG Interface

PARAMETER		TEST CONDITIONS	VCC	MIN	NOM	MAX	UNIT
f_{TCK}	TCK input frequency	see Note 1	2.2 V	0		5	MHz
			3 V	0		10	MHz
$R_{Internal}$	Internal pull-down resistance on TEST		2.2 V/ 3 V	25	60	90	kΩ

NOTES: 1. f_{TCK} may be restricted to meet the timing requirements of the module selected.

JTAG Fuse (see Note 1)

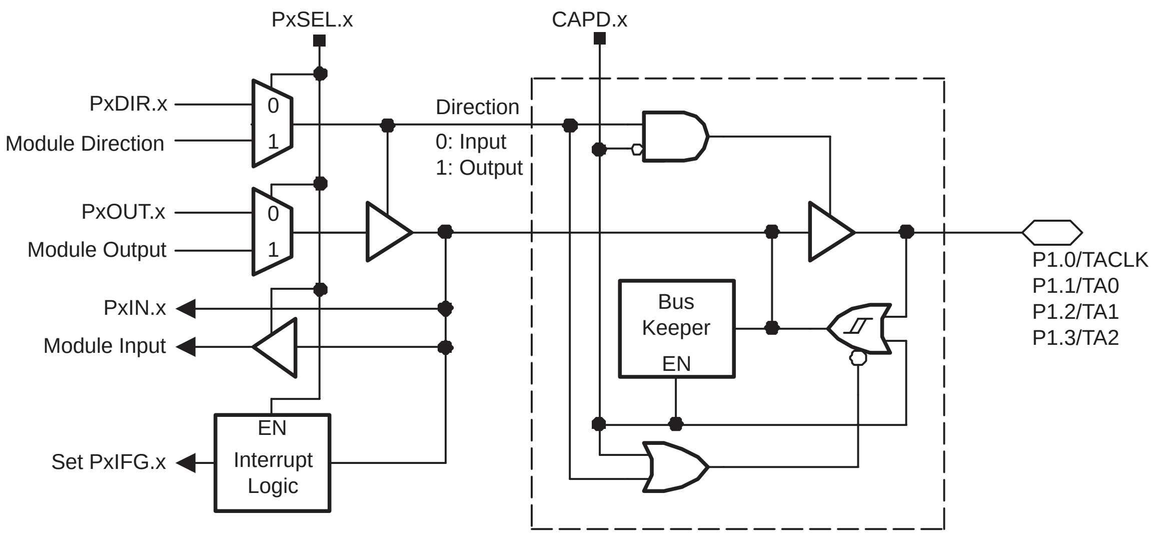
PARAMETER		TEST CONDITIONS	VCC	MIN	NOM	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse-blow condition	T_A = 25°C		2.5			V
V_{FB}	Voltage level on TEST for fuse-blow			6		7	V
I_{FB}	Supply current into TEST during fuse blow					100	mA
t_{FB}	Time to blow fuse					1	ms

NOTES: 1. Once the fuse is blown, no further access to the JTAG/Test and emulation feature is possible and is switched to bypass mode.

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P1 pin schematic: P1.0 to P1.3, input/output with Schmitt-trigger



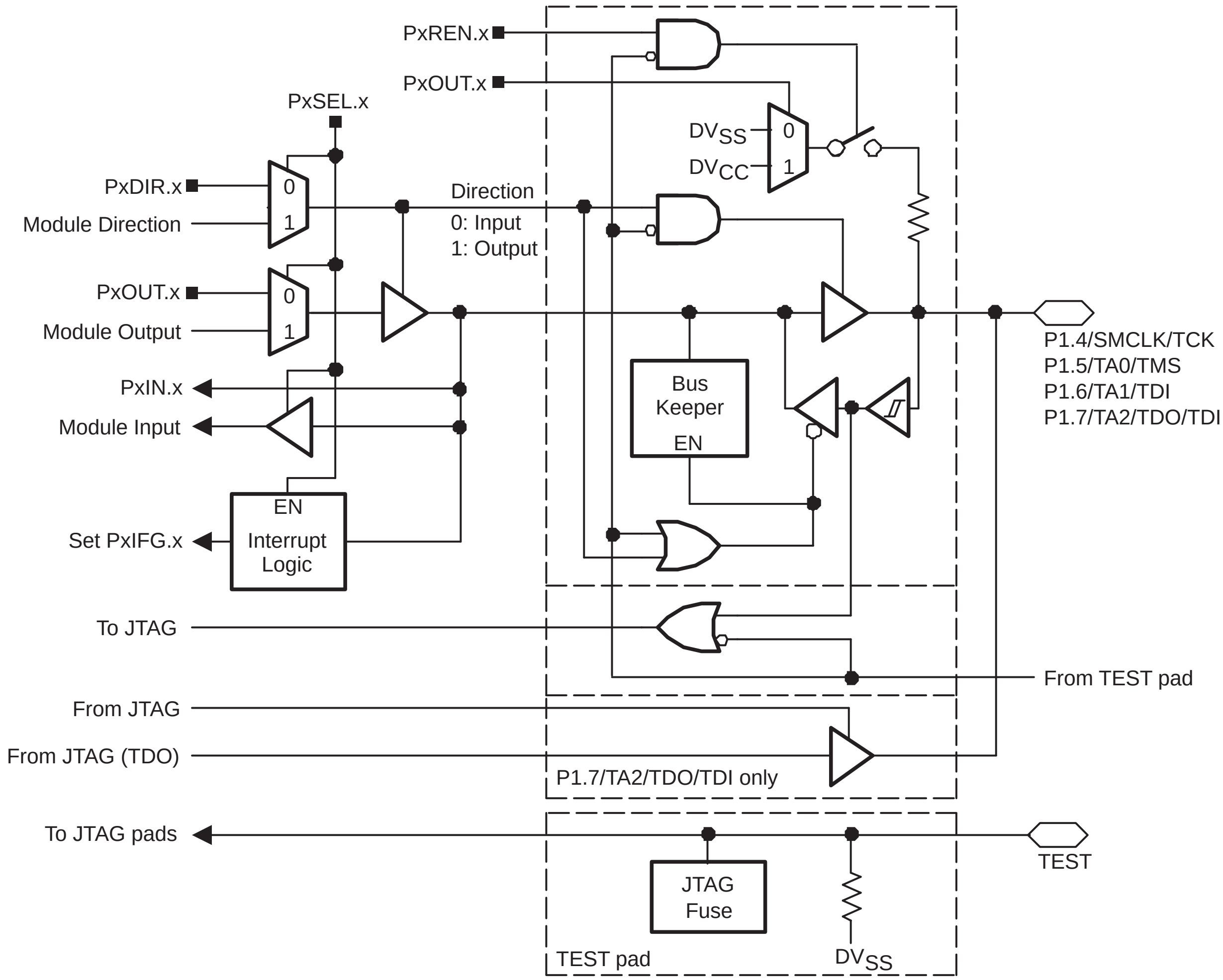
	PRIMARY FUNCTION		SECONDARY FUNCTION			
	GPIO		*Module IO*		*Analog IO*	*JTAG*
Control Bits/Signals	input	output	input	output		
P1SEL.x	0†	0	1	1	N/A	N/A
P1DIR.x	0†	1	0	1	N/A	N/A
Pin Name (P1.x)						
P1.0/TACLK	P1.0 input†	P1.0 output	Timer_A3.TACLK	DV_{SS}	N/A	N/A
P1.1/TA0	P1.1 input†	P1.1 output	Timer_A3.CCI0A	Timer_A3.TA0	N/A	N/A
P1.2/TA1	P1.2 input†	P1.2 output	Timer_A3.CCI1A	Timer_A3.TA1	N/A	N/A
P1.3/TA2	P1.3 input†	P1.3 output	Timer_A3.CCI2A	Timer_A3.TA2	N/A	N/A

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.

APPLICATION INFORMATION

Port P1 pin schematic: P1.4 to P1.7, input/output with Schmitt-trigger and in-system access features

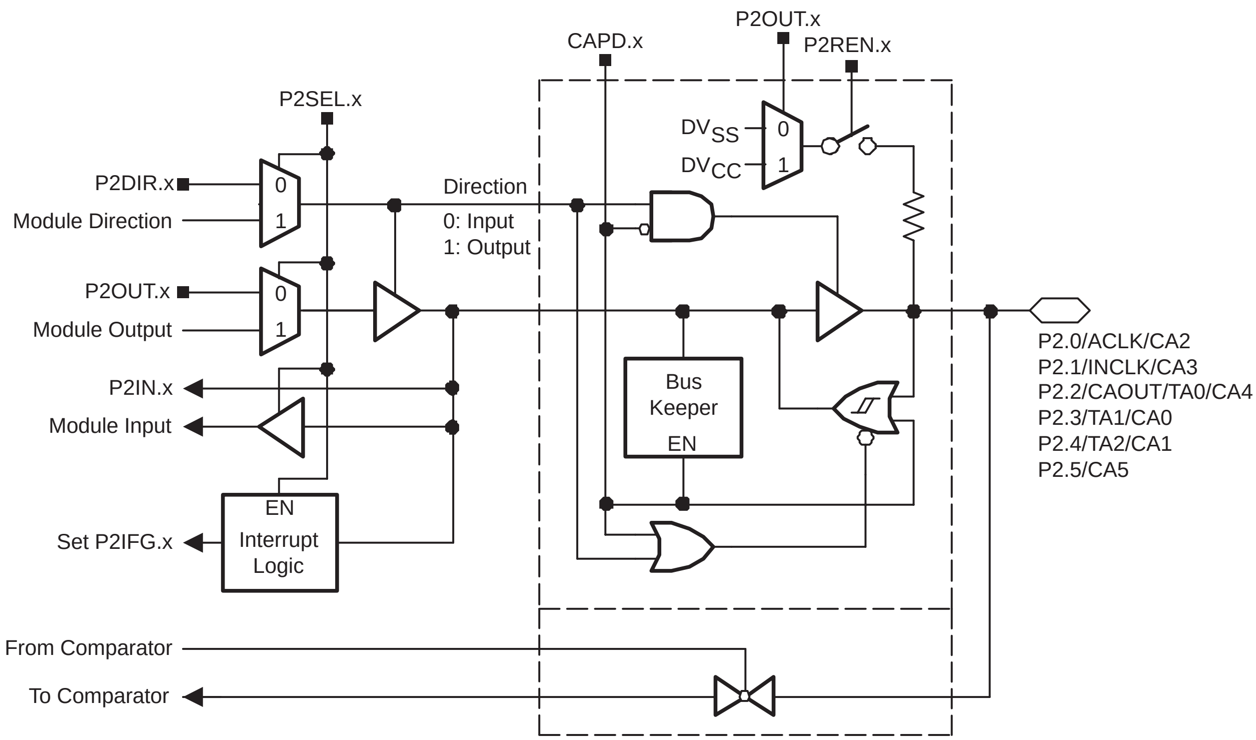


	PRIMARY FUNCTION		SECONDARY FUNCTION			
	GPIO		*Module IO*		*Analog IO*	*JTAG*
Control Bits/Signals	input	output	input	output		
P1SEL.x	0†	0	1	1	N/A	X
P1DIR.x	0†	1	0	1	N/A	X
TEST (from pin)	0†	0	0	0	N/A	1
Pin Name (P1.x)						
P1.4/SMCLK/TCK	P1.4 input†	P1.4 output	N/A	SMCLK	N/A	TCK
P1.5/TA0/TMS	P1.5 input†	P1.5 output	N/A	Timer_A3.TA0	N/A	TMS
P1.6/TA1/TDI/TCLK	P1.6 input†	P1.6 output	N/A	Timer_A3.TA1	N/A	TDI/TCLK‡
P1.7/TA2/TDO/TDI	P1.7 input†	P1.7 output	N/A	Timer_A3.TA2	N/A	TDO/TDI‡

† Default after reset (PUC/POR)
† Function controlled by JTAG
NOTES: 1. N/A: Not available or not applicable.
2. X: Don't care.

APPLICATION INFORMATION

Port P2 pin schematic: P2.0 to P2.5, input/output with Schmitt-trigger



	PRIMARY FUNCTION		SECONDARY FUNCTION			
	GPIO		*Module IO*		*Analog IO*	*JTAG*
Control Bits/Signals	input	output	input	output		
P2SEL.x	0†	0	1	1	X	N/A
P2DIR.x	0†	1	0	1	X	N/A
CAPD.x	0†	0	0	0	1	N/A
Pin Name (P2.x)						
P2.0/ACLK/CA2	P2.0 input†	P2.0 output	N/A	ACLK	CA2	N/A
P2.1/INCLK/CA3	P2.1 input†	P2.1 output	Timer_A3.INCLK	DV_{SS}	CA3	N/A
P2.2/CAOUT/TA0/CA4	P2.2 input†	P2.2 output	Timer_A3.CCI0B	Comparator_A.OUT	CA4	N/A
P2.3/TA1/CA0	P2.3 input†	P2.3 output	N/A	Timer_A3.TA1	CA0	N/A
P2.4/TA2/CA1	P2.4 input†	P2.4 output	N/A	Timer_A3.TA2	CA1	N/A
P2.5/CA5	P2.5 input†	P2.5 output	N/A	N/A	CA5	N/A

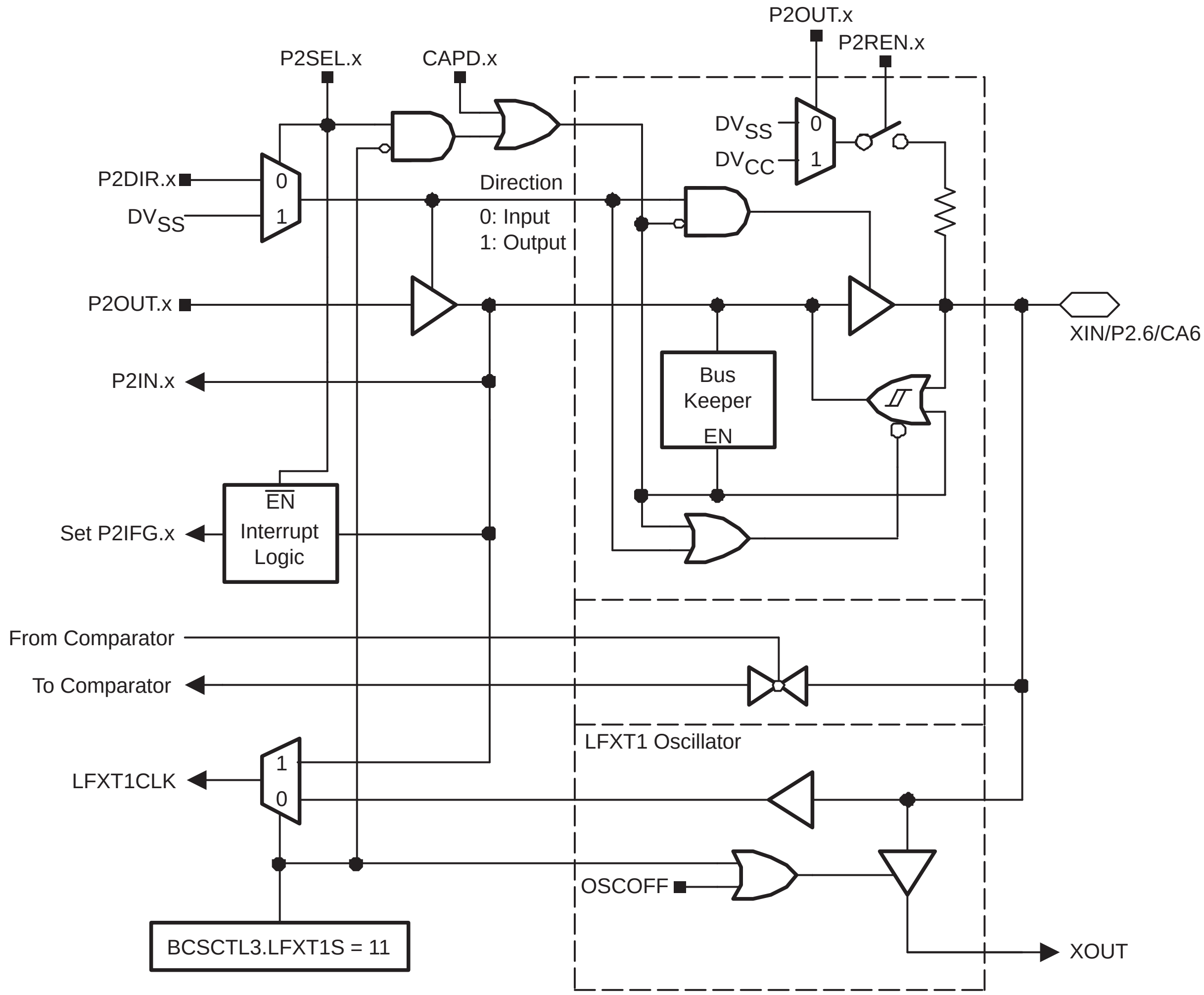
† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don’t care.

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P2 pin schematic: P2.6, input/output with Schmitt-trigger and crystal oscillator input



	PRIMARY FUNCTION		SECONDARY FUNCTION			
	GPIO		*Module IO*		*Analog IO*	*JTAG*
Control Bits/Signals	input	output	input	output		
P2SEL.x	0	0	1†	N/A	0	N/A
P2DIR.x	0†	1	X	N/A	X	N/A
CAPD.x	0†	0	X	N/A	1	N/A
Pin Name (P2.x)						
P2.6/XIN/CA6	P2.6 input	P2.6 output	XIN†	N/A	CA6	N/A

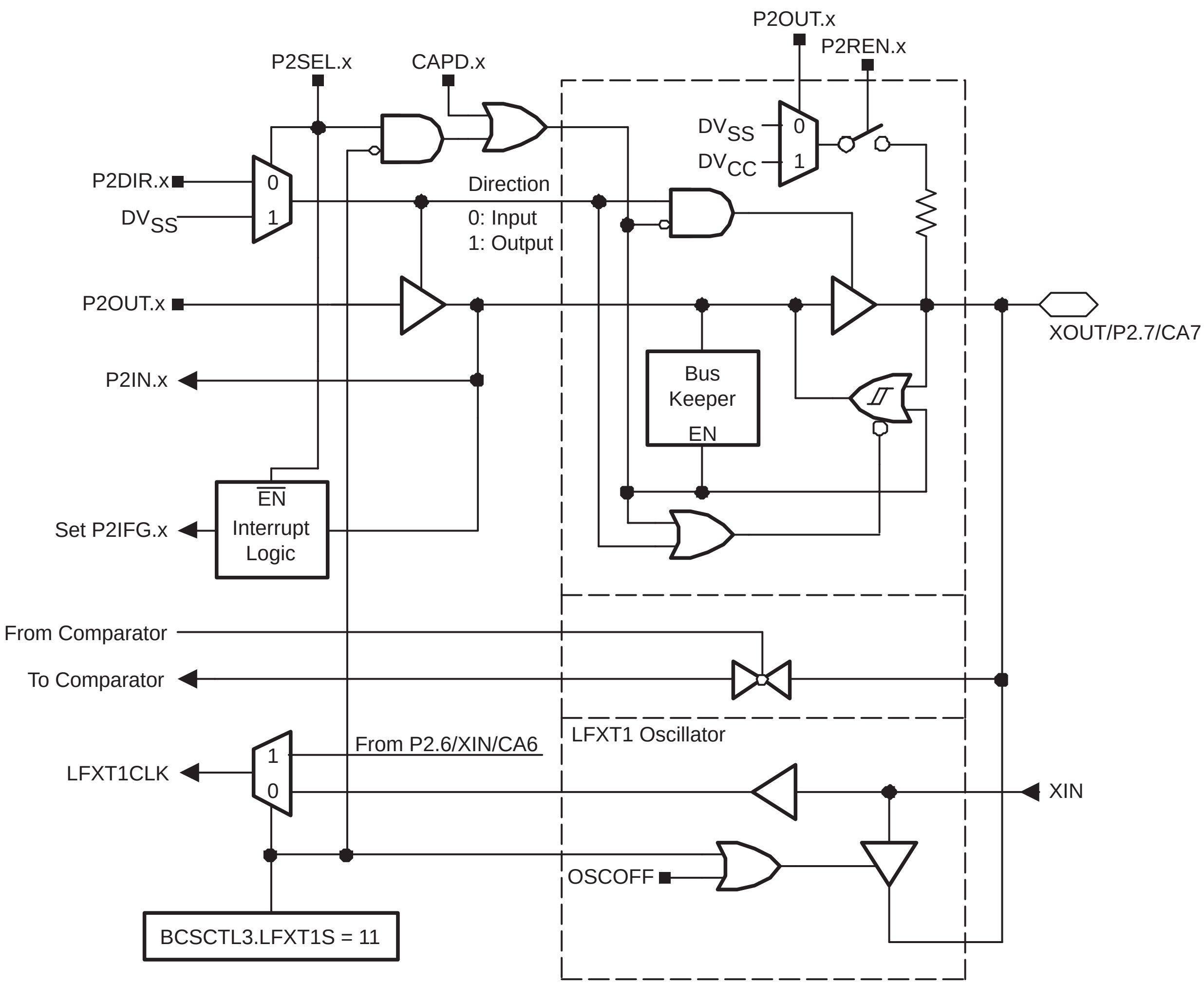
† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don’t care.

PRODUCT PREVIEW

APPLICATION INFORMATION

Port P2 pin schematic: P2.7, input/output with Schmitt-trigger and crystal oscillator output



	PRIMARY FUNCTION		SECONDARY FUNCTION			
	GPIO		*Module IO*		*Analog IO*	*JTAG*
Control Bits/Signals	input	output	input	output		
P2SEL.x	0	0	N/A	1†	0	N/A
P2DIR.x	0†	1	N/A	X	X	N/A
CAPD.x	0†	0	N/A	X	1	N/A
Pin Name (P2.x)						
XOUT/P2.7/CA7	P2.7 input	P2.7 output	N/A	XOUT†	CA7	N/A

† Default after reset (PUC/POR)

NOTES: 1. N/A: Not available or not applicable.
2. X: Don’t care.
3. If the pin XOUT/P2.7/CA7 is used as an input a current can flow until P2SEL.7 is cleared due to the oscillator output driver connection to this pin after reset.

JTAG fuse check mode

MSP430 devices that have the fuse on the TEST terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current, I_{TF}, of 1 mA at 3 V, 2.5 mA at 5 V can flow from the TEST pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

When the TEST pin is again taken low after a test or programming session, the fuse check mode and sense currents are terminated.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current will only flow when the fuse check mode is active and the TMS pin is in a low state (see Figure 19). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

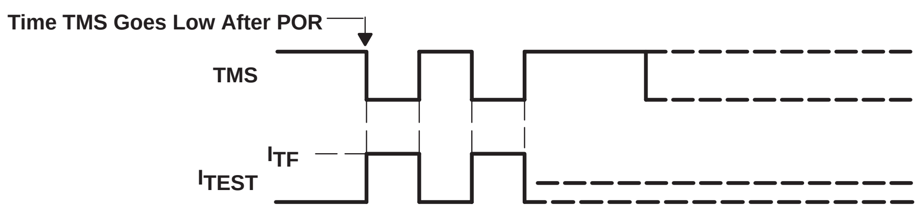


Figure 19. Fuse Check Mode Current, MSP430F21x1

NOTE:
The CODE and RAM data protection is ensured if the JTAG fuse is blown and the 256-bit bootloader access key is used. Also, see the *bootstrap loader* section for more information.

PRODUCT PREVIEW

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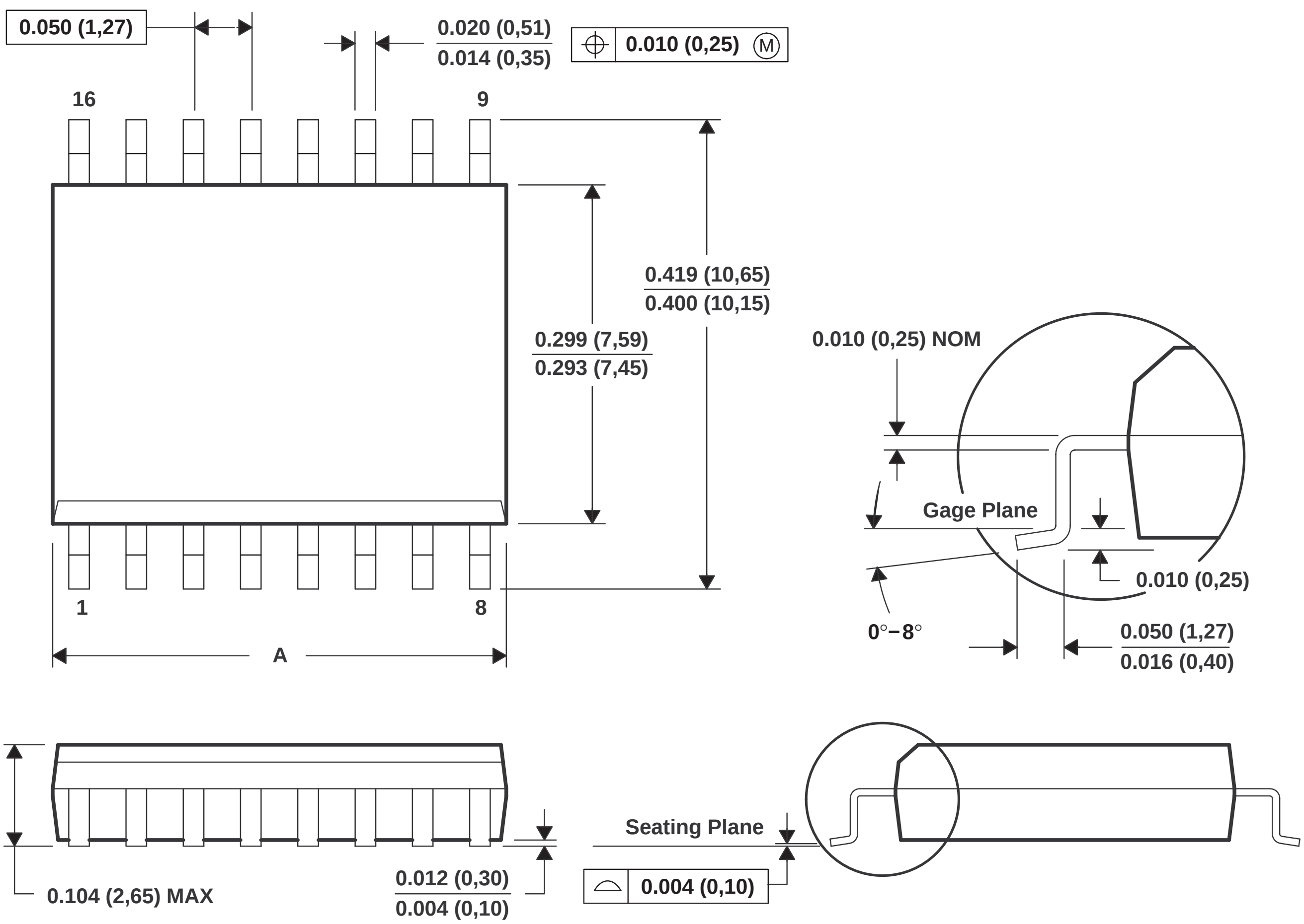
MECHANICAL DATA

DW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

16 PIN SHOWN



DIM \ PINS **	16	20	24
A MAX	0.410 (10,41)	0.510 (12,95)	0.610 (15,49)
A MIN	0.400 (10,16)	0.500 (12,70)	0.600 (15,24)

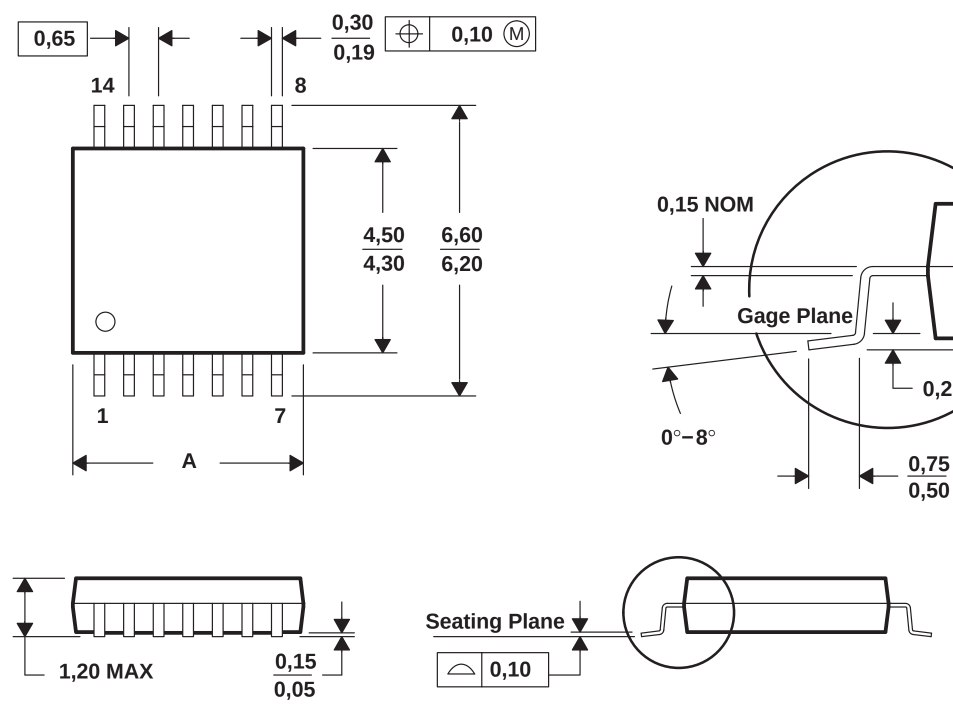
4040000/D 02/98

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-013

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PRODUCT PREVIEW

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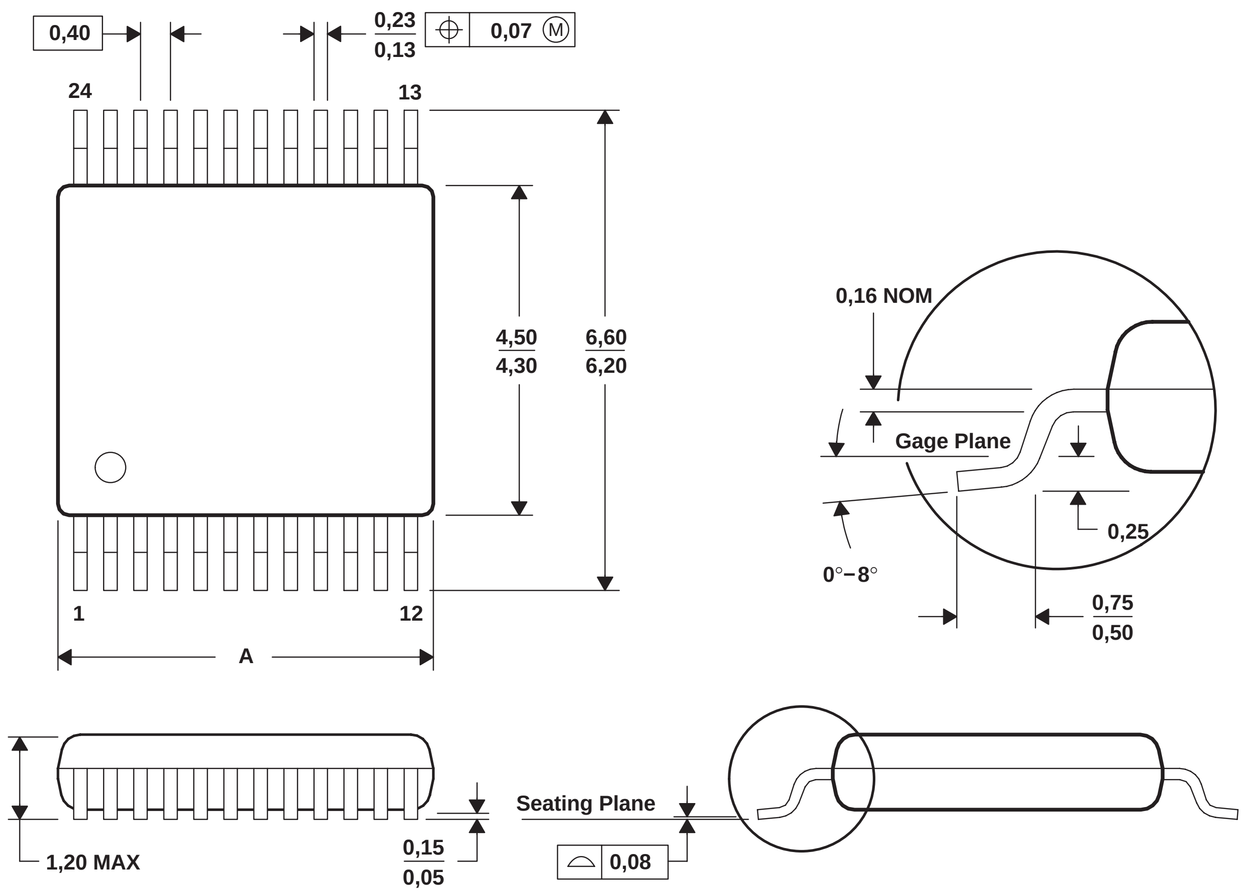
MECHANICAL DATA

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



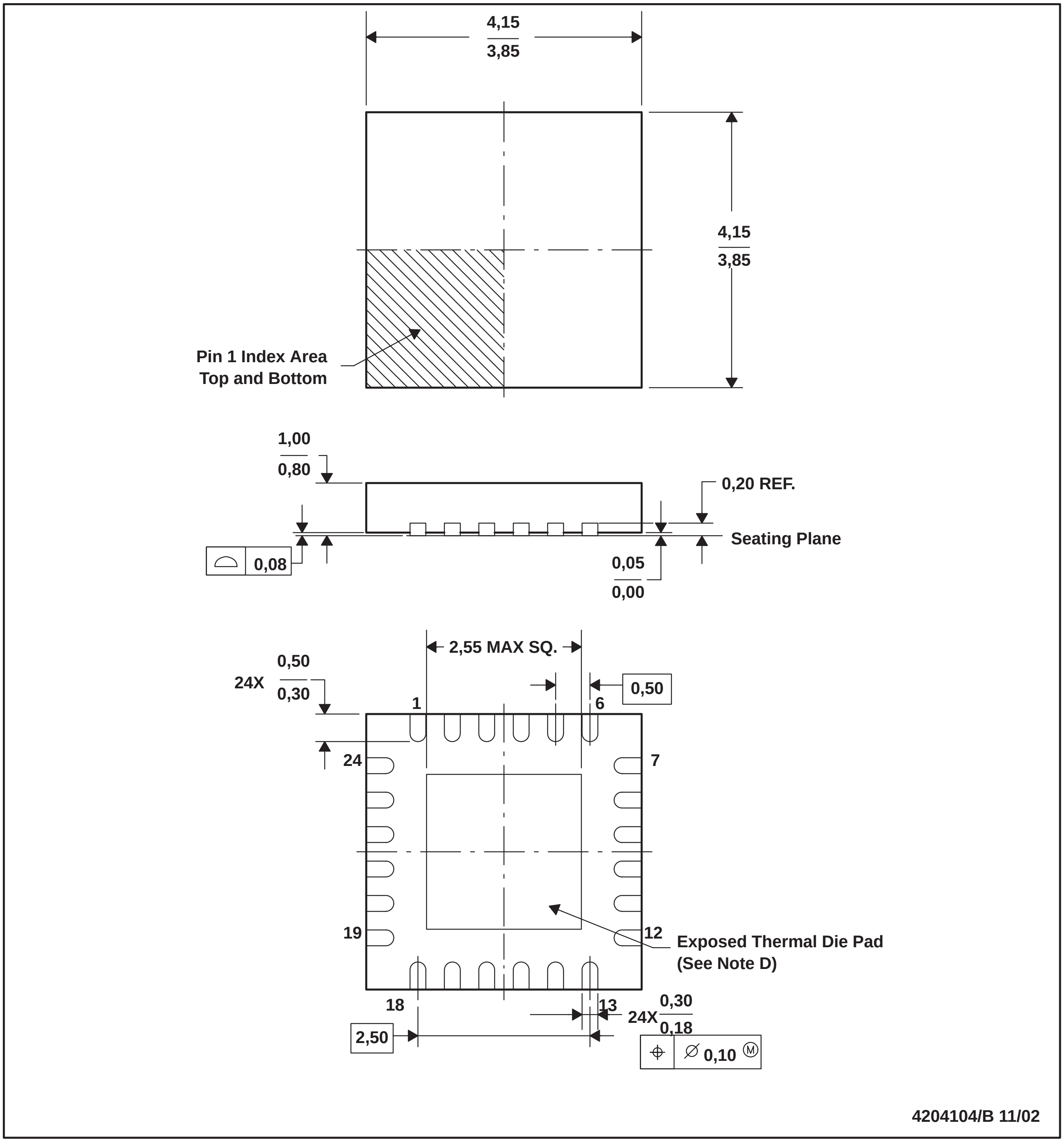
PINS ** / DIM	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins − MO-153
  14/16/20/56 Pins − MO-194

MECHANICAL DATA

RGE (S-PQFP-N24) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-leads, (QFN) package configuration.
D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.
E. Falls within JEDEC M0-220.

PRODUCT PREVIEW

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