

# DATA SHEET

**74F242**

Quad transceiver, inverting (3-State)

**74F243**

Quad transceiver (3-State)

Product specification

1990 Aug 31

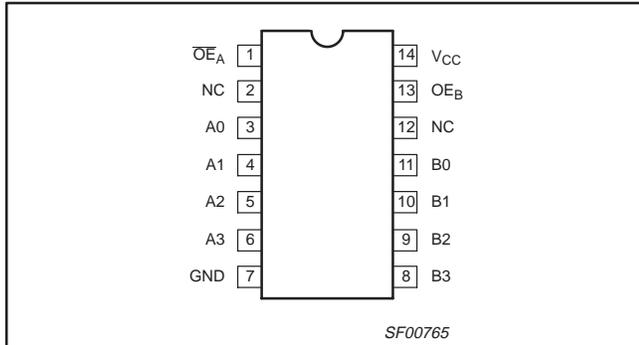
IC15 Data Handbook

# Transceivers

# 74F242/74F243

74F242 Quad Transceiver, Inverting (3-State)  
 74F243 Quad Transceiver (3-State)

### PIN CONFIGURATION



TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F242	4.3ns	31.2mA
74F243	4.0ns	66mA

### ORDERING INFORMATION

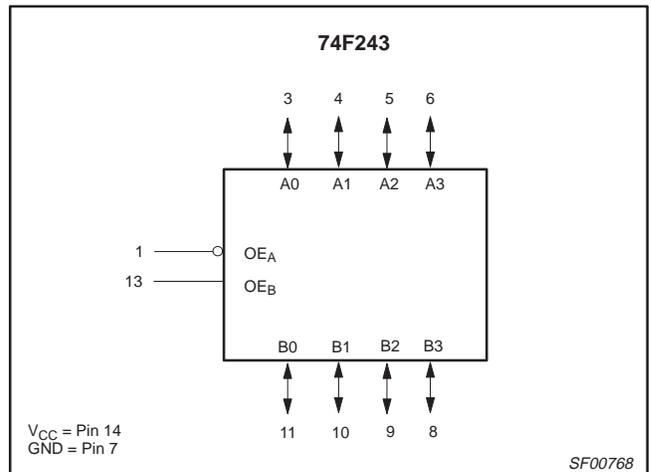
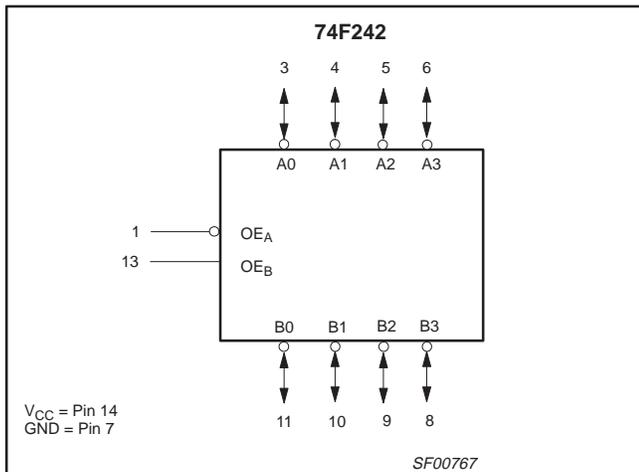
DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$ , $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$	PKG DWG #
14-pin plastic DIP	N74F242N, N74F243N	SOT27-1
14-pin plastic SO	N74F242D, N74F243D	SOT108-1

### INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
An, Bn	Data inputs (74F242)	3.5/1.67	70µA/1.0mA
An, Bn	Data inputs (74F243)	3.5/2.67	70µA/1.6mA
$\overline{OE}_A$	Output enable input (active Low)	1.0/1.67	20µA/1.0mA
$OE_B$	Output enable input	1.0/1.67	20µA/1.0mA
An, Bn	Data outputs	750/106.7	15mA/64mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

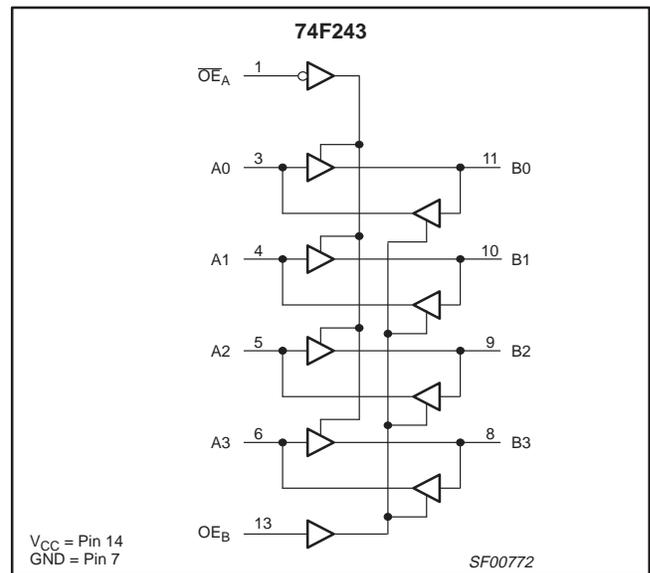
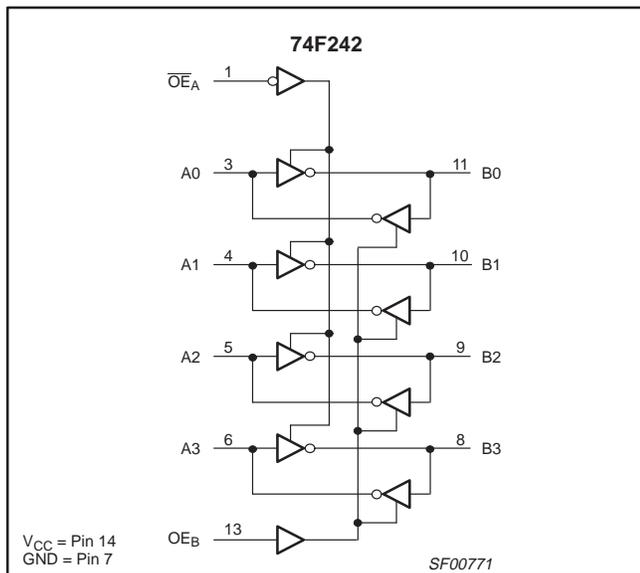
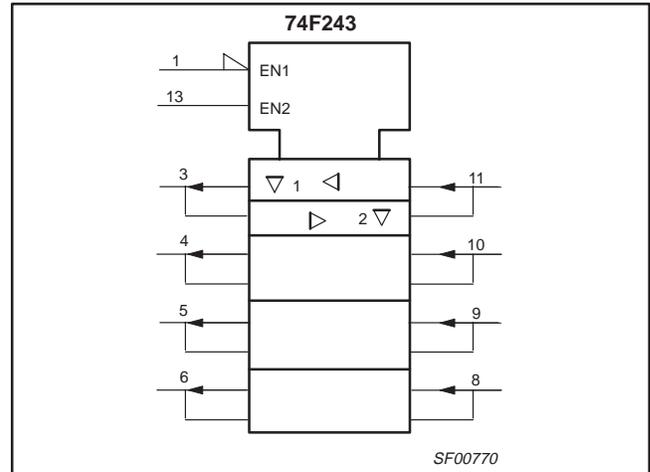
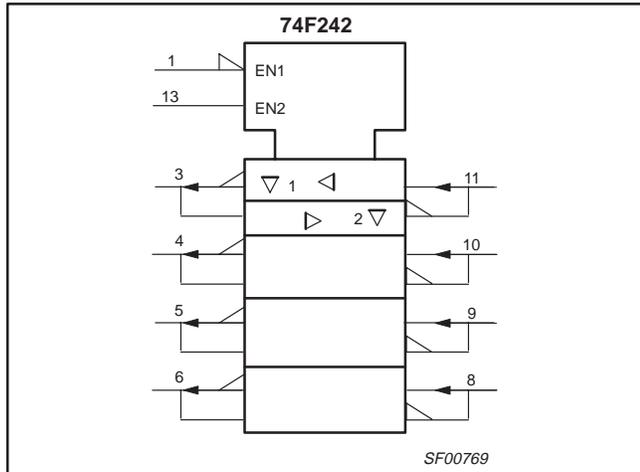
### LOGIC SYMBOLS



Transceivers

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LOGIC SYMBOLS (IEEE/IEC)



LOGIC DIAGRAMS  
FUNCTION TABLE, 74F242

INPUTS		OUTPUTS	
$\overline{OE}_A$	$OE_B$	A <sub>n</sub>	B <sub>n</sub>
L	L	INPUT	B= $\overline{A}$
H	L	Z	Z
L	H	a	a
H	H	A= $\overline{B}$	INPUT

FUNCTION TABLE, 74F243

INPUTS		OUTPUTS	
$\overline{OE}_A$	$OE_B$	A <sub>n</sub>	B <sub>n</sub>
L	L	INPUT	B=A
H	L	Z	Z
L	H	a	a
H	H	A=B	INPUT

H = High voltage level  
 L = Low voltage level  
 Z = High impedance "off" state  
 a = This condition is not allowed due to excessive currents

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**ABSOLUTE MAXIMUM RATINGS**

(Operation beyond the limits set forth in this table may impair the useful life of the device.  
Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V <sub>CC</sub>	Supply voltage	-0.5 to +7.0	V
V <sub>IN</sub>	Input voltage	-0.5 to +7.0	V
I <sub>IN</sub>	Input current	-30 to +5	mA
V <sub>OUT</sub>	Voltage applied to output in High output state	-0.5 to V <sub>CC</sub>	V
I <sub>OUT</sub>	Current applied to output in Low output state	128	mA
T <sub>amb</sub>	Operating free-air temperature range	0 to +70	°C
T <sub>stg</sub>	Storage temperature	-65 to +150	°C

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-15	mA
I <sub>OL</sub>	Low-level output current			64	mA
T <sub>amb</sub>	Operating free-air temperature range	0		70	°C

## Transceivers

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## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS <sup>1</sup>			LIMITS			UNIT	
						MIN	TYP <sup>2</sup>	MAX		
V <sub>OH</sub>	High-level output voltage		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = -3mA	±10%V <sub>CC</sub>	2.4			V	
					±5%V <sub>CC</sub>	2.7	3.3			
			V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OL</sub> = -15mA	±10%V <sub>CC</sub>	2.0	3.2		V	
					±5%V <sub>CC</sub>	2.0	3.1			
V <sub>OL</sub>	Low-level output voltage		V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = MAX	±10%V <sub>CC</sub>		0.55	V		
					±5%V <sub>CC</sub>		0.42		0.55	
V <sub>IK</sub>	Input clamp voltage		V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>				-0.73	-1.2	V	
I <sub>I</sub>	Input current at maximum input voltage		A0-A3, B0-B3	V <sub>CC</sub> = MAX, V <sub>I</sub> = 5.5V				1	mA	
			OE <sub>A</sub> , OE <sub>B</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V				100	μA	
I <sub>IH</sub>	High-level input current	OE <sub>A</sub> , OE <sub>B</sub>	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V					20	μA	
I <sub>IL</sub>	Low-level input current	only	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V					-1	mA	
I <sub>IH</sub> +I <sub>OZH</sub>	Off-state output current High-level voltage applied		V <sub>CC</sub> = MAX, V <sub>O</sub> = 2.7V					70	μA	
I <sub>IL</sub> +I <sub>OZL</sub>	Off-state output current Low-level voltage applied		74F242	V <sub>CC</sub> = MAX, V <sub>O</sub> = 0.5V				-1.0	mA	
			74F243					-1.6		
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>		V <sub>CC</sub> = MAX			-100		-225	mA	
I <sub>CC</sub>	Supply current (total)		74F242	I <sub>CCH</sub>	V <sub>CC</sub> = MAX			22	35	mA
				I <sub>CCL</sub>				40	55	mA
				I <sub>CCZ</sub>				32	45	mA
			74F243	I <sub>CCH</sub>				64	80	mA
				I <sub>CCL</sub>				64	90	mA
				I <sub>CCZ</sub>				71	90	mA

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

Transceivers

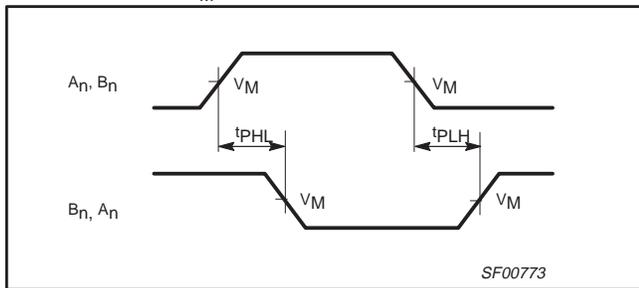
74F242/74F243

AC ELECTRICAL CHARACTERISTICS

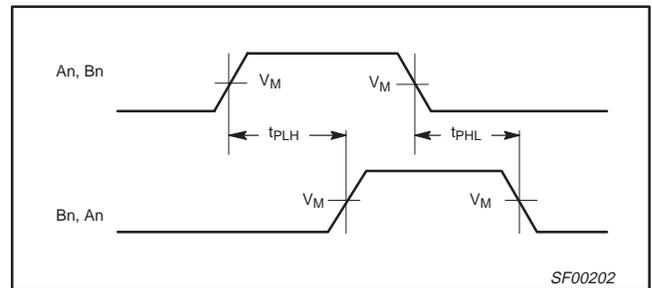
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT	
			V <sub>CC</sub> = +5V T <sub>amb</sub> = +25°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			V <sub>CC</sub> = +5V ± 10% T <sub>amb</sub> = 0°C to +70°C C <sub>L</sub> = 50pF, R <sub>L</sub> = 500Ω			
			MIN	TYP	MAX	MIN	MAX		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay An, Bn to Bn, An	74F242	Waveform NO TAG	2.5 2.0	3.5 3.0	6.0 4.5	2.5 2.0	7.0 4.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time to High or Low level		Waveform 3 Waveform 4	3.0 3.5	4.0 6.5	7.0 9.0	3.0 3.5	8.0 10.5	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time from High or Low level		Waveform 3 Waveform 4	3.5 3.5	5.5 6.0	8.5 9.5	3.5 3.5	9.0 11.0	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay An, Bn to Bn, An	74F243	Waveform 2	2.5 2.5	4.0 4.0	5.2 5.2	2.0 2.0	6.2 6.5	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable time to High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.5 5.0	5.7 7.5	2.0 2.0	6.7 8.5	
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable time from High or Low level		Waveform 3 Waveform 4	2.0 2.0	4.0 4.5	6.0 6.0	2.0 2.0	7.0 7.0	

AC WAVEFORMS

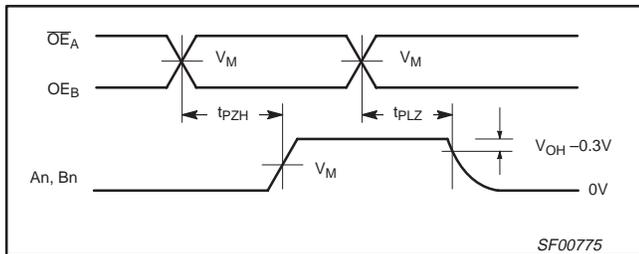
For all waveforms, V<sub>M</sub> = 1.5V.



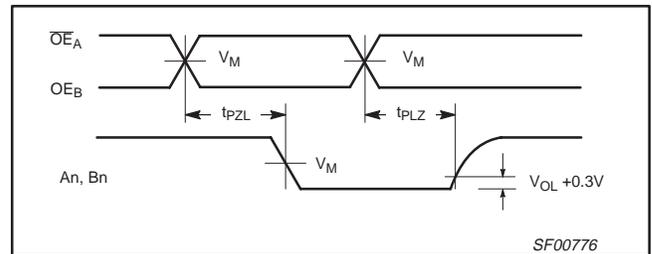
Waveform 1. For Inverting Outputs



Waveform 2. For Non-Inverting Outputs



Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

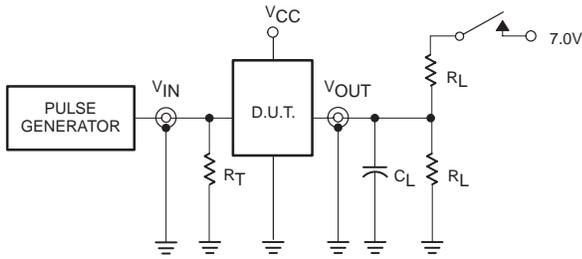


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

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TEST CIRCUIT AND WAVEFORMS



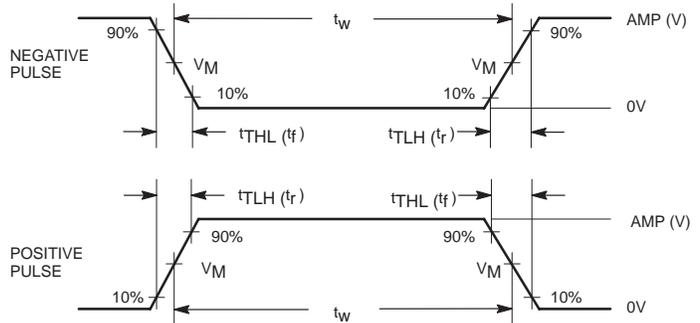
Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
$t_{PLZ}$	closed
$t_{PZL}$	closed
All other	open

DEFINITIONS:

- $R_L$  = Load resistor; see AC electrical characteristics for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.



Input Pulse Definition

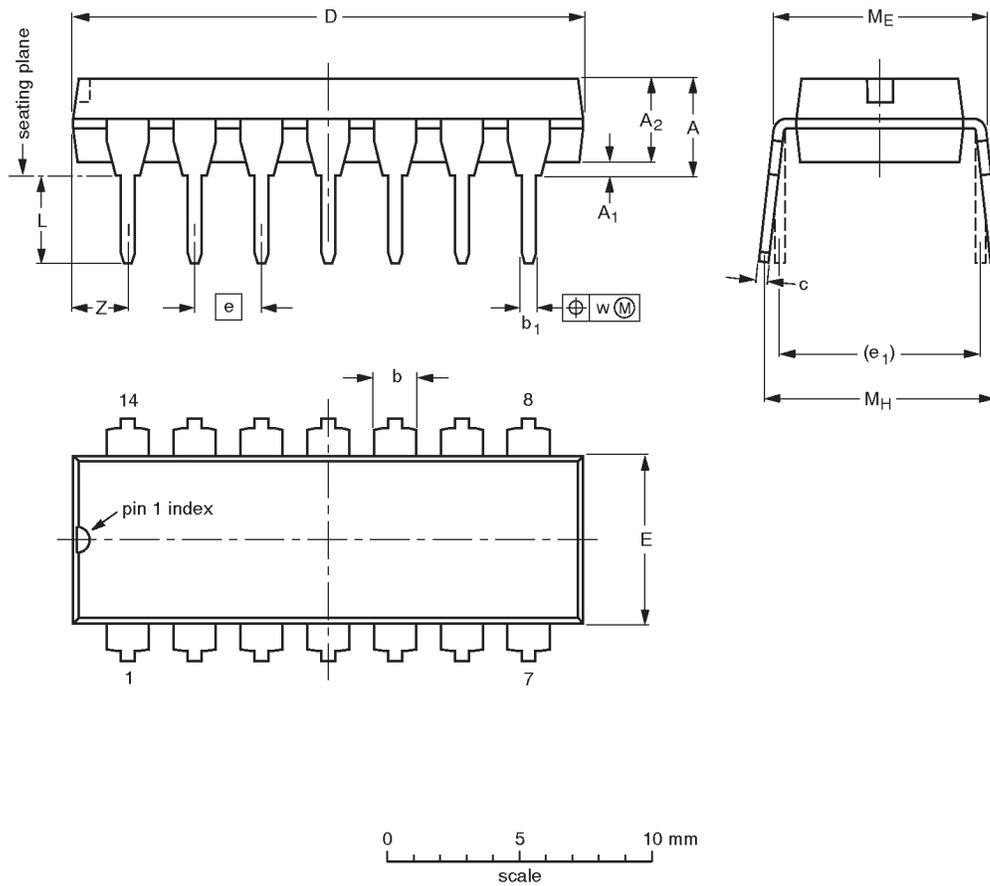
family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

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DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.020	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

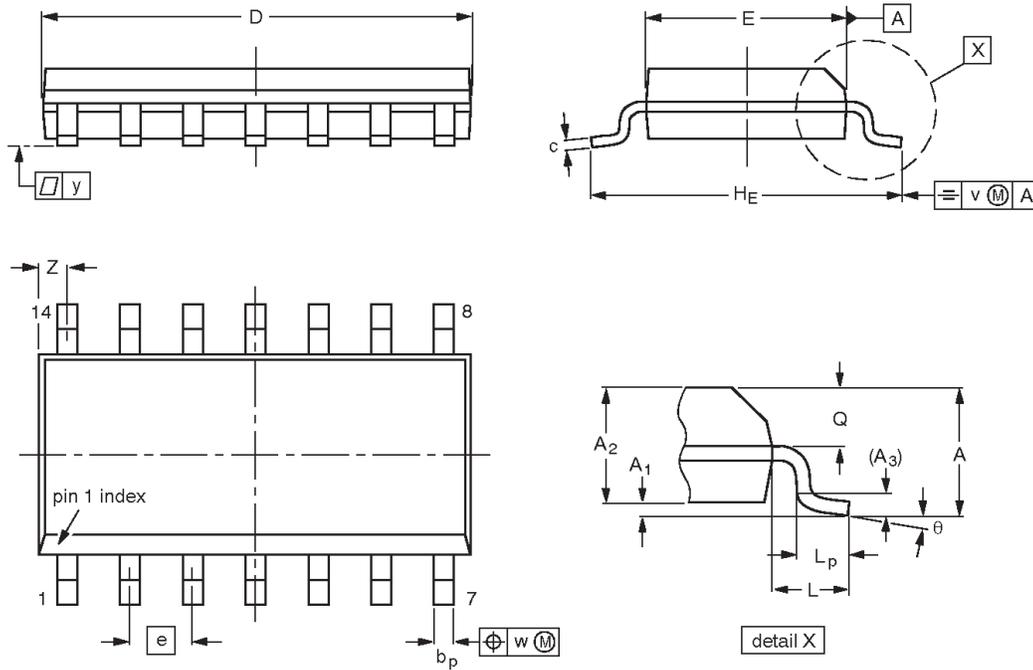
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT27-1	050G04	MO-001AA				92-11-17 95-03-11

Transceivers

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	HE	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06S	MS-012AB				95-01-23 97-05-22

## Transceivers

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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Philips Semiconductors  
811 East Arques Avenue  
P.O. Box 3409  
Sunnyvale, California 94088-3409  
Telephone 800-234-7381

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