RF MICRO·DEVICES

RF2413

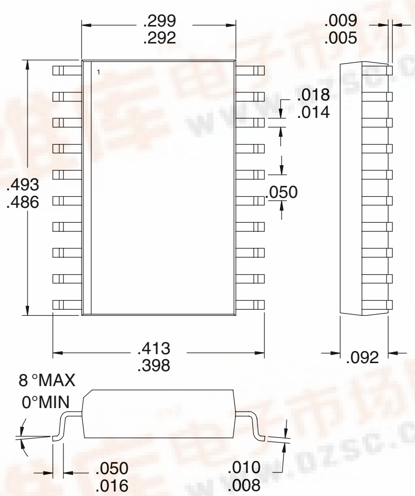
GAIN CONTROLLED DUAL-CONVERSION QUADRATURE MODULATOR

Typical Applications

- Digital and Spread Spectrum Systems
- Analog Communication Systems
- GSM Systems
- CDMA Systems
- General Purpose Frequency Conversion
- Portable Battery Powered Equipment

Product Description

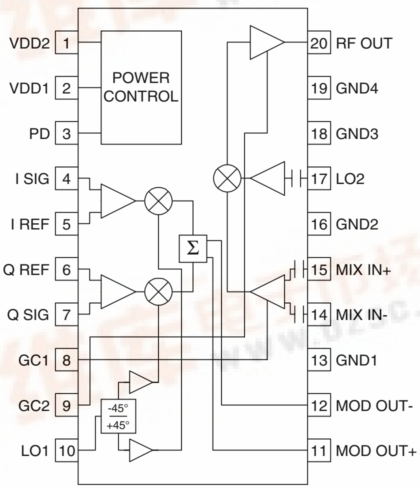
The RF2413 is a monolithic integrated transmitter universal modulation IC capable of generating modulated AM, PM, or compound carriers in the VHF/UHF frequency range. The modulation is performed at VHF, then the resulting spectrum is upconverted to a frequency range between 100MHz and 1000MHz. Up to 60dB of power control is possible through the use of two gain control pins. The IC contains all of the required components to implement the modulation function including differential amplifiers for the baseband inputs, a 90° hybrid phase splitter, limiting LO amplifiers, two balanced mixers, a combining, gain-controlled differential amplifier, a second balanced mixer, and an output gain-controlled RF amplifier which will drive a 50Ω load.



Package Style: SOP-20

Optimum Technology Matching® Applied

- ☐ Si BJT
- ☐ GaAs HBT
- ☑ GaAs MESFET
- ☐ Si Bi-CMOS
- ☐ SiGe HBT
- ☐ Si CMOS



Functional Block Diagram

Features

- Single 3V to 6.5V Power Supply
- Low Broadband Noise Floor
- Excellent Amplitude & Phase Balance
- Digitally Controlled Power Down
- 30MHz to 100MHz IF Frequency
- 200MHz to 1000MHz RF Frequency

Ordering Information

RF2413	Gain Controlled Dual-Conversion Quadrature Modulator
RF2413 PCBA	Fully Assembled Evaluation Board

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5 MODULATORS AND UPCONVERTERS

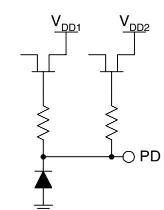
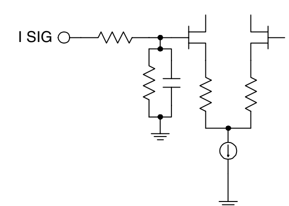
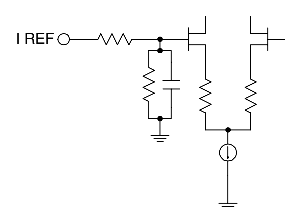
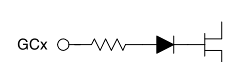
Absolute Maximum Ratings

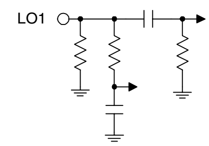
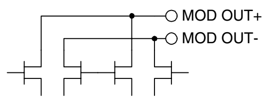
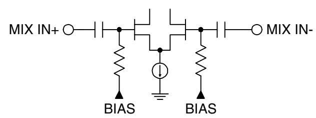
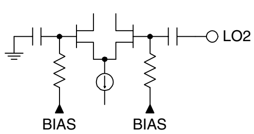
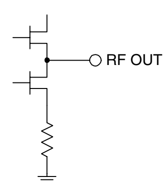
Parameter	Rating	Unit
Supply Voltage	-0.5 to 7.0	V_{DC}
Input LO and RF Levels	+6	dBm
I and Q Modulation Levels	V_{DD}	V
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

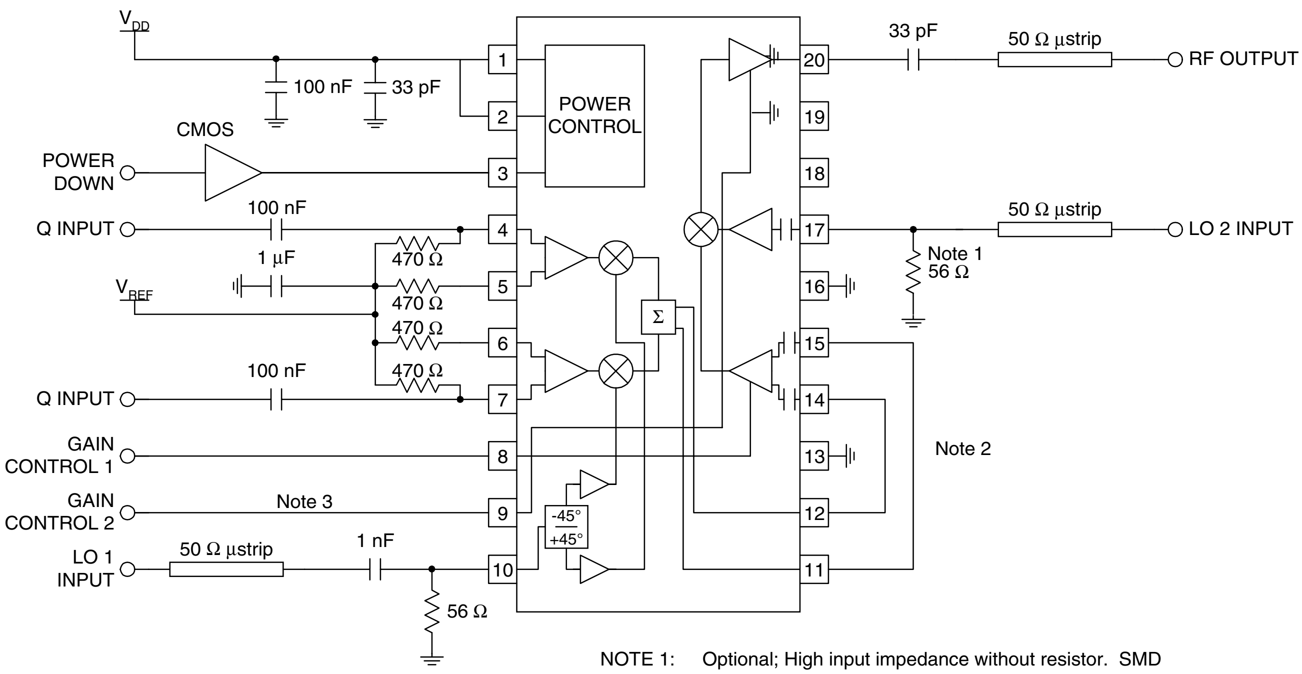
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Modulation Signals (I&Q)					T=25°C, V_{DD}=5V, V_{REF}=2.5V, BB=100kHz, LO1=70MHz, LO2=700MHz, V_{MOD}=3.0V_{PP} SSB, unless indicated otherwise.
Frequency Range		DC to 25		MHz	
Signal Level		3.0		V_{PP}	For 1dB compression
Reference Voltage (V_{REF})		2.0 to 3.0		V	
Input Impedance		3		kΩ	
Amplitude Balance		0.1		dB	
Quadrature Phase Error		1		°	
First LO Input					
Frequency Range		30 to 200		MHz	For 30dB sideband suppression
		30 to 250		MHz	For 20dB sideband suppression
Power Level		-5 to +6		dBm	
Input Impedance		750-j500		Ω	At 100MHz, without external 50Ω termination
IF Inputs & Outputs (MOD OUT & MIX IN)					
Output Impedance		290-j160		Ω	At 100MHz
		170-j180		Ω	At 200MHz
Input Impedance		6000-j2500		Ω	At 100MHz
		5200-j2800		Ω	At 200MHz
Second LO Input					
Frequency Range		100 to 1000		MHz	
Power Level		0 to +6		dBm	
Input Impedance		2000-j3000		Ω	At 300MHz, without external 50Ω termination
		600-j1400		Ω	At 1000MHz, without external 50Ω termination
RF Output					
Output Power					V_{DD}=6V, LO1,2 power=0dBm, SSB
		+6		dBm	Freq=200MHz to 500MHz
	-2	+2	+5	dBm	Freq=500MHz to 800MHz
		-1		dBm	Freq=800MHz to 1000MHz
Total Gain Control Range		75		dB	Gain 1 and Gain 2
Gain Control Voltage for minimum gain		1.5		V	
Gain Control Voltage for maximum gain		5.0		V	
Nominal Output Impedance		50		Ω	
Output VSWR		1.5:1			Freq<600MHz
		3:1			600MHz<Freq<1000MHz
Output Broadband Noise Power		-155		dBm/Hz	

Spurious					Single sideband modulation
Sideband Suppression	30	35		dBc	Unadjusted.
Carrier Suppression	20	25		dBc	Unadjusted. Modulation DC offset may be externally adjusted for maximum suppression. Suppression is then typically 40dBc.
First LO Harmonics		20		dBc	Odd unfiltered IF
		30		dBc	Even unfiltered IF
Power Down					
Turn On/Off Time		<100		ns	
PD Input Resistance		>50		kΩ	
Power Down "ON"		V_{CC}		V	Threshold voltage
Power Down "OFF"		0		V	Threshold voltage
Power Supply					
Voltage		5		V	Specifications
		3 to 6.5		V	Operating limits
Current Consumption		35	50	mA	

Pin	Function	Description	Interface Schematic
1	VDD2	Supply Voltage for the RF Output Stage only. A 33pF external bypass capacitor is required and an optional 0.1µF will be required if no other low frequency bypass capacitors are nearby. The trace length between the pin and the bypass capacitors should be minimized. The ground side of the bypass capacitors should connect immediately to ground plane. Though the part is designed to run from a 5V supply, it will work at 3V. Gain and available output power will be reduced by 5 to 10dB. This also means that the part is sensitive to unintended power supply variation. Power supply voltage should be kept constant, or another way of maintaining constant output power is required.	
2	VDD1	Supply Voltage for all circuits except the RF Output Stage. The same comments as for VDD2 apply to this pin.	
3	PD	Power Down control. When this pin is 0V all circuits are turned off, and when this pin is VDD all circuits are operating. This is a high impedance input, internally connected to the gates of a few FETs. To minimize current consumption in power down mode, this pin should be as close to 0V as possible. Turn-on voltage of some parts of the circuit may be as low as 0.1V. In order to maximize output power this pin should be as close to VDD as possible during normal operation.	
4	I SIG	Baseband input to the I mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. The DC level supplied to this pin should be VDD2/2. Input impedance of this pin is about 3kΩ.	
5	I REF	Reference voltage for the I mixer. This voltage should be the same as the DC voltage supplied to the I SIG pin. To obtain a carrier suppression of better than 25dB it may be tuned ±0.15V (relative to the I SIG DC voltage). Without tuning it will typically be better than 25dB. Input impedance of this pin is about 3kΩ.	
6	Q REF	Reference voltage for the Q mixer. This voltage should be the same as the DC voltage supplied to the Q SIG pin. To obtain a carrier suppression of better than 25dB it may be tuned ±0.15V (relative to the Q SIG DC voltage). Without tuning, the carrier suppression will typically be better than 25dB. The input impedance of this pin is about 3 kΩ.	Same as pin 5.
7	Q SIG	Baseband input to the Q mixer. This pin is DC coupled. Maximum output power is obtained when the input signal has a peak to peak amplitude of 5V. The DC level supplied to this pin should be VDD2/2. Input impedance of this pin is about 3kΩ.	Same as pin 4.
8	GC1	Gain control of the IF input amplifier. This pin, when used as the only gain control, will give a 30dB control range. When used together with GC2, a 60dB range is available. When this pin is at 1.8V or lower, the gain is set to the minimum; when this pin is at 3.8V or above, the gain is set to the maximum; see the plot below for typical characteristics. If fixed maximum output level is required, it is recommended to connect this pin to VDD. There are no provisions in the chip for limiting the bandwidth of the gain control, so very fast response times are available. If a slower response is desired, an external capacitor can be added.	
9	GC2	Gain control for the RF output amplifier. This pin has the same control characteristics as GC1.	Same as pin 8.

10	**LO1**	High impedance modulator LO input. A shunt 56Ω resistor can be used for matching. This pin is NOT internally DC blocked. An external blocking capacitor must be provided if the pin is connected to a device with DC present. A DC path to ground (i.e. an inductor or resistor to ground) is, however, acceptable at this pin. If a blocking capacitor is required, a value of 1nF is recommended.	
11	**MOD OUT+**	Balanced IF output port. If no filtering is required this pin can be connected directly to the MIX IN+ pin. This pin is NOT DC blocked and carries DC. A blocking capacitor of 1nF is needed when this pin is connected to a DC path. An appropriate matching network may be needed if an IF filter is used.	
12	**MOD OUT-**	Same as pin 11, except complementary output.	See pin 11.
13	**GND1**	Ground connection for all baseband circuits, modulator and the IF buffer amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
14	**MIX IN-**	High impedance balanced input to the gain controlled IF stage. This pin has an internal DC blocking capacitor. If no IF filter is needed, this pin may be connected directly to MOD OUT-. If an IF filter is used, an external shunt resistor to ground may be needed to provide correct matching for the filter.	
15	**MIX IN+**	Same as pin 14, except complementary input.	See pin 14.
16	**GND2**	Ground connection for the limiting LO2 buffer amplifier. Keep traces physically short and connect immediately to ground plane for best performance.	
17	**LO2**	Mixer LO Input port. A shunt 56Ω resistor can be used for matching. This pin has internal DC blocking,	
18	**GND3**	Ground connection for the IF mixer and the RF gain control stage. Keep traces physically short and connect immediately to ground plane for best performance.	
19	**GND4**	Ground connection for the RF output stage. Keep traces physically short and connect immediately to ground plane for best performance.	
20	**RF OUT**	50Ω output. This pin is not internally DC blocked, and an external blocking capacitor of 100pF is required.	

Application Schematic



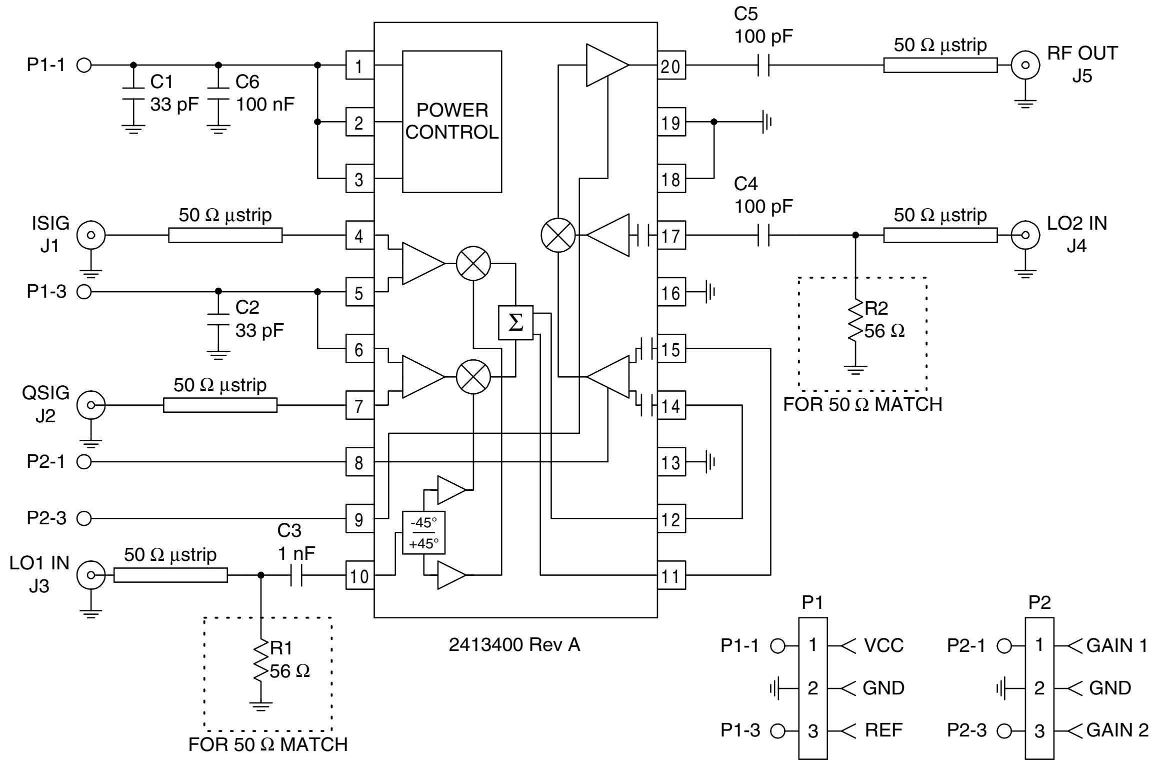
NOTE 1: Optional; High input impedance without resistor. SMD resistor mounted adjacent to package pin, grounded through via to the ground plane.

NOTE 2: If no IF filter is needed, tie pins 11, 12, 14, and 15 as shown. Otherwise insert the filter and the matching network.

NOTE 3: Gain control pins (8 and 9) may be tied together directly.

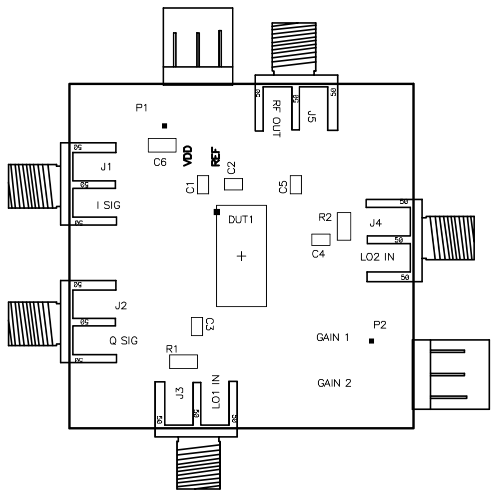
Evaluation Board Schematic

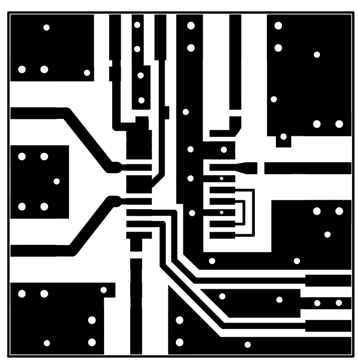
(Download Bill of Materials from www.rfmd.com.)

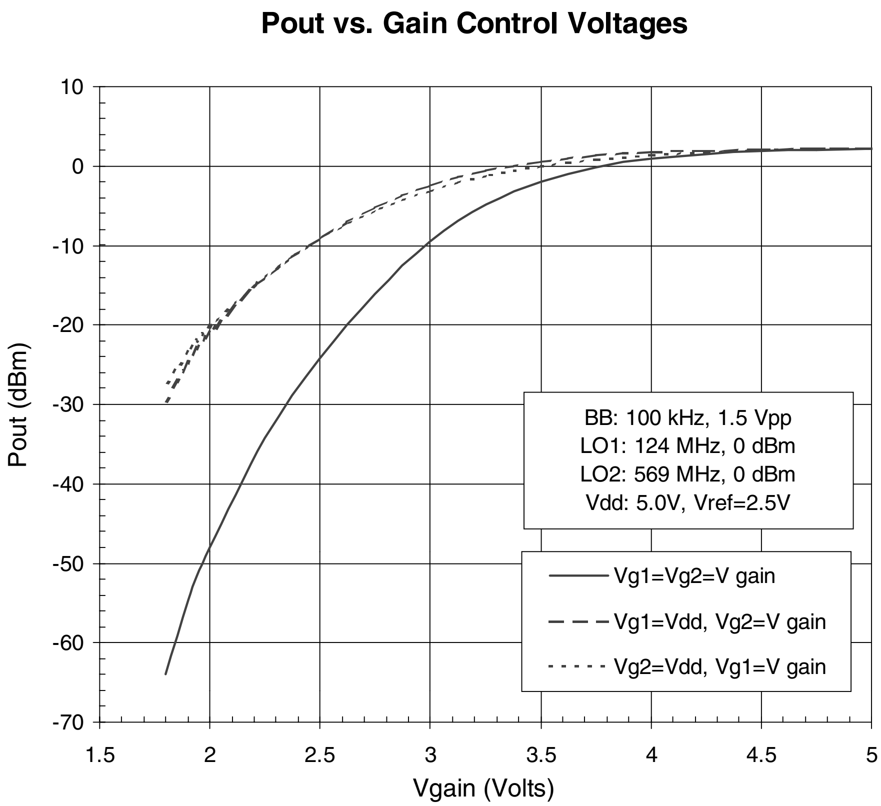


Evaluation Board Layout
1.52” x 1.52”

Board Size 0.039”; Board Material FR-4; Multi-Layer







Pout vs. Gain Control Voltages
10
0
-10
-20
-30
-40
-50
-60
-70
Pout (dBm)
1.5
2
2.5
3
3.5
4
4.5
5
Vgain (Volts)
BB: 100 kHz, 1.5 Vpp
LO1: 124 MHz, 0 dBm
LO2: 569 MHz, 0 dBm
Vdd: 5.0V, Vref=2.5V
Vg1=Vg2=V gain
Vg1=Vdd, Vg2=V gain
Vg2=Vdd, Vg1=V gain