National Semiconductor

May 1995

54F/74F540 • 54F/74F541
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'F540 and 'F541 are similar in function to the 'F240 and 'F244 respectively, except that the inputs and outputs are on opposite sides of the package (see Connection Diagrams). This pinout arrangement makes these devices especially useful as output ports for microprocessors, allowing ease of layout and greater PC board density.

Features

- TRI-STATE outputs drive bus lines
- Inputs and outputs opposite side of package, allowing easier interface to microprocessors

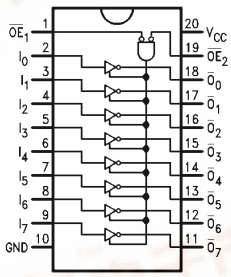
Commercial	Military	Package Number	Package Description
74F540PC		N20A	20-Lead (0.300″ Wide) Molded Dual-In-Line
	54F540DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F540SC (Note 1)		M20B	20-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74F540SJ (Note 1)		M20D	20-Lead (0.300″ Wide) Molded Small Outline, EIAJ
	54F540FM (Note 2)	W20A	20-Lead Cerpack
	54F540LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C
74F541PC		N20A	20-Lead (0.300″ Wide) Molded Dual-In-Line
	54F541DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F541SC (Note 1)		M20B	20-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74F541SJ (Note 1)		M20D	20-Lead (0.300″ Wide) Molded Small Outline, EIAJ
	54F541FM (Note 2)	W20A	20-Lead Cerpack
	54F541LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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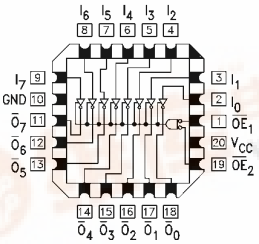
Pin Assignment for LCC



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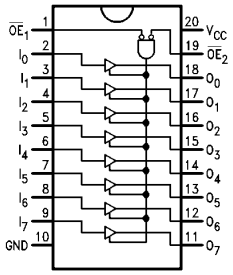
RRD-B30M75/Printed in U. S. A.

Connection Diagrams (Continued)

'F541



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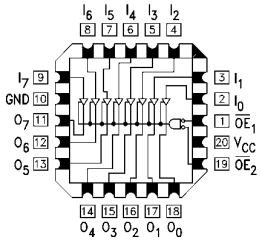

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Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{OE}_1$, $\overline{OE}_2$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μA/ −0.6 mA
I_n	Inputs	1.0/1.0	20 μA/ −0.6 mA
O_n, $\overline{O}_n$	Outputs	600/106.6 (80)	−12 mA/64 mA (48 mA)

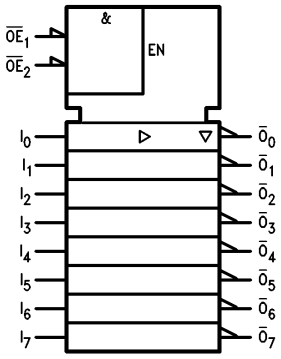
Truth Table

Inputs			Outputs	
$\overline{OE}_1$	$\overline{OE}_2$	I	'F540	'F541
L	L	H	L	H
H	X	X	Z	Z
X	H	X	Z	Z
L	L	L	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagrams

IEEE/IEC
'F540



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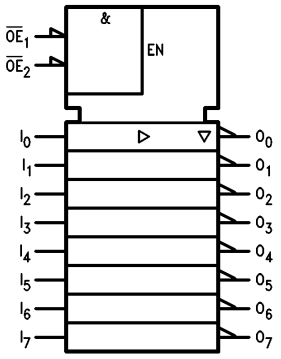
IEEE/IEC
'F541



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.4			V	Min	I_{OH} = −3 mA
		54F 10% V_{CC}	2.0					I_{OH} = −12 mA
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 10% V_{CC}	2.0					I_{OH} = −15 mA
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.55	V	Min	I_{OL} = 48 mA
		74F 10% V_{CC}			0.55			I_{OL} = 64 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−100		−225	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V

DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F			Units	V_{CC}	Conditions
		Min	Typ	Max			
I_{CCH}	Power Supply Current ('F540)		11	20	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current ('F540)		53	75	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current ('F540)		31	45	mA	Max	V_O = HIGH Z
I_{CCH}	Power Supply Current ('F541)		26	35	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current ('F541)		55	75	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current ('F541)		31	55	mA	Max	V_O = HIGH Z

AC Electrical Characteristics

Symbol	Parameter	74F			54F		74F		Units
		T_A = +25°C, V_{CC} = +5.0V, C_L = 50 pF			T_A, V_{CC} = Mil, C_L = 50 pF		T_A, V_{CC} = Com, C_L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay	1.5	3.0	5.0	1.0	6.0	1.0	5.5	ns
t_{PHL}	Data to Output ('F540)	1.0	2.0	4.0	1.0	4.5	1.0	4.0	
t_{PZH}	Output Enable Time ('F540)	2.5	4.9	8.0	2.5	9.0	2.5	8.5	ns
t_{PZL}		3.5	5.8	10.0	3.5	11.0	3.5	10.5	
t_{PHZ}	Output Disable Time ('F540)	1.5	3.4	6.0	1.5	7.0	1.5	6.5	
t_{PLZ}		1.0	2.5	5.5	1.0	7.5	1.0	6.0	
t_{PLH}	Propagation Delay	1.5	3.3	5.5			1.5	6.0	ns
t_{PHL}	Data to Output ('F541)	1.5	2.7	5.5			1.5	6.0	
t_{PZH}	Output Enable Time ('F541)	3.0	5.8	8.0			2.5	9.5	ns
t_{PZL}		3.5	6.1	8.5			3.0	9.5	
t_{PHZ}	Output Disable Time ('F541)	1.5	3.4	6.0			1.5	6.5	
t_{PLZ}		1.5	2.9	5.5			1.5	6.0	

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74F 540/541 S C X

Temperature Range Family
74F = Commercial
54F = Military

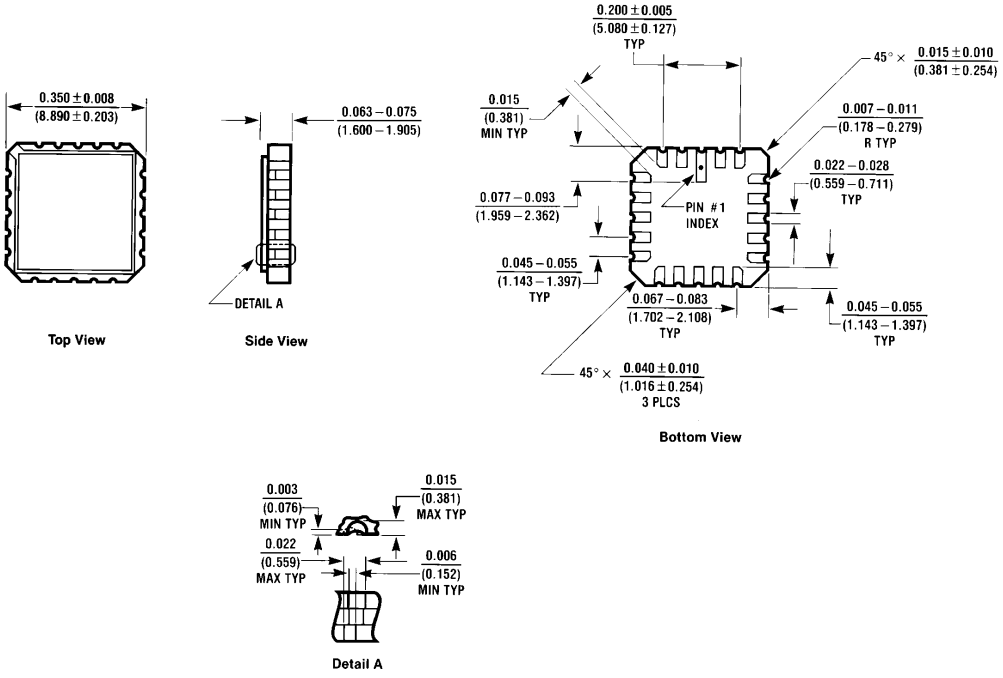
Device Type

Package Code
P = Plastic DIP
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier (LCC)
S = Small Outline SOIC JEDEC
SJ = Small Outline SOIC EIAJ

Temperature Range
C = Commercial (0°C to +70°C)
M = Military (−55°C to +125°C)

Special Variations
QB = Military grade device with environmental and burn-in processing
X = Devices shipped in 13″ reel

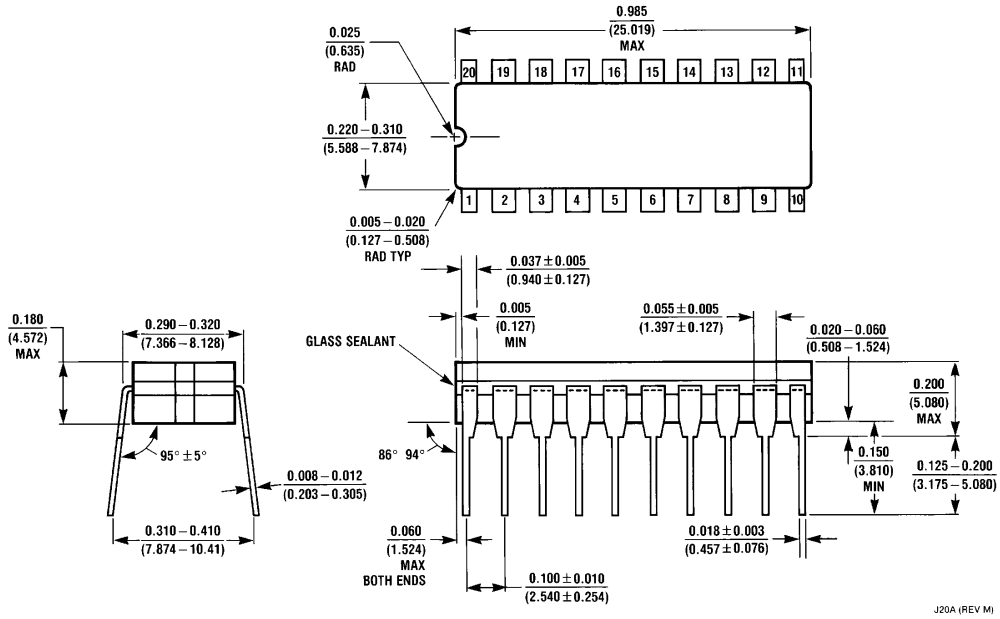
Physical Dimensions inches (millimeters)



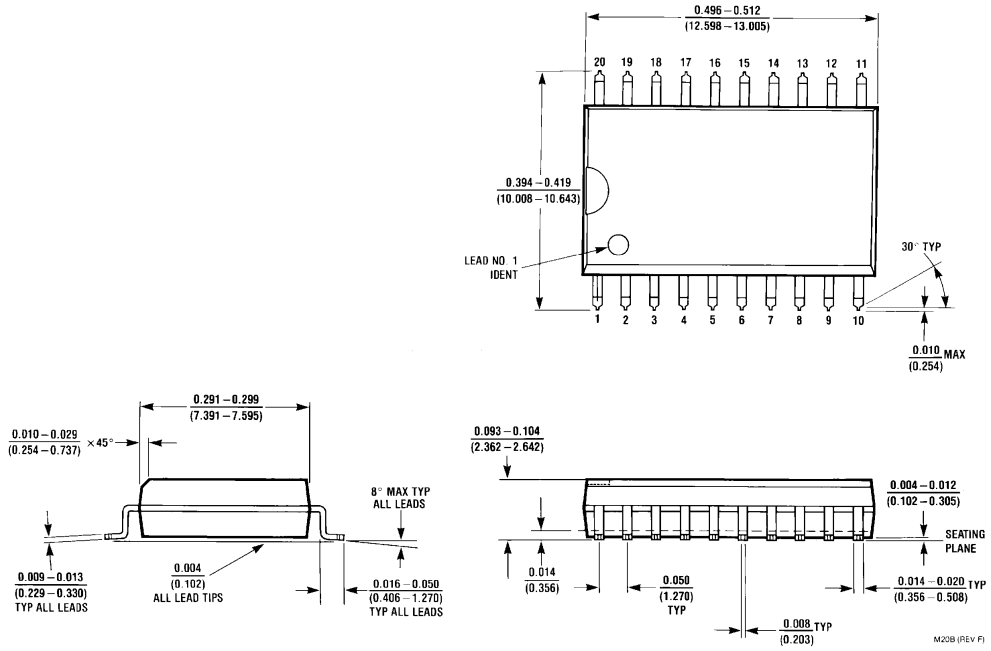
E20A (REV D)

20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

Physical Dimensions inches (millimeters) (Continued)

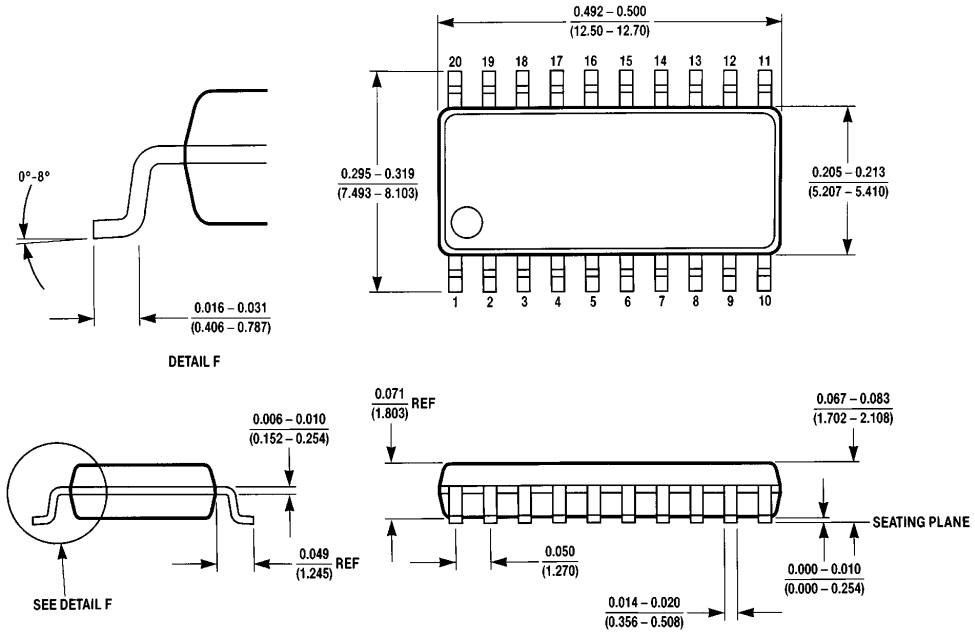


20-Lead Ceramic Dual-In-Lead Package (D)
NS Package Number J20A

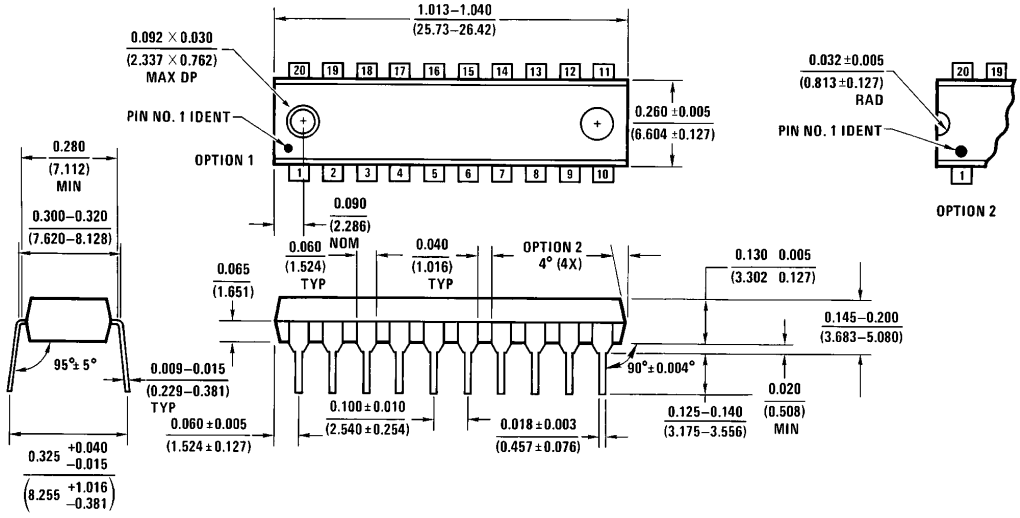


20-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)

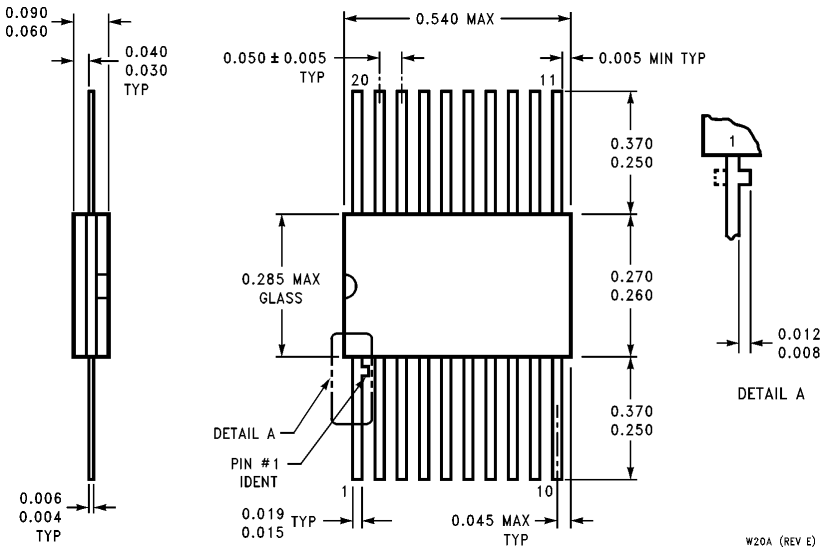


20-Lead (0.300″ Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M20D



20-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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