



November 1990

54F/74F579 8-Bit Bidirectional Binary Counter with TRI-STATE® Outputs

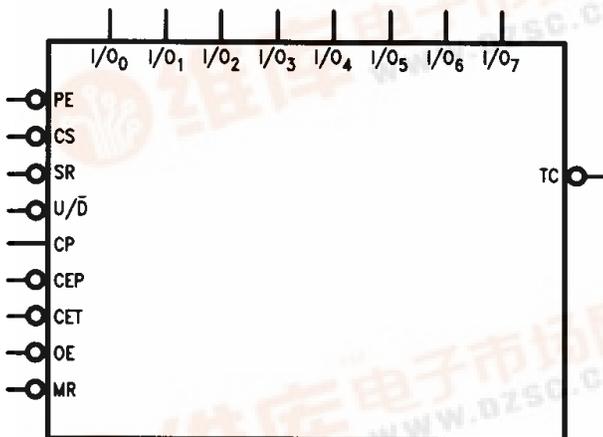
General Description

The 'F579 is a fully synchronous 8-stage up/down counter with multiplexed TRI-STATE I/O ports for bus-oriented applications. It features a preset capability for programmable operation, carry lookahead for easy cascading and a U/\bar{D} input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

Features

- Multiplexed TRI-STATE I/O ports
- Built-in lookahead carry capability
- Count frequency 100 MHz typical
- Supply current 75 mA typical
- Guaranteed 4000V minimum ESD protection

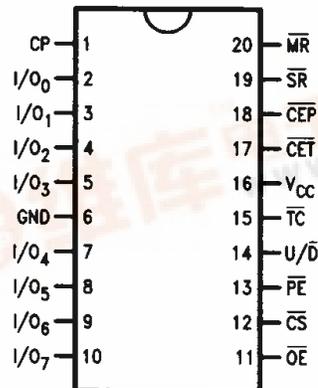
Logic Symbol



TL/F/9568-1

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak

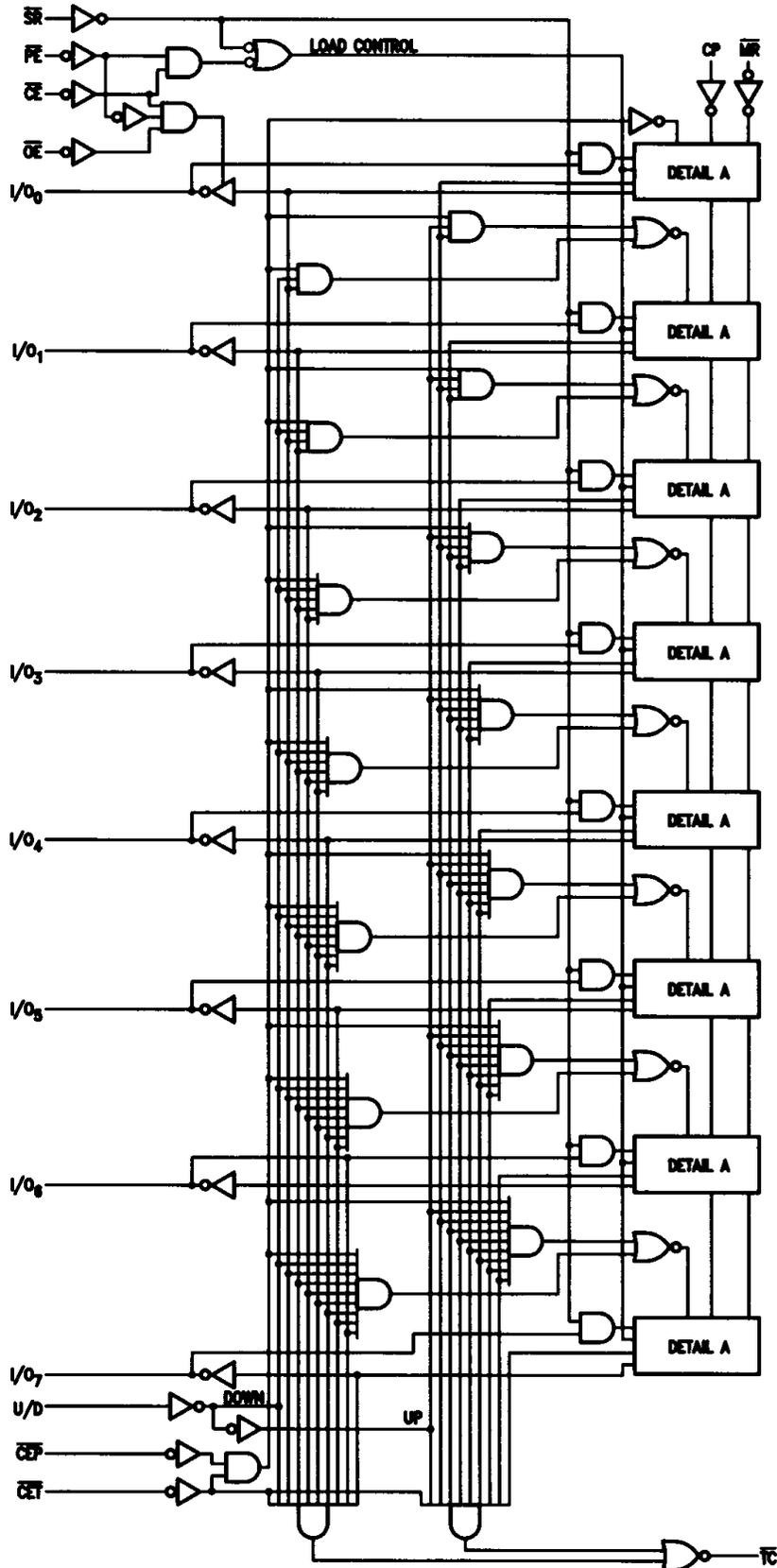


TL/F/9568-2

54F/74F579 8-Bit Bidirectional Binary Counter with TRI-STATE Outputs



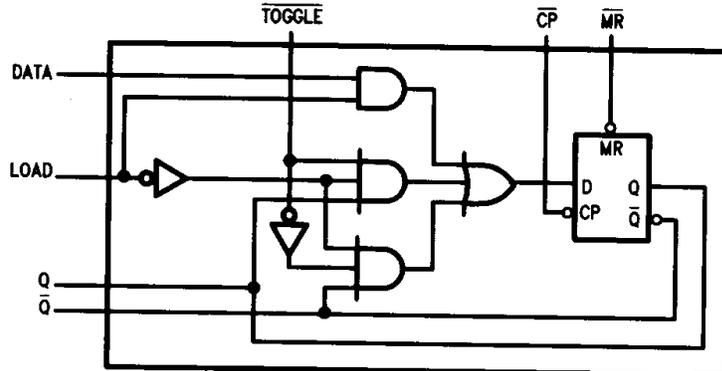
Logic Diagram



TL/F/9568-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Logic Diagram (Continued)



V_{CC} = Pin 16
 GND = Pin 6
 () = Pin Numbers

Detail A

TL/F/9568-6

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
I/O ₀ -I/O ₇	Data Inputs or TRI-STATE Outputs	3.5/0.333 75/15 (12.5)	70 μA/-0.2 mA -3 mA/24 mA (20 mA)
PE	Parallel Enable Input (Active LOW)	0.25/0.333	5 μA/-0.2 mA
U/D	Up-Down Count Control Input	0.25/0.333	5 μA/-0.2 mA
MR	Master Reset Input (Active LOW)	0.25/0.333	5 μA/-0.2 mA
SR	Synchronous Reset Input (Active LOW)	0.25/0.333	5 μA/-0.2 mA
CEP	Count Enable Parallel Input (Active LOW)	0.25/0.333	5 μA/-0.2 mA
CET	Count Enable Trickle Input (Active LOW)	0.25/0.333	5 μA/-0.2 mA
CS	Chip Select Input Active (Active LOW)	0.25/0.333	5 μA/-0.2 mA
OE	Output Enable Input (Active LOW)	0.25/0.333	5 μA/-0.2 mA
CP	Clock Pulse Input (Active Rising Edge)	0.25/0.333	5 μA/-0.2 mA
TC	Terminal Count Output (Active LOW)	25/12.5	-1 mA/5 mA

Function Table

MR	SR	CS	PE	CEP	CET	U/D	OE	CP	Function
X	X	H	X	X	X	X	X	X	I/O _a to I/O _h in High Z (\overline{PE} Disabled)
X	X	L	H	X	X	X	H	X	I/O _a to I/O _h in High Z
X	X	L	H	X	X	X	L	X	Flip-Flop Outputs Appear on I/O Lines
L	X	X	X	X	X	X	X	X	Asynchronous Reset for all Flip-Flops
H	L	X	X	X	X	X	X	—	Synchronous Reset for all Flip-Flops
H	H	L	L	X	X	X	X	—	Parallel Load all Flip-Flops
H	H	(Not LL)		H	X	X	X	—	Hold
H	H	(Not LL)		X	H	X	X	—	Hold (\overline{TC} Held HIGH)
H	H	(Not LL)		L	L	H	X	—	Count Up
H	H	(Not LL)		L	L	L	X	—	Count Down

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

— = LOW to HIGH Clock Transition

Not LL = \overline{CS} and \overline{PE} should never both be LOW voltage level at the same time.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	Mil 10% V _{CC} 5% V _{CC}	2.4 2.4 2.7		V	Min	I _{OH} = -3 mA
V _{OL}	Output LOW Voltage	Mil 10% V _{CC} 5% V _{CC}		0.5 0.5 0.5	V	Min	I _{OL} = 24 mA (TC, I/O _n) I _{OL} = 20 mA (TC), I _{OL} = 24 mA (I/O _n) I _{OL} = 20 mA (TC), I _{OL} = 24 mA (I/O _n)
I _{IH}	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V _{IN} = 2.7V (Non-I/O Pins)
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V _{IN} = 7.0V (Non-I/O Pins)
I _{BVIT}	Input HIGH Current Breakdown (I/O)	54F 74F		1.0 0.5	mA	Max	V _{IN} = 5.5V (I/O _n)
I _{CEX}	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Control	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{ZZ}	Bus Drainage Test			500	μA	0.0	V _{OUT} = 5.25V
I _{IL}	Input LOW Current			-0.2	mA	Max	V _{IN} = 0.5V (Non-I/O Pins)
I _{IH} & I _{OZH}	Output Leakage Current			70	μA	Max	V _{OUT} = 2.7V (I/O _n)
I _{IL} & I _{OZL}	Output Leakage Current			-200	μA	Max	V _{OUT} = 0.5V (I/O _n)
I _{OS}	Output Short-Circuit Current		-60	-150	mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current		70	110	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		85	120	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		85	125	mA	Max	V _O = HIGH Z

AC Electrical Characteristics

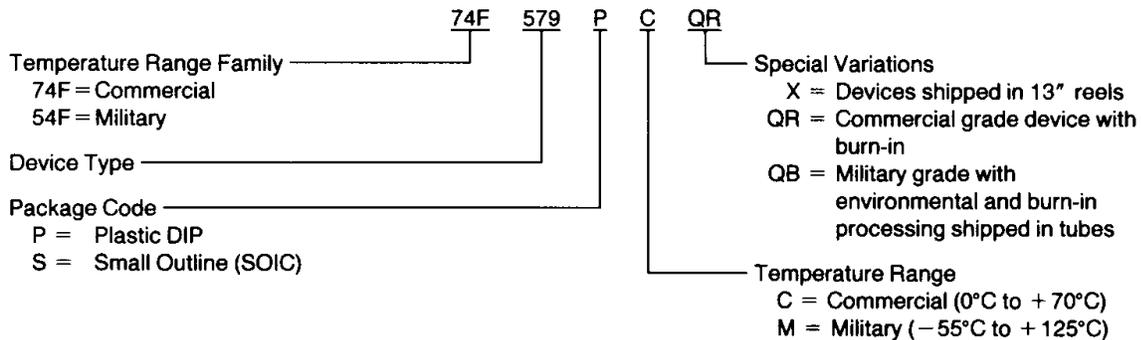
Symbol	Parameter	74F			54F		74F		Units
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Comm C _L = 50 pF		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	90	105			80			
t _{PLH} t _{PHL}	Propagation Delay CP to I/O _n	3.0 5.0	5.0 8.0	7.5 11.5		3.0 5.0	8.0 11.5	ns	
t _{PLH} t _{PHL}	Propagation Delay CP to TC	5.0 5.0	7.5 9.0	11.5 11.5		5.0 5.0	12.0 12.0	ns	
t _{PLH} t _{PHL}	Propagation Delay U/D to TC	4.5 4.5	7.0 8.0	9.0 9.5		4.5 4.5	10.0 10.0	ns	
t _{PLH} t _{PHL}	Propagation Delay CEP or CET to TC	2.5 3.5	3.8 6.0	6.0 8.0		2.5 3.5	6.5 8.5	ns	
t _{PHL}	Propagation Delay MR to I/O _n	5.0	7.5	10.0		5.0	10.0	ns	
t _{PHL}	Propagation Delay MR to TC	6.5	10.0	13.0		6.5	13.5	ns	
t _{PZH} t _{PZL}	Output Enable Time CS or PE to I/O	3.0 5.5	5.0 8.0	8.5 10.5		3.0 5.5	9.0 11.5	ns	
t _{PHZ} t _{PLZ}	Output Disable Time CS or PE to I/O	2.0 2.0	5.0 4.5	8.5 8.0		2.0 2.0	9.0 8.5	ns	
t _{PZH} t _{PZL}	Output Enable Time OE to I/O _n	3.0 5.0	5.0 8.0	8.0 11.0		3.0 5.0	8.5 12.0	ns	
t _{PHZ} t _{PLZ}	Output Disable Time OE to I/O _n	2.0 2.0	4.0 4.0	6.5 6.0		2.0 2.0	6.5 6.5	ns	

AC Operating Requirements

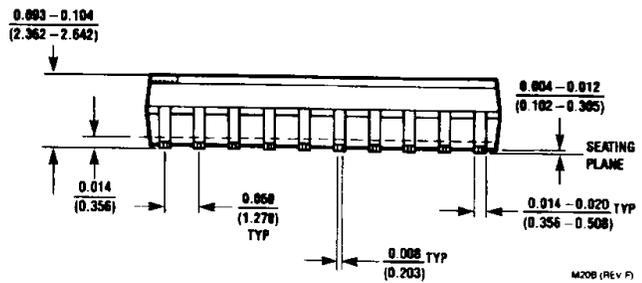
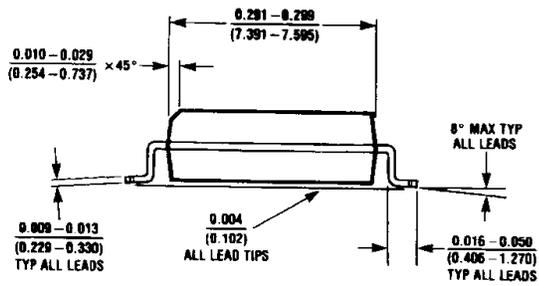
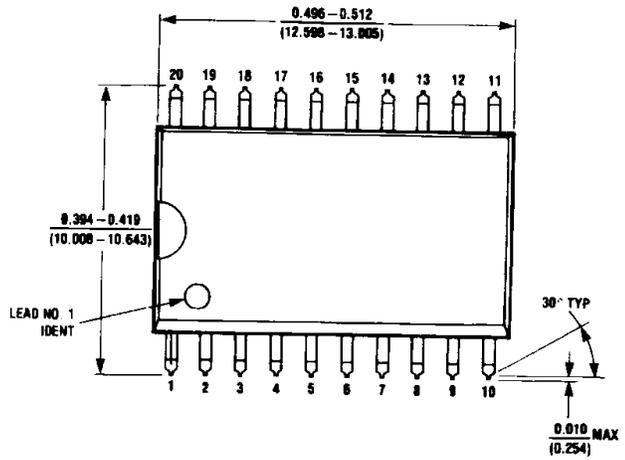
Symbol	Parameter	74F			54F		74F	
		T _A = +25°C V _{CC} = +5.0V			T _A , V _{CC} = Mil		T _A , V _{CC} = Comm	
		Min	Typ	Max	Min	Max	Min	Max
t _s (H)	Setup Time	4.0					4.0	
t _s (L)	I/O _n to CP	4.0					4.0	
t _h (H)	Hold Time	0.0					0.0	
t _h (L)	I/O _n to CP	0.0					0.0	
t _s (H)	Setup Time	9.5					9.5	
t _s (L)	\overline{PE} , \overline{CS} or \overline{SR} to CP	9.5					9.5	
t _h (H)	Hold Time	0.0					0.0	
t _h (L)	\overline{PE} , \overline{CS} or \overline{SR} to CP	0.0					0.0	
t _s (H)	Setup Time	6.5					6.5	
t _s (L)	\overline{CET} or \overline{CEP} to CP	9.5					9.5	
t _h (H)	Hold Time	0.0					0.0	
t _h (L)	\overline{CET} or \overline{CEP} to CP	0.0					0.0	
t _s (H)	Setup Time	9.0					9.5	
t _s (L)	U/ \overline{D} to CP	9.0					9.5	
t _h (H)	Hold Time	0.0					0.0	
t _h (L)	U/ \overline{D} to CP	0.0					0.0	
t _w (H)	Clock Pulse Width	4.5					4.5	
t _w (L)	High or Low	4.5					4.5	
t _w (L)	\overline{MR} Pulse Width	3.0					3.0	
t _{rec}	Recovery Time MR to CP	4.0					4.0	

Ordering Information

The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)

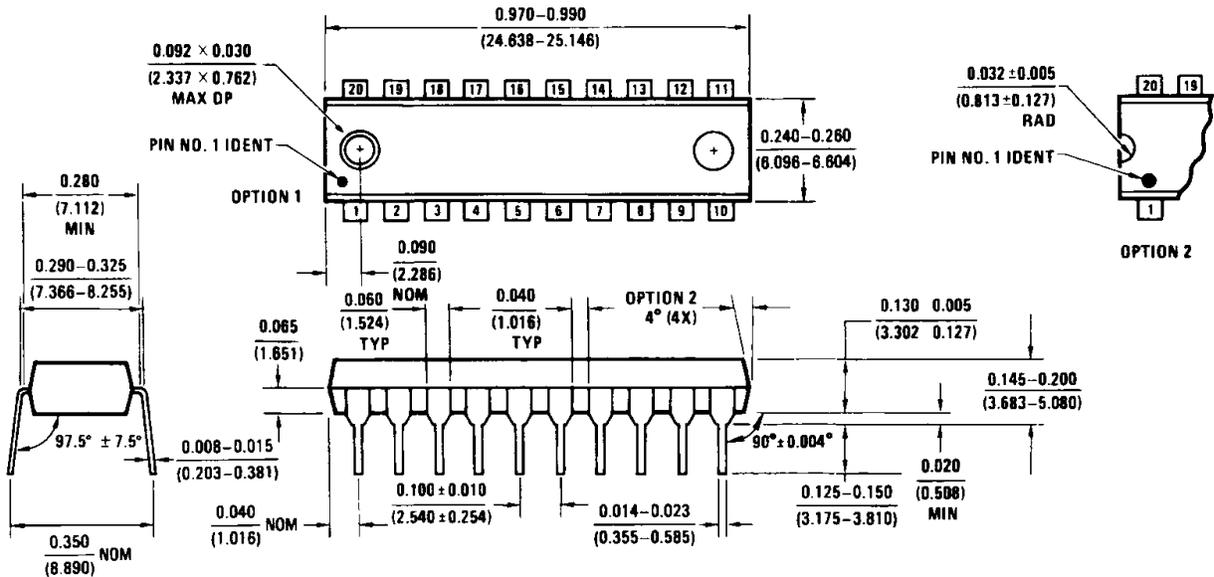


**20-Lead Small Outline Package - JEDEC (S)
NS Package Number M20B**

M20B (REV F)

Physical Dimensions inches (millimeters) (Continued)

Lit # 114851



**20-Lead Plastic Dual In-Line Package (P)
NS Package Number N20B**

N20B (REV A)

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: (408) 721-5000
TWX: (910) 339-9240

National Semiconductor GmbH
Industriestrasse 10
D-9060 Furstenfeldbruck
West Germany
Tel: (0-81-41) 103-0
Telex: 527-649
Fax: (08141) 103554

National Semiconductor Japan Ltd.
Sarseido Bldg. 5F
4-15 Nishi Shinjuku
Shinjuku-Ku,
Tokyo 160, Japan
Tel: 3-299-7001
FAX: 3-299-7000

National Semiconductor Hong Kong Ltd.
Suite 513, 5th Floor
Chinachem Golden Plaza,
77 Mody Road, Tsimshatsui East,
Kowloon, Hong Kong
Tel: 3-7231290
Telex: 52996 NSSEA HX
Fax: 3-3112536

National Semicondutores Do Brasil Ltda.
Av. Brig. Faria Lima, 1383
6.0 Andor-Conj. 62
01451 Sao Paulo, SP, Brasil
Tel: (55/11) 212-5066
Fax: (55/11) 211-1181 NSBR BR

National Semiconductor (Australia) PTY, Ltd.
1st Floor, 441 St. Kilda Rd.
Melbourne, 3004
Victoria, Australia
Tel: (03) 267-5000
Fax: 61-3-2677458