

Freescal Semiconductor

Technical Data

Document Number: MRF6S9060

Rev. 1, 6/2005

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies up to 1000 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common-source amplifier applications in 28 volt base station equipment.

- Typical Single-Carrier N-CDMA Performance @ 880 MHz, $V_{DD} = 28$ Volts, $I_{DQ} = 450$ mA, $P_{out} = 14$ Watts Avg., IS-95 CDMA (Pilot, Sync, Paging, Traffic Codes 8 Through 13) Channel Bandwidth = 1.2288 MHz. PAR = 9.8 dB @ 0.01% Probability on CCDF.
Power Gain — 21.4 dB
Drain Efficiency — 32.1%
ACPR @ 750 kHz Offset — -47.6 dBc @ 30 kHz Bandwidth

GSM EDGE Application

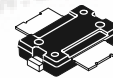
- Typical GSM EDGE Performance: $V_{DD} = 28$ Volts, $I_{DQ} = 500$ mA, $P_{out} = 21$ Watts Avg., Full Frequency Band (921-960 MHz)
Power Gain — 20 dB
Drain Efficiency — 46%
Spectral Regrowth @ 400 kHz Offset = -62 dBc
Spectral Regrowth @ 600 kHz Offset = -78 dBc
EVM — 1.5% rms

GSM Application

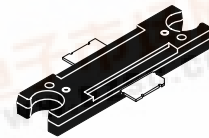
- Typical GSM Performance: $V_{DD} = 28$ Volts, $I_{DQ} = 500$ mA, $P_{out} = 60$ Watts, Full Frequency Band (921-960 MHz)
Power Gain — 20 dB
Drain Efficiency — 63%
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 880 MHz, 60 Watts CW Output Power
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Integrated ESD Protection
- N Suffix Indicates Lead-Free Terminations
- 200°C Capable Plastic Package
- TO-270-2 in Tape and Reel. R1 Suffix = 500 Units per 24 mm, 13 inch Reel.
- TO-272-2 in Tape and Reel. R1 Suffix = 500 Units per 44 mm, 13 inch Reel.

MRF6S9060NR1
MRF6S9060NBR1
MRF6S9060MR1
MRF6S9060MBR1

880 MHz, 14 W AVG., 28 V
SINGLE N-CDMA
LATERAL N-CHANNEL
BROADBAND RF POWER MOSFETs



CASE 1265-08, STYLE 1
TO-270-2
PLASTIC
MRF6S9060NR1(MR1)



CASE 1337-03, STYLE 1
TO-272-2
PLASTIC
MRF6S9060NBR1(MBR1)

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	- 0.5, +68	Vdc
Gate-Source Voltage	V_{GS}	- 0.5, +12	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	227 1.3	W W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

NOTE - CAUTION - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.



Table 2. Thermal Characteristics

Characteristic	Symbol	Value (1,2)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 60 W CW Case Temperature 80°C, 14 W CW	$R_{\theta JC}$	0.77 0.88	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22-A114)	1A (Minimum)
Machine Model (per EIA/JESD22-A115)	A (Minimum)
Charge Device Model (per JESD22-C101)	IV (Minimum)

Table 4. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	3	260	°C

Table 5. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

Off Characteristics

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 68\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc

On Characteristics

Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 200\text{ }\mu\text{A}$)	$V_{GS(th)}$	1	2	3	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ Vdc}$, $I_D = 450\text{ mAdc}$)	$V_{GS(Q)}$	—	2.9	—	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1.5\text{ Adc}$)	$V_{DS(on)}$	—	0.18	0.4	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 3\text{ Adc}$)	g_{fs}	—	4.2	—	S

Dynamic Characteristics

Input Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{iss}	—	106	—	pF
Output Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{oss}	—	33	—	pF
Reverse Transfer Capacitance ($V_{DS} = 28\text{ Vdc} \pm 30\text{ mV(rms)ac}$ @ 1 MHz, $V_{GS} = 0\text{ Vdc}$)	C_{rss}	—	1.4	—	pF

Functional Tests (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 450\text{ mA}$, $P_{out} = 14\text{ W Avg.}$, $f = 880\text{ MHz}$, Single-Carrier N-CDMA, 1.2288 MHz Channel Bandwidth Carrier. ACPR measured in 30 kHz Channel Bandwidth @ $\pm 750\text{ kHz}$ Offset. PAR = 9.8 dB @ 0.01% Probability on CCDF

Power Gain	G_{ps}	20.5	21.4	23.5	dB
Drain Efficiency	η_D	30.5	32.1	—	%
Adjacent Channel Power Ratio	ACPR	—	-47.6	-45	dBc
Input Return Loss	IRL	—	-15.3	-9	dB

1. MTTF calculator available at <http://www.freescale.com/rf>. Select Tools/Software/Application Software/Calculators to access the MTTF calculators by product.
2. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes - AN1955.

Table 5. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

Typical GSM EDGE Performances (In Freescale GSM EDGE Test Fixture Optimized for 921-960 MHz, 50 ohm system)

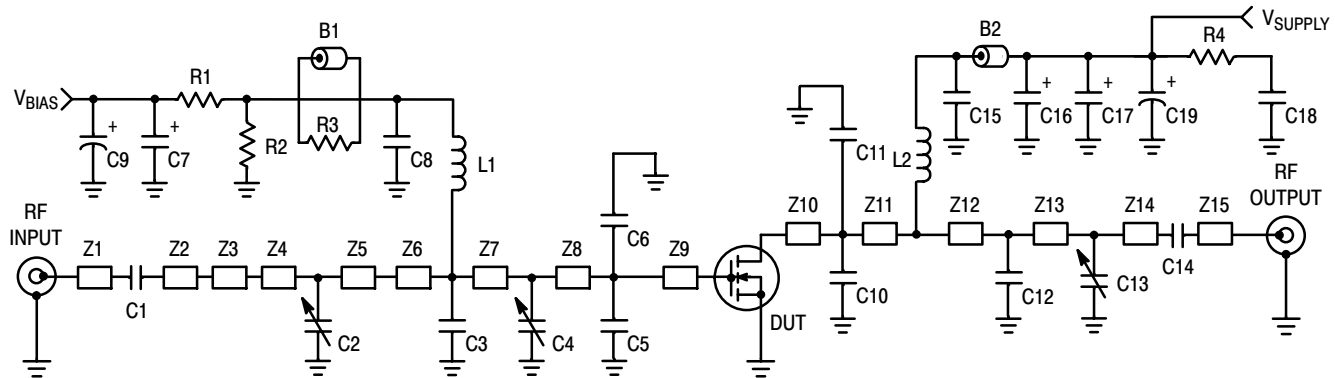
$V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 500\text{ mA}$, $P_{out} = 21\text{ W Avg.}$, $f = 921\text{ -}960\text{ MHz}$, GSM EDGE Signal

Power Gain	G_{ps}	—	20	—	dB
Drain Efficiency	η_D	—	46	—	%
Error Vector Magnitude	EVM	—	1.5	—	%
Spectral Regrowth at 400 kHz Offset	SR1	—	-62	—	dBc
Spectral Regrowth at 600 kHz Offset	SR2	—	-78	—	dBc

Typical CW Performances (In Freescale GSM Test Fixture Optimized for 921-960 MHz, 50 ohm system) $V_{DD} = 28\text{ Vdc}$,

$I_{DQ} = 500\text{ mA}$, $P_{out} = 60\text{ W}$, $f = 921\text{ -}960\text{ MHz}$

Power Gain	G_{ps}	—	20	—	dB
Drain Efficiency	η_D	—	63	—	%
Input Return Loss	IRL	—	-12	—	dB
P_{out} @ 1 dB Compression Point ($f = 940\text{ MHz}$)	P1dB	—	67	—	W



Z1	0.215" x 0.065" Microstrip	Z9	0.057" x 0.525" Microstrip
Z2	0.221" x 0.065" Microstrip	Z10	0.360" x 0.270" Microstrip
Z3	0.500" x 0.100" Microstrip	Z11	0.063" x 0.270" Microstrip
Z4	0.460" x 0.270" Microstrip	Z12	0.360" x 0.065" Microstrip
Z5	0.040" x 0.270" Microstrip	Z13	0.170" x 0.065" Microstrip
Z6	0.280" x 0.270" x 0.530" Taper	Z14	0.880" x 0.065" Microstrip
Z7	0.087" x 0.525" Microstrip	Z15	0.260" x 0.065" Microstrip
Z8	0.435" x 0.525" Microstrip	PCB	Taconic RF -35 0.030", $\epsilon_r = 3.5$

Figure 1. MRF6S9060NR1(NBR1)/MR1(MBR1) Test Circuit Schematic

Table 6. MRF6S9060NR1(NBR1)/MR1(MBR1) Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
B1	Ferrite Bead	95F786	Newark
B2	Ferrite Bead	95F787	Newark
C1, C8, C14, C15	47 pF Chip Capacitors	100B470JP500X	Newark
C2, C4, C13	0.8 - 8.0 pF Variable Capacitors, Gigatrim	44F3360	Newark
C3	3.0 pF Chip Capacitor	100B3R0JP500X	Newark
C5, C6	15 pF Chip Capacitors	100B150JP500X	Newark
C7, C16, C17	10 μ F, 35 V Tantalum Capacitors	93F2975	Newark
C9	100 μ F, 50 V Electrolytic Capacitor	51F2913	Newark
C10, C11	13 pF Chip Capacitors	100B130JP500X	Newark
C12	3.9 pF Chip Capacitor	100B3R9JP500X	Newark
C18	0.56 μ F Chip Capacitor	700A561MP150X	Newark
C19	470 μ F, 63 V Electrolytic Capacitor	95F4579	Newark
L1, L2	12.5 nH Inductor	A04T-5	Coilcraft
R1	1 k Ω Chip Resistor	05F1545	Newark
R2	560 k Ω Chip Resistor	84N2435	Newark
R3	12 Ω Chip Resistor	97C9103	Newark
R4	27 Ω Chip Resistor	04H7058	Newark

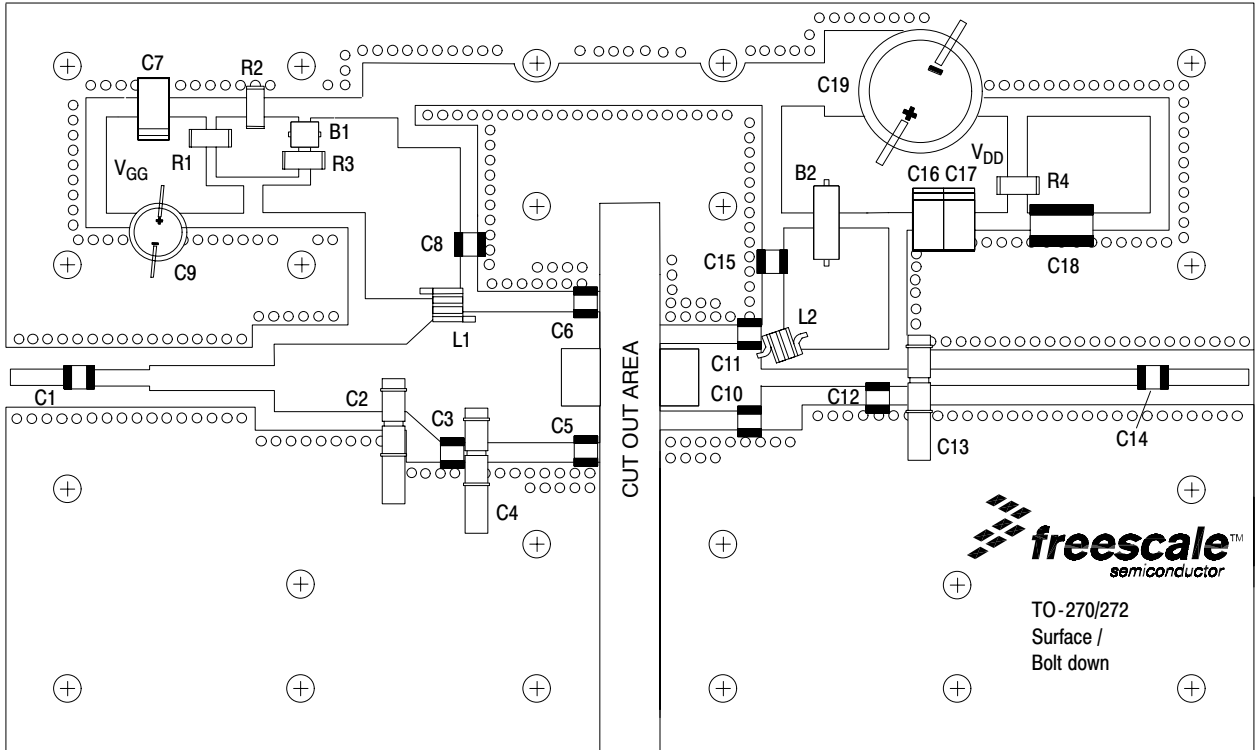


Figure 2. MRF6S9060NR1(NBR1)/MR1(MBR1) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

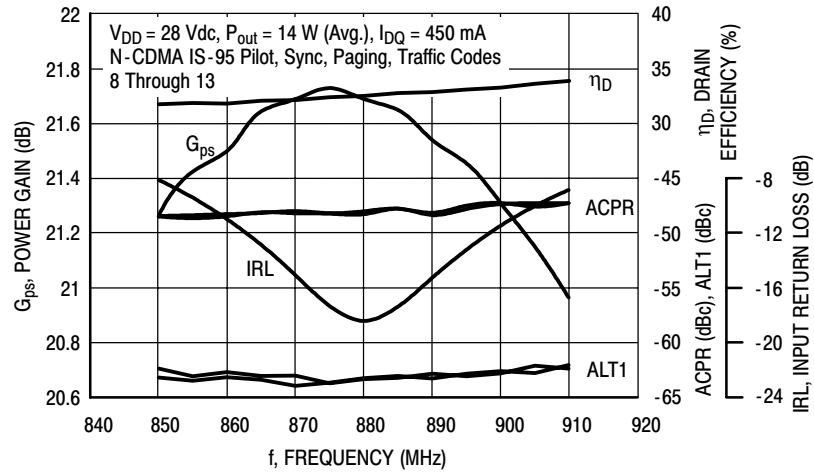


Figure 3. Single-Carrier N-CDMA Broadband Performance @ $P_{out} = 14$ Watts Avg.

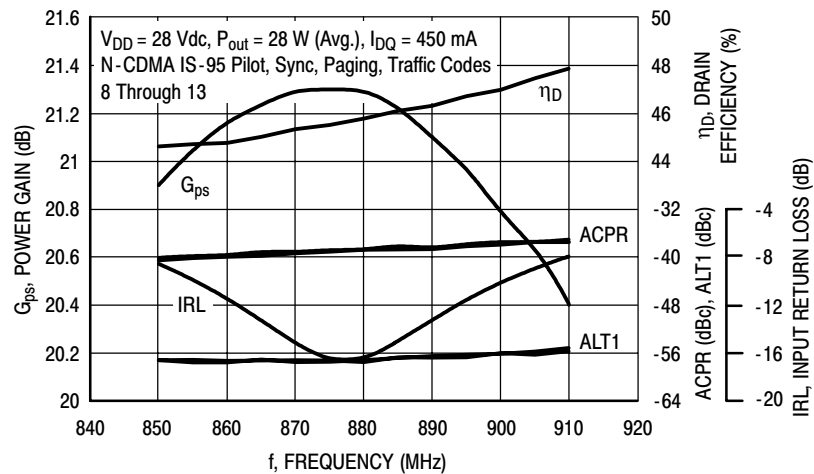


Figure 4. Single-Carrier N-CDMA Broadband Performance @ $P_{out} = 28$ Watts Avg.

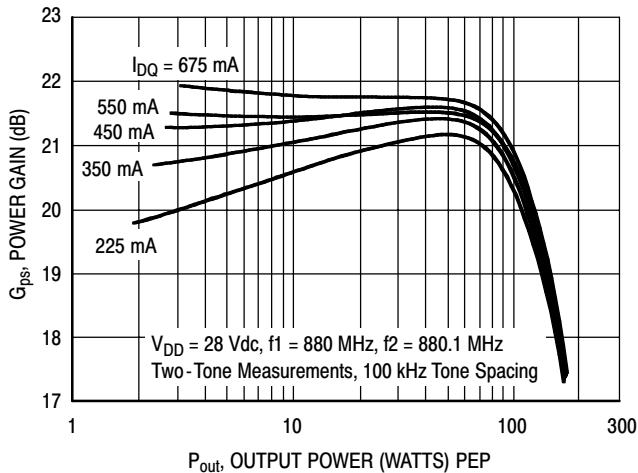


Figure 5. Two-Tone Power Gain versus Output Power

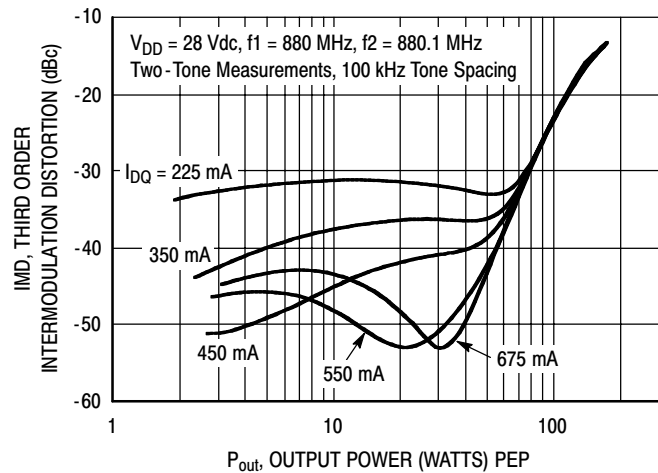


Figure 6. Third Order Intermodulation Distortion versus Output Power

TYPICAL CHARACTERISTICS

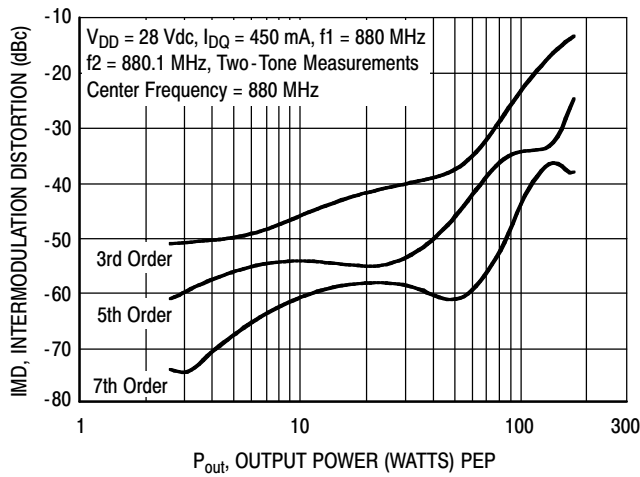


Figure 7. Intermodulation Distortion Products versus Output Power

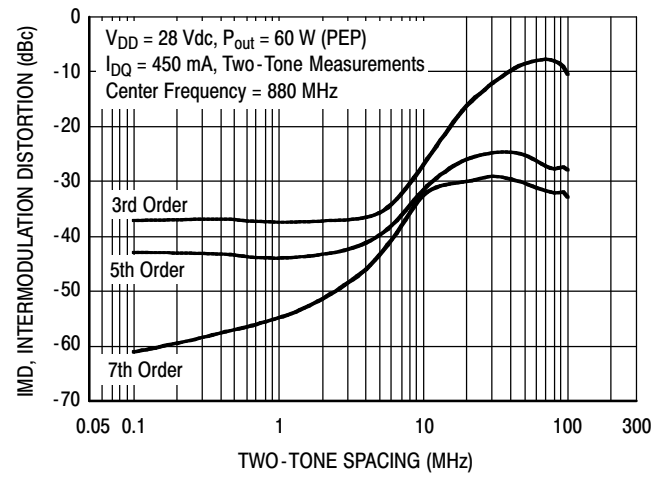


Figure 8. Intermodulation Distortion Products versus Tone Spacing

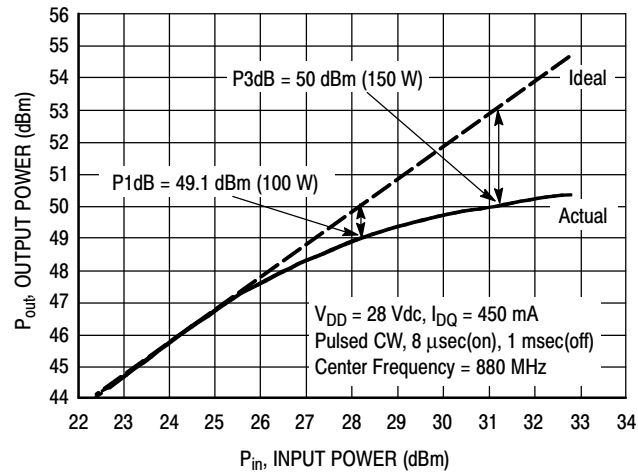


Figure 9. Pulse CW Output Power versus Input Power

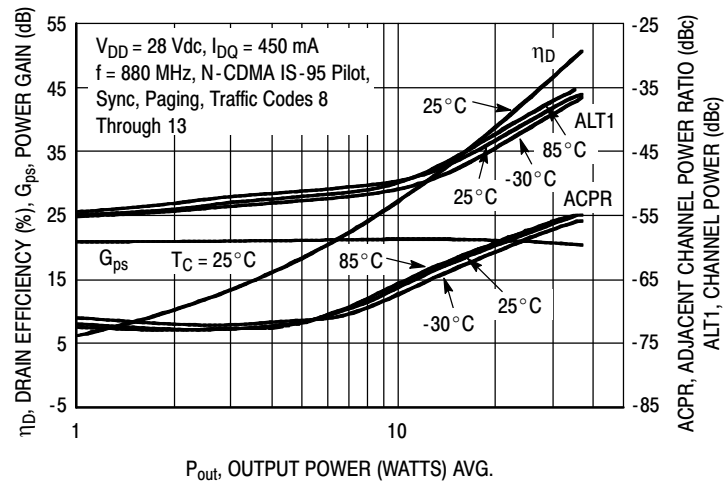


Figure 10. Single-Carrier N-CDMA ACPR, ALT1, Power Gain and Drain Efficiency versus Output Power

TYPICAL CHARACTERISTICS

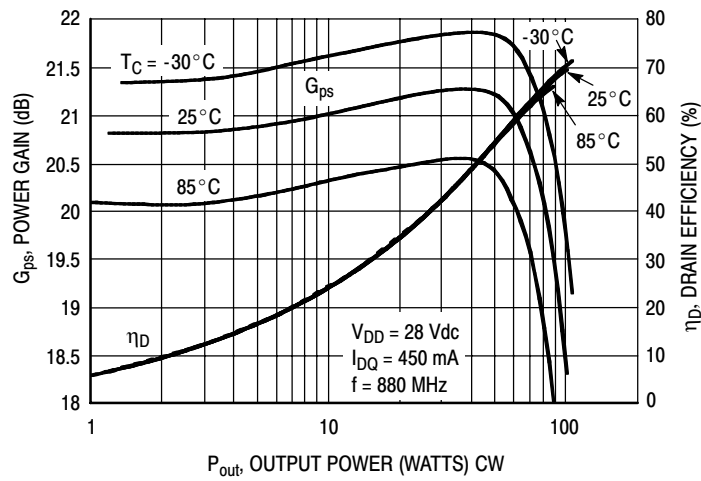


Figure 11. Power Gain and Drain Efficiency versus CW Output Power

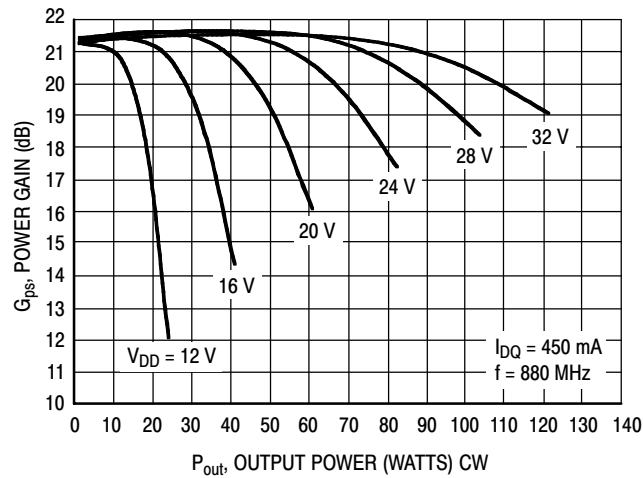
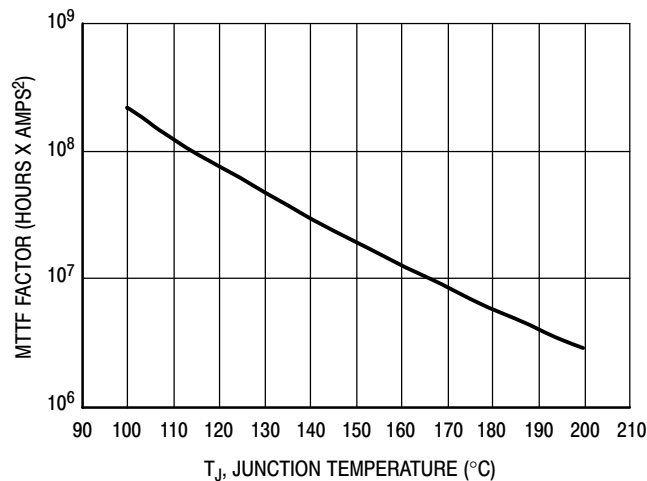


Figure 12. Power Gain versus Output Power



This above graph displays calculated MTTF in hours $\times$ ampere² drain current. Life tests at elevated temperatures have correlated to better than $\pm 10\%$ of the theoretical prediction for metal failure. Divide MTTF factor by I_D^2 for MTTF in a particular application.

Figure 13. MTTF Factor versus Junction Temperature

N-CDMA TEST SIGNAL

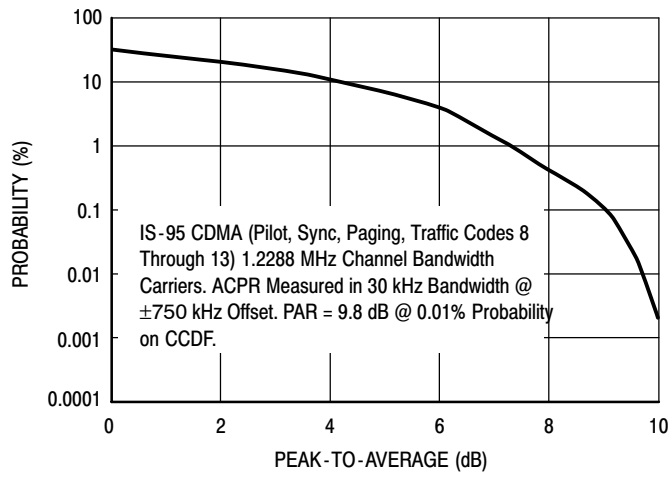


Figure 14. Single-Carrier CCDF N-CDMA

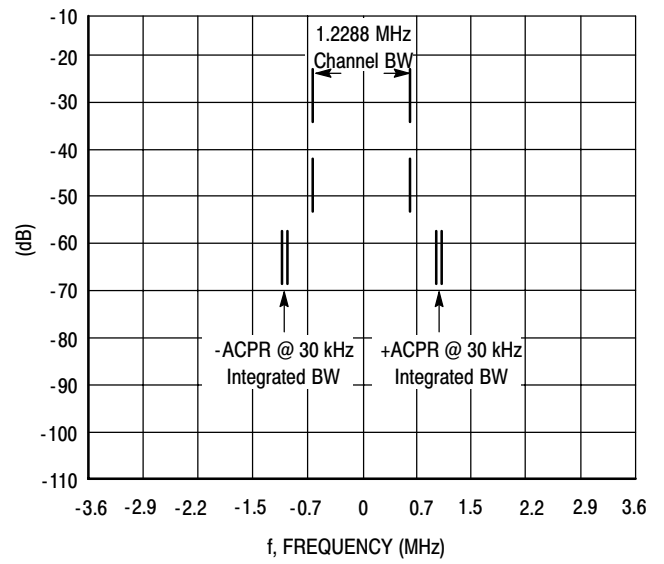
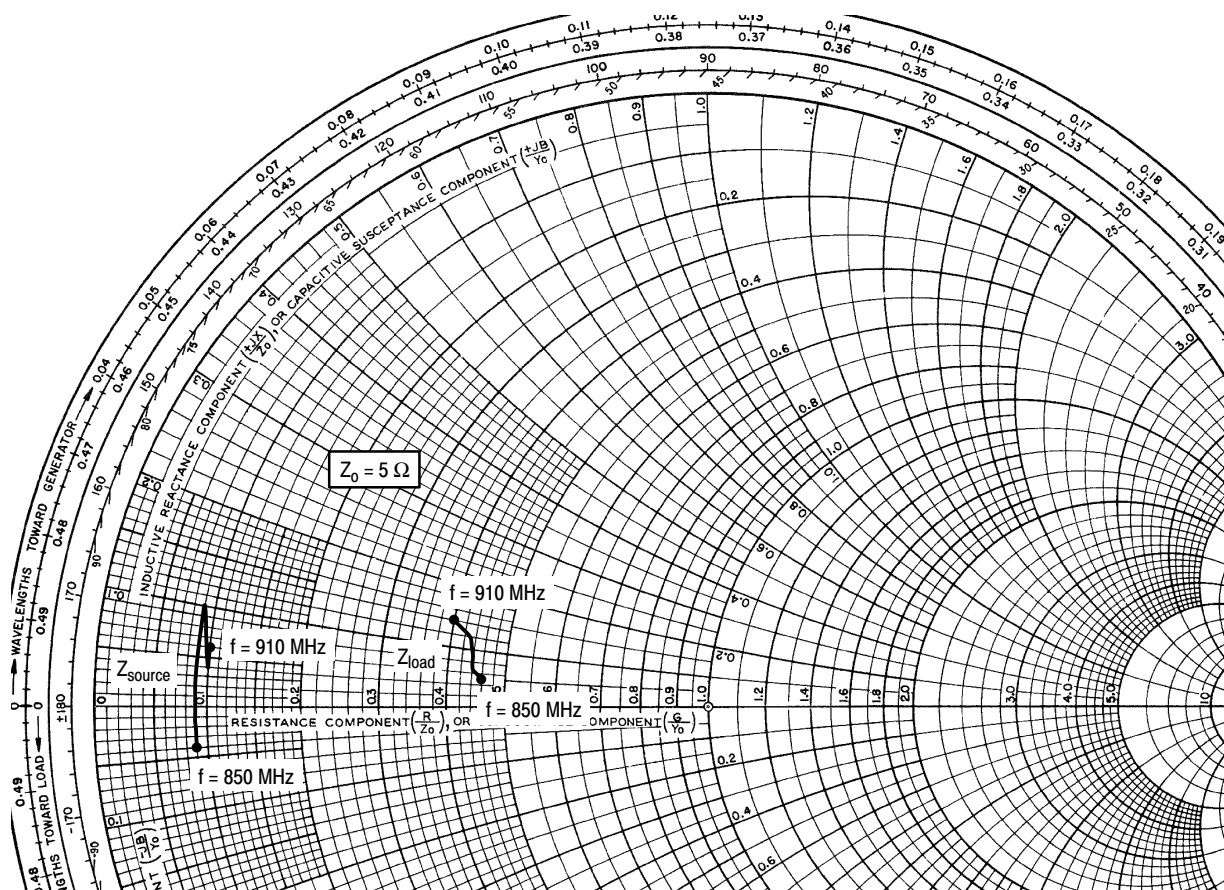


Figure 15. Single-Carrier N-CDMA Spectrum



$V_{DD} = 28 \text{ Vdc}$, $I_{DQ} = 450 \text{ mA}$, $P_{out} = 14 \text{ W Avg.}$

f MHz	Z_{source} Ω	Z_{load} Ω
850	$0.44 - j0.20$	$2.28 + j0.23$
865	$0.44 - j0.07$	$2.18 + j0.33$
880	$0.45 + j0.50$	$2.20 + j0.47$
895	$0.48 + j0.18$	$2.15 + j0.61$
910	$0.52 + j0.29$	$2.00 + j0.68$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

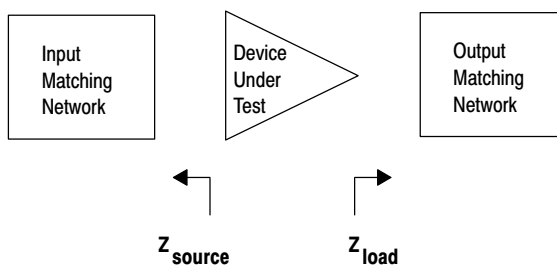


Figure 16. Series Equivalent Source and Load Impedance

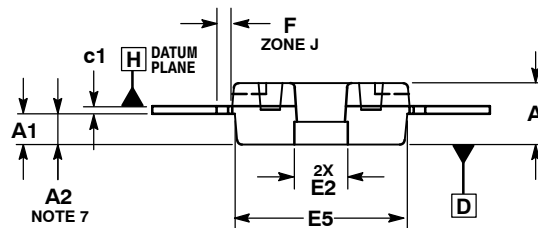
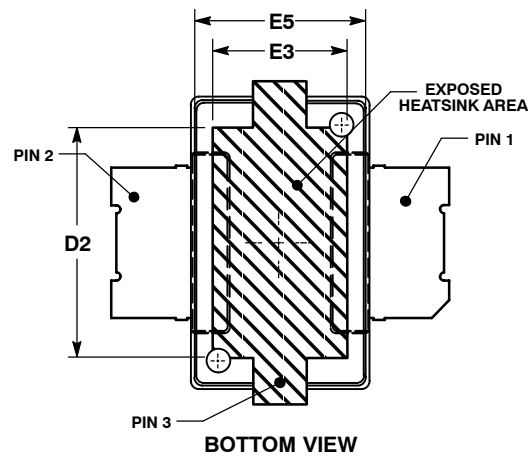
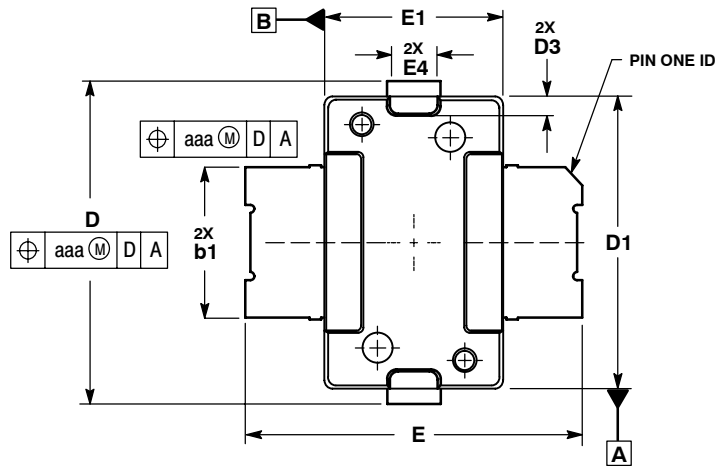
NOTES



NOTES

NOTES

PACKAGE DIMENSIONS



NOTES:

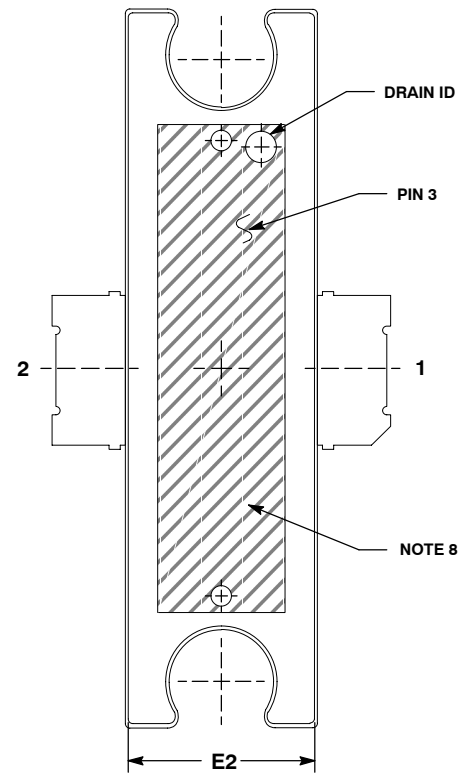
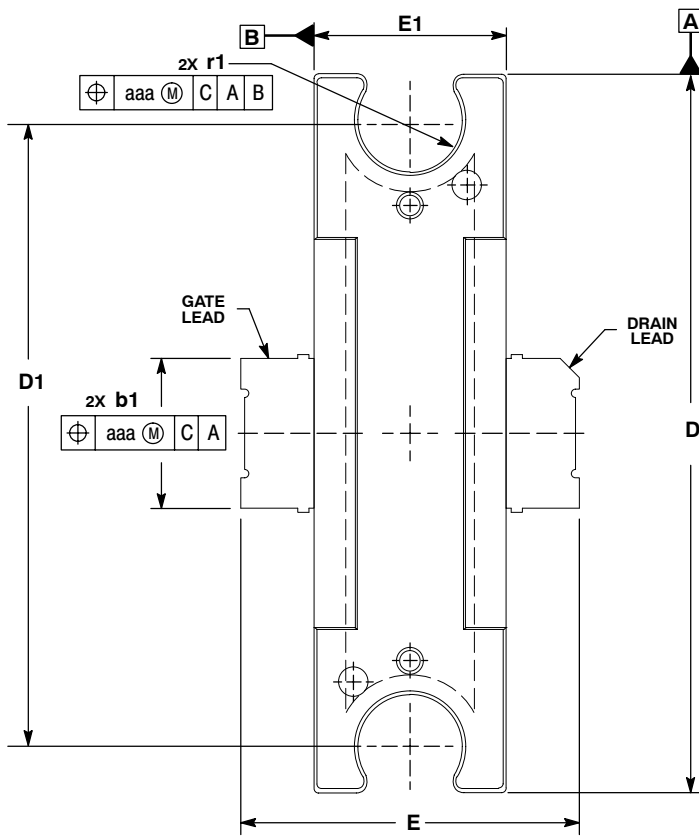
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D1" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D1" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION b1 DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE b1 DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. DIMENSIONS "D" AND "E2" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .003 PER SIDE. DIMENSIONS "D" AND "E2" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -D-.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.078	.082	1.98	2.08
A1	.039	.043	0.99	1.09
A2	.040	.042	1.02	1.07
D	.416	.424	10.57	10.77
D1	.378	.382	9.60	9.70
D2	.290	.320	7.37	8.13
D3	.016	.024	0.41	0.61
E	.436	.444	11.07	11.28
E1	.238	.242	6.04	6.15
E2	.066	.074	1.68	1.88
E3	.150	.180	3.81	4.57
E4	.058	.066	1.47	1.68
E5	.231	.235	5.87	5.97
F	.025 BSC		0.64 BSC	
b1	.193	.199	4.90	5.06
c1	.007	.011	0.18	0.28
aaa	.004		0.10	

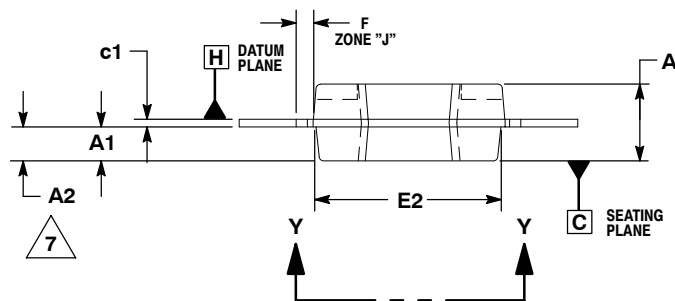
STYLE 1:

1. DRAIN
2. GATE
3. SOURCE

CASE 1265-08
ISSUE H
TO-270-2
PLASTIC
MRF6S9060NR1(MR1)



VIEW Y-Y



NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSION "b1" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.
8. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.100	.104	2.54	2.64
A1	.039	.043	0.99	1.09
A2	.040	.042	1.02	1.07
D	.928	.932	23.57	23.67
D1	.810 BSC		20.57 BSC	
E	.438	.442	11.12	11.23
E1	.248	.252	6.30	6.40
E2	.241	.245	6.12	6.22
F	.025 BSC		0.64 BSC	
b1	.193	.199	4.90	5.05
c1	.007	.011	.18	.28
r1	.063	.068	1.60	1.73
aaa	.004		.10	

STYLE 1:
PIN 1. DRAIN
2. GATE
3. SOURCE

**CASE 1337-03
ISSUE C
TO-272-2
PLASTIC
MRF6S9060NBR1(MBR1)**

How to Reach Us:

Home Page:

www.freescale.com

E-mail:

support@freescale.com

USA/Europe or Locations Not Listed:

Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:

Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.
© Freescale Semiconductor, Inc. 2005. All rights reserved.

