DUAL POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH CLEAR AND PRESET

SDFS046A – MARCH 1987 – REVISED OCTOBER 1993

- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

description

These devices contain two independent positive-edge-triggered D-type flip-flops. A low level at the preset ($\overline{PRE}$) or clear ($\overline{CLR}$) inputs sets or resets the outputs regardless of the levels of the other inputs. When $\overline{PRE}$ and $\overline{CLR}$ are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input may be changed without affecting the levels at the outputs.

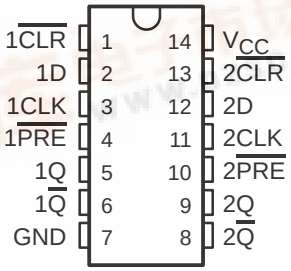
The SN54F74 is characterized for operation over the full military temperature range of –55°C to 125°C. The SN74F74 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

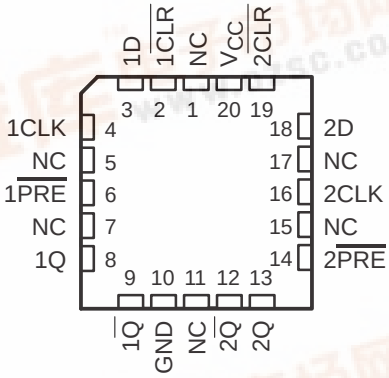
INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

† The output levels are not guaranteed to meet the minimum levels for V_{OH}. Furthermore, this configuration is nonstable; that is, it will not persist when $\overline{PRE}$ or $\overline{CLR}$ returns to its inactive (high) level.

SN54F74 . . . J PACKAGE
SN74F74 . . . D OR N PACKAGE
(TOP VIEW)

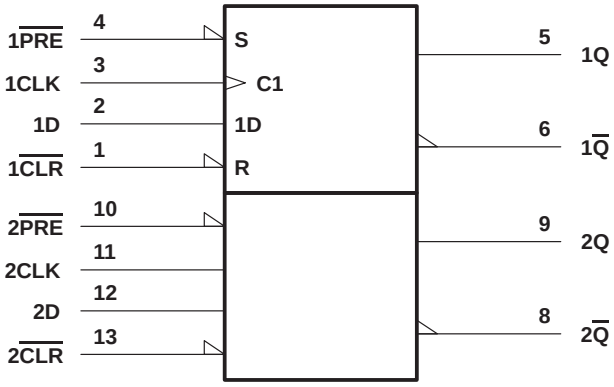


SN54F74 . . . FK PACKAGE
(TOP VIEW)



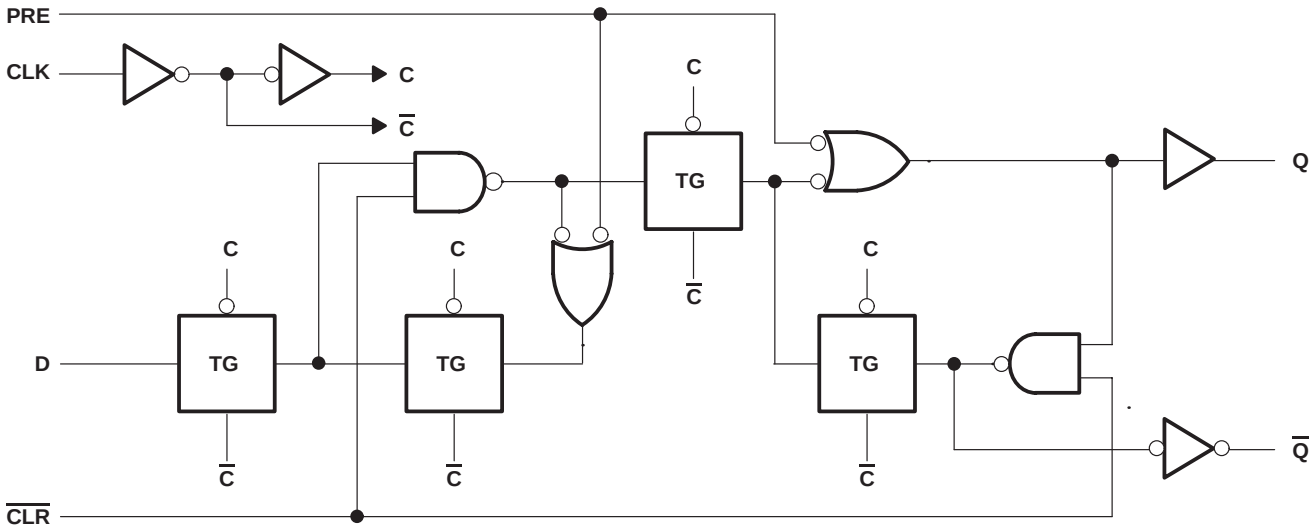
NC – No internal connection

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the D, J, and N packages.

logic diagram, each flip-flop (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –1.2 V to 7 V
Input current range . . . . . –30 mA to 5 mA
Voltage range applied to any output in the high state . . . . . –0.5 V to V_{CC}
Current into any output in the low state . . . . . 40 mA
Operating free-air temperature range: SN54F74 . . . . . –55°C to 125°C
SN74F74 . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input voltage ratings may be exceeded provided the input current ratings are observed.

recommended operating conditions

		SN54F74			SN74F74			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{IK}	Input clamp current			–18			–18	mA
I_{OH}	High-level output current			– 1			– 1	mA
I_{OL}	Low-level output current			20			20	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54F74			SN74F74			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = – 1 mA	2.5	3.4		2.5	3.4		V
		V_{CC} = 4.75 V,	I_{OH} = – 1 mA				2.7			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.3	0.5		0.3	0.5	V
I_I		V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}		V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	Data, CLK	V_{CC} = 5.5 V,	V_I = 0.5 V			– 0.6			– 0.6	mA
	$\overline{PRE}$ or $\overline{CLR}$					– 1.8			– 1.8	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0	–60		–150	–60		–150	mA
I_{CC}		V_{CC} = 5.5 V,	See Note 2		10.5	16		10.5	16	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: I_{CC} is measured with D, CLK, and $\overline{PRE}$ grounded then with D, CLK, and $\overline{CLR}$ grounded.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V_{CC} = 5 V, T_A = 25°C		SN54F74		SN74F74		UNIT
			′F74						
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0	100	0	80	0	100	MHz
t_w	Pulse duration	CLK high, $\overline{PRE}$ or $\overline{CLR}$ low	4		4		4		ns
		CLK low	5		6		5		
t_{su}	Setup time, data before CLK↑	High	2		3		2		ns
		Low	3		4		3		
	Setup time, inactive-state before CLK↑§	$\overline{PRE}$ or $\overline{CLR}$ to CLK	2		3		2		
t_h	Hold time, data after CLK↑	High	1		2		1		ns
		Low	1		2		1		

§ Inactive-state setup time is also referred to as recovery time.

switching characteristics (see Note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R_L = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†				UNIT
			′F74			SN54F74		SN74F74		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			100	145		80		100		MHz
t_{PLH}	CLK	Q or $\overline{Q}$	3	4.9	6.8	3.8	8.5	3	7.8	ns
t_{PHL}			3.6	5.8	8	4.4	10.5	3.6	9.2	
t_{PLH}	$\overline{PRE}$ or $\overline{CLR}$	Q or $\overline{Q}$	2.4	4.2	6.1	3.2	8	2.4	7.1	ns
t_{PHL}			2.7	6.6	9	3.5	11.5	2.7	10.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

NOTE 3: Load circuits and waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
5962-9759201Q2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
5962-9759201QCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
5962-9759201QDA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
JM38510/34101B2A	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
JM38510/34101BCA	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
JM38510/34101BDA	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC
SN54F74J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SN74F74D	ACTIVE	SOIC	D	14	50	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74F74DR	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SN74F74N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN74F74N3	OBSOLETE	PDIP	N	14		None	Call TI	Call TI
SN74F74NSR	ACTIVE	SO	NS	14	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
SNJ54F74FK	ACTIVE	LCCC	FK	20	1	None	Call TI	Level-NC-NC-NC
SNJ54F74J	ACTIVE	CDIP	J	14	1	None	Call TI	Level-NC-NC-NC
SNJ54F74W	ACTIVE	CFP	W	14	1	None	Call TI	Level-NC-NC-NC

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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