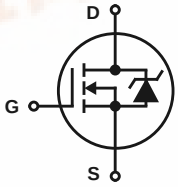
20A, 20V, 0.022 Ohm, N-Channel, Logic Level Power MOSFETs

The HUF76013 is an application-specific MOSFET optimized for switching when used as the upper switch in synchronous buck applications. The low gate charge and low input capacitance results in lower driver and lower switching losses thereby increasing the overall system efficiency.

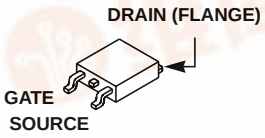
UltraFET™

Symbol

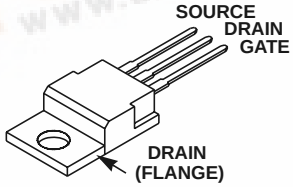


Packaging

HUF76013D3S
JEDEC TO-252AA



HUF76013P3
JEDEC TO-220AB



Features

- 20A, 20V
  - $r_{DS(ON)}$ = 0.022Ω, V_{GS} = 10V
  - $r_{DS(ON)}$ = 0.030Ω, V_{GS} = 5V
- PWM Optimized for Synchronous Buck Applications
- Fast Switching
- Low Gate Charge
  - Q_g Total 14nC (Typ)
- Low Capacitance
  - C_{ISS} 624pF (Typ)
  - C_{RSS} 71pF (Typ)

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF76013P3	TO-220AB	76013P
HUF76013D3S	TO-252AA	76013D

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the HUF76013D3S in tape and reel, e.g., HUF76013D3ST.

Absolute Maximum Ratings T_C = 25°C, Unless Otherwise Specified

SYMBOL	PARAMETER	HUF76013P3, HUF76013D3S	UNITS
V_{DSS}	Drain to Source Voltage (Note 1)	20	V
V_{DGR}	Drain to Gate Voltage (R_{GS} = 20kΩ) (Note 1)	20	V
V_{GS}	Gate to Source Voltage	±16	V
	Drain Current		
I_D	Continuous (T_C = 25°C, V_{GS} = 10V) (Figure 2)	20	A
I_D	Continuous (T_C = 100°C, V_{GS} = 5V)	20	A
I_{DM}	Pulsed Drain Current	Figure 4	A
P_D	Power Dissipation	50	W
	Derate Above 25°C	0.4	W/°C
T_J, T_{STG}	Operating and Storage Temperature	-55 to 150	°C
	Maximum Temperature for Soldering		
T_L	Leads at 0.063in (1.6mm) from Case for 10s	300	°C
T_{pkg}	Package Body for 10s, See Techbrief TB334	260	°C
THERMAL SPECIFICATIONS			
$R_{\theta JC}$	Thermal Resistance Junction to Case, TO-220, TO-252	2.5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient TO-220	62	°C/W
	Thermal Resistance Junction to Ambient TO-252	100	°C/W

NOTE:

1. T_J = 25°C to 125°C.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV_{DSS}	I_D = 250μA, V_{GS} = 0V (Figure 11)		20	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V		-	-	1	μA
		V_{DS} = 20V, V_{GS} = 0V, $T_C = 150^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	V_{GS} = ±16V		-	-	±100	nA
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250μA (Figure 10)		1	-	3	V
Drain to Source ON Resistance	$r_{DS(ON)}$	I_D = 20A, V_{GS} = 10V (Figures 8, 9)		-	0.018	0.022	W
		I_D = 20A, V_{GS} = 5V (Figure 8)		-	0.025	0.030	W
SWITCHING SPECIFICATIONS (V_{GS} = 5V)							
Turn-On Time	t_{ON}	V_{DD} = 10V, I_D = 20A V_{GS} = 5V, R_{GS} = 19Ω (Figures 14, 18, 19)		-	-	197	ns
Turn-On Delay Time	$t_{d(ON)}$			-	11	-	ns
Rise Time	t_r			-	120	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	19	-	ns
Fall Time	t_f			-	30	-	ns
Turn-Off Time	t_{OFF}			-	-	72	ns
SWITCHING SPECIFICATIONS (V_{GS} = 10V)							
Turn-On Time	t_{ON}	V_{DD} = 10V, I_D = 20A V_{GS} = 10V, R_{GS} = 19Ω (Figures 15, 18, 19)		-	-	151	ns
Turn-On Delay Time	$t_{d(ON)}$			-	7	-	ns
Rise Time	t_r			-	93	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	37	-	ns
Fall Time	t_f			-	29	-	ns
Turn-Off Time	t_{OFF}			-	-	100	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge at 10V	$Q_{g(TOT)}$	V_{GS} = 0V to 10V	V_{DD} = 10V, I_D = 20A, $I_{g(REF)}$ = 1.0mA (Figures 13, 16, 17)	-	14.4	17	nC
Total Gate Charge at 5V	$Q_{g(TOT)}$	V_{GS} = 0V to 5V		-	7.8	9	nC
Threshold Gate Charge	$Q_{g(TH)}$	V_{GS} = 0V to 1V		-	0.9	1	nC
Gate to Source Gate Charge	Q_{gs}			-	3.5	-	nC
Gate to Drain “Miller” Charge	Q_{gd}			-	3.2	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz (Figure 12)		-	624	-	pF
Output Capacitance	C_{OSS}			-	444	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	71	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 20A	-	-	1.25	V
		I_{SD} = 10A	-	-	1.0	V
Reverse Recovery Time	t_{rr}	I_{SD} = 20A, dI_{SD}/dt = 100A/μs	-	-	55	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 20A, dI_{SD}/dt = 100A/μs	-	-	82	nC

Typical Performance Curves

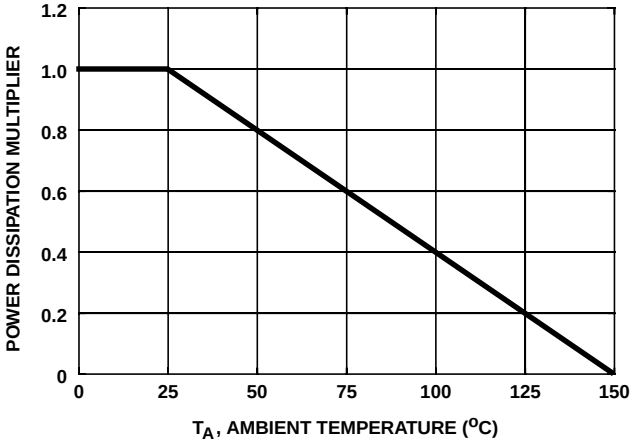


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

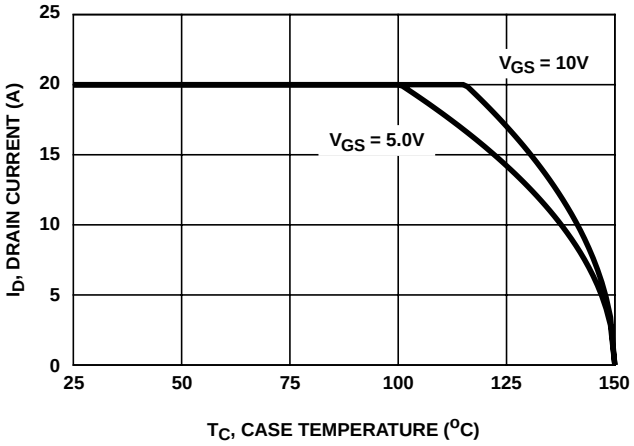


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

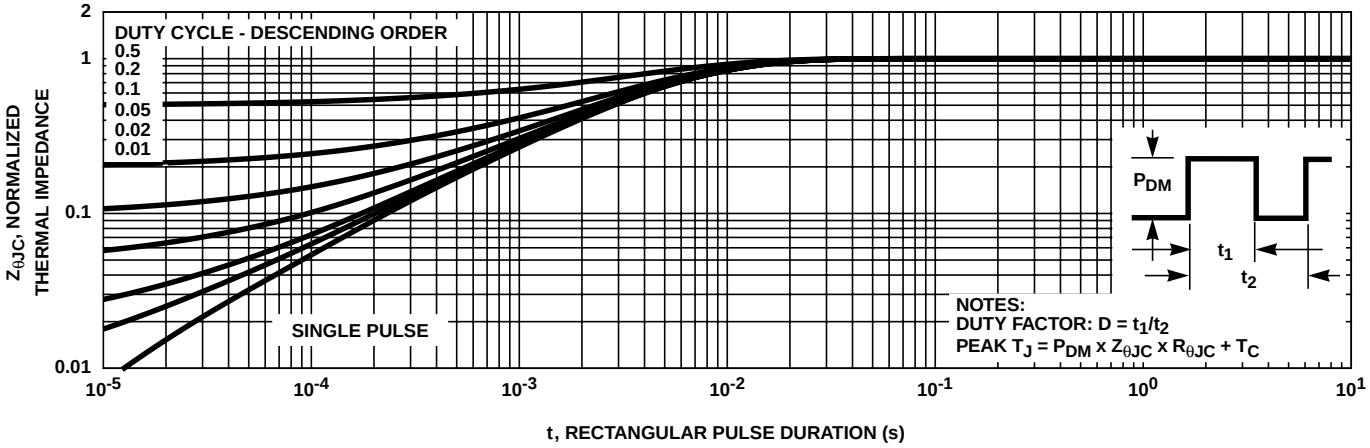


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

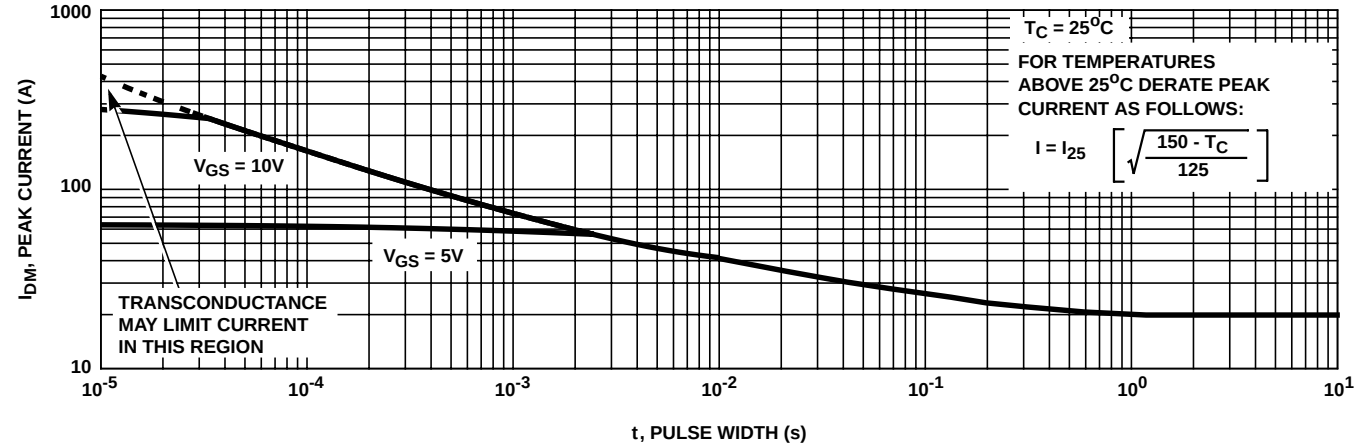


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

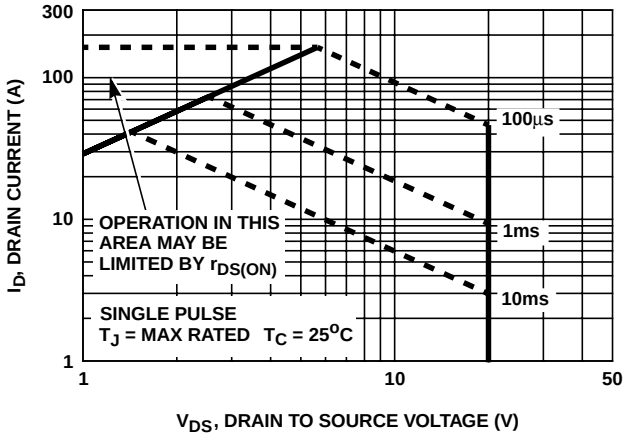


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA

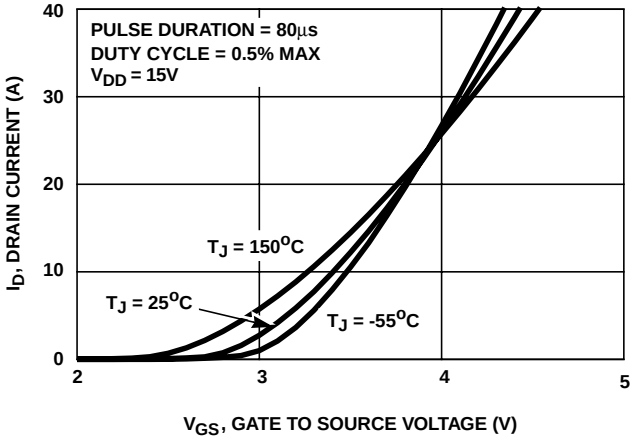


FIGURE 6. TRANSFER CHARACTERISTICS

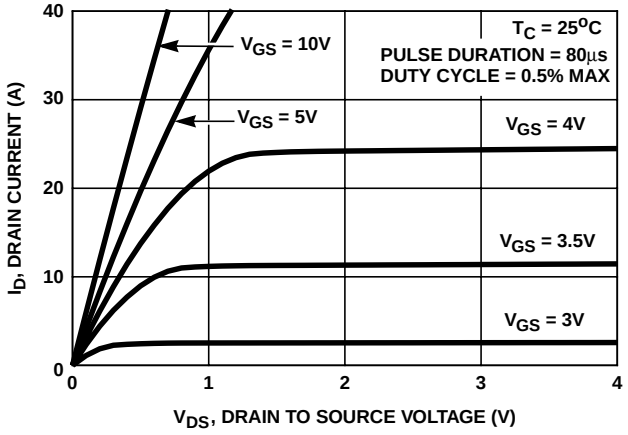


FIGURE 7. SATURATION CHARACTERISTICS

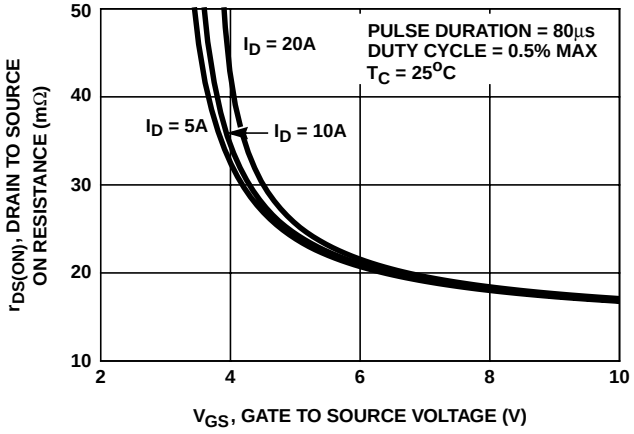


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

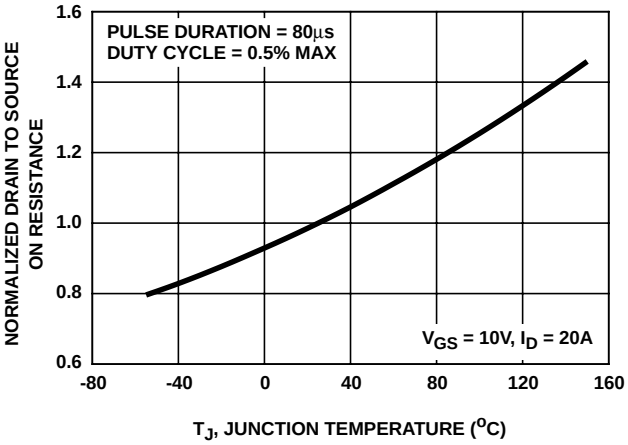


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

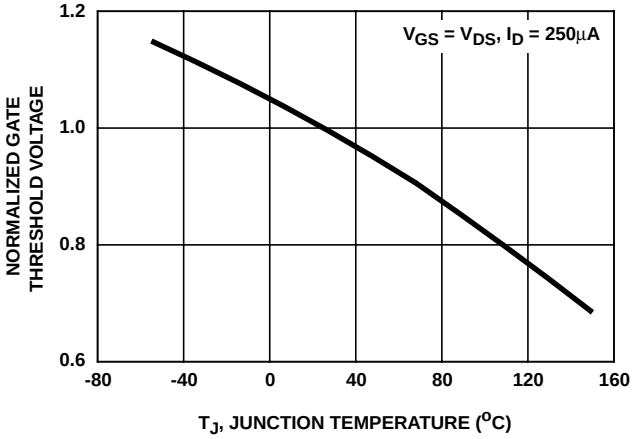


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

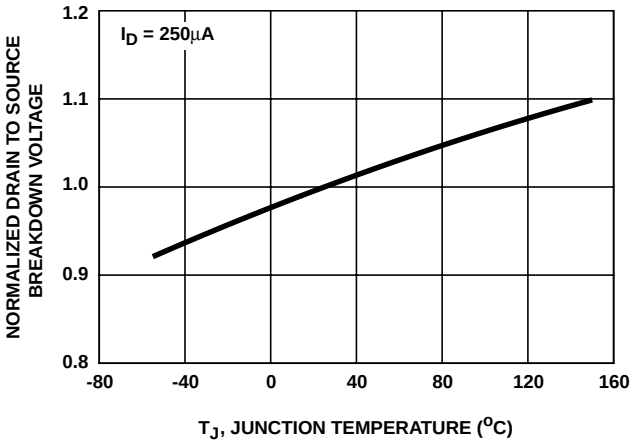


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

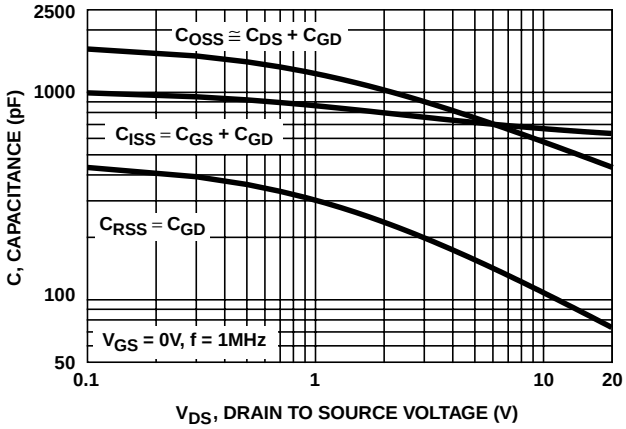
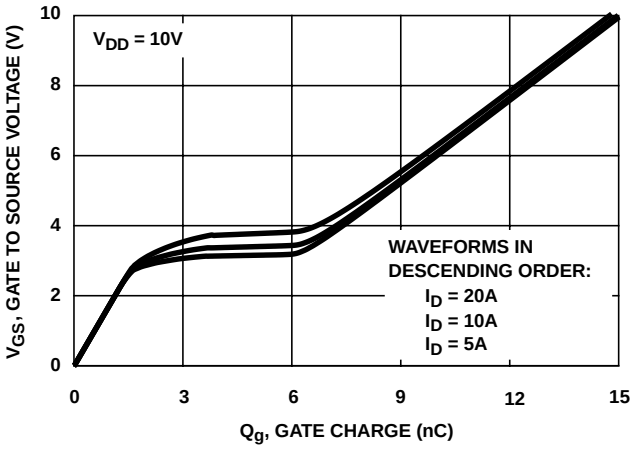


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

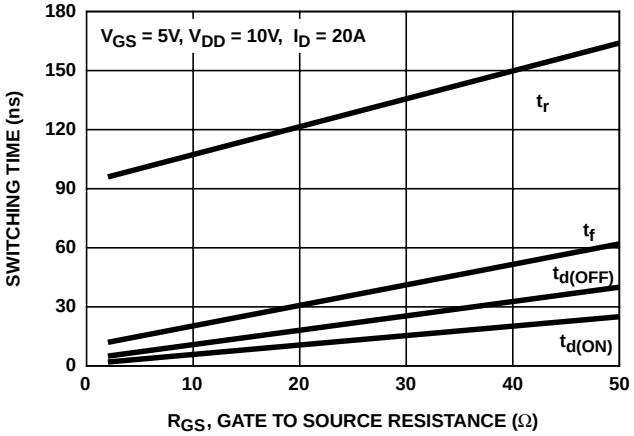


FIGURE 14. SWITCHING TIME vs GATE RESISTANCE

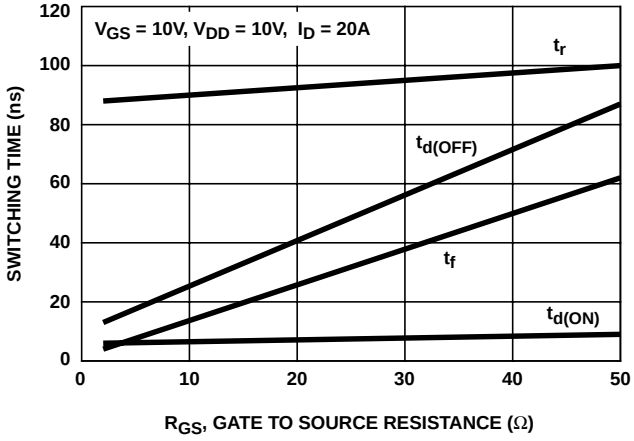


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

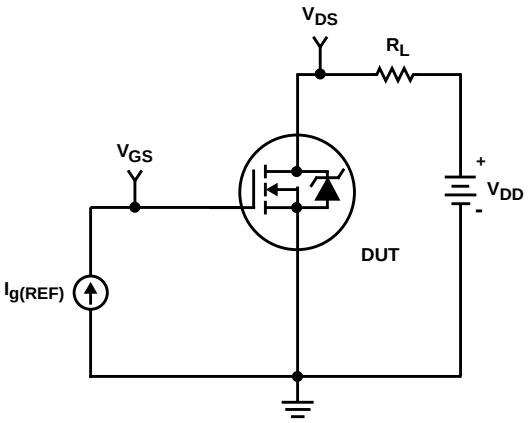


FIGURE 16. GATE CHARGE TEST CIRCUIT

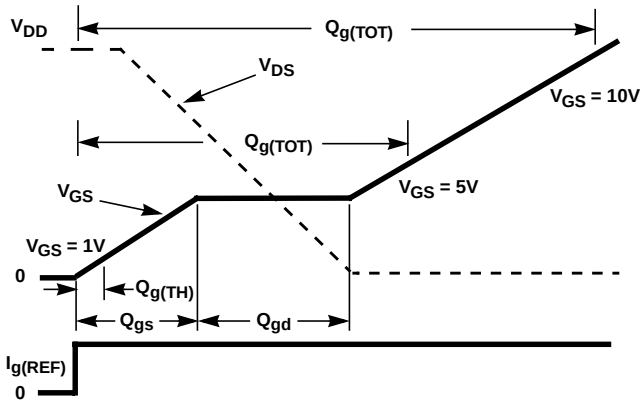


FIGURE 17. GATE CHARGE WAVEFORMS

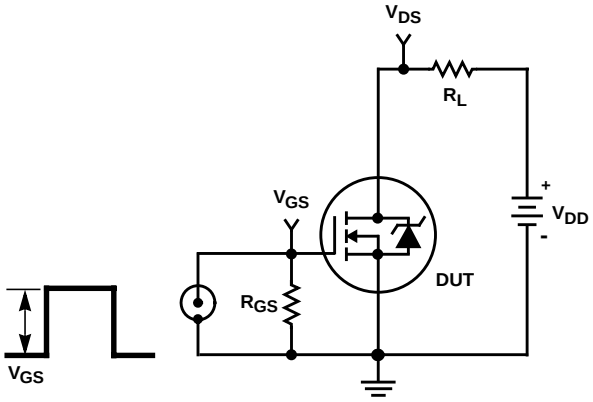


FIGURE 18. SWITCHING TIME TEST CIRCUIT

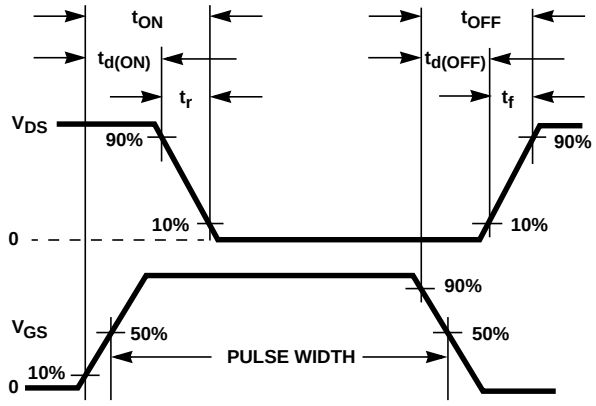


FIGURE 19. SWITCHING TIME WAVEFORM

PSPICE Electrical Model

.SUBCKT HUF76013P3 2 1 3 ; rev 23March 2000

CA 12 8 6.5e-10
CB 15 14 7.0e-10
CIN 6 8 5.6e-10

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 26
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

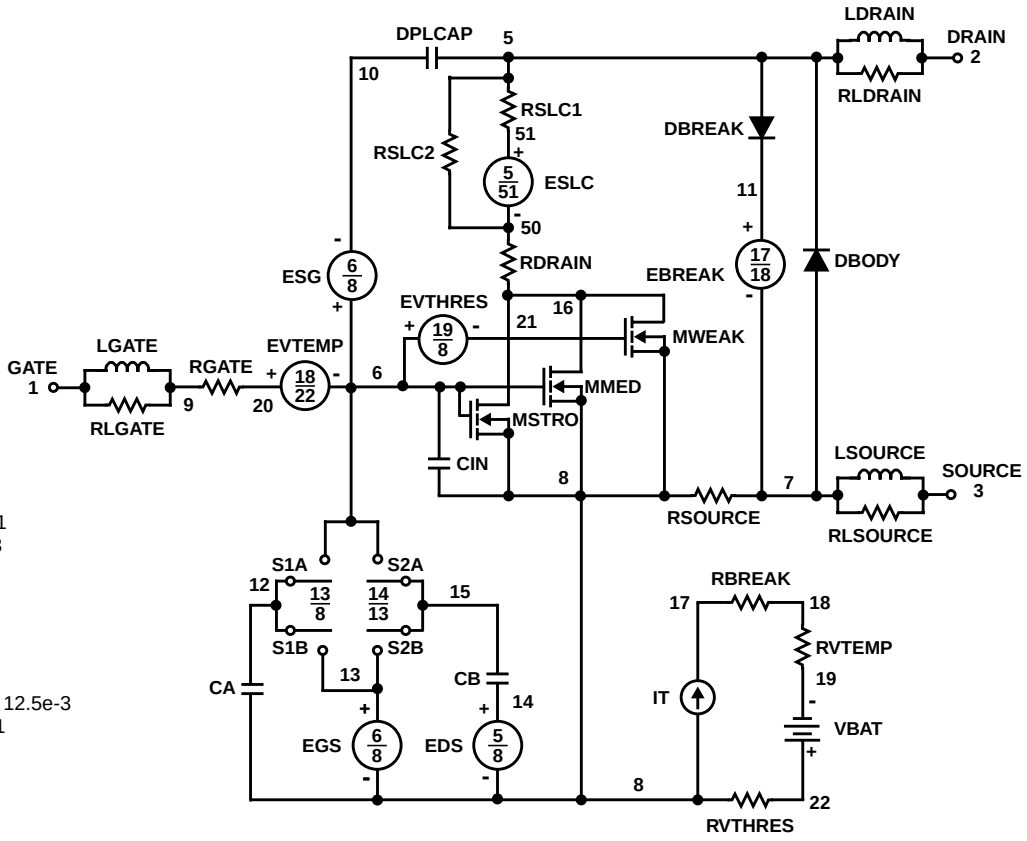
IT 8 17 1

LDRAIN 2 5 1.00e-9
LGATE 1 9 4.9e-9
LSOURCE 3 7 4.9e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 1e-3
RGATE 9 20 3.0
RLDRAIN 2 5 10
RLGATE 1 9 49
RLSOURCE 3 7 49
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 12.5e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD



VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*175),2.5))}

.MODEL DBODYMOD D (IS = 5.4e-13 RS = 1.15e-2 TRS1 = 7.0e-5 TRS2 = -1.0e-6 CJO = 12.3e-10 TT = 2.93e-8 M = 0.40)
.MODEL DBREAKMOD D (RS = 3.50e-1 TRS1 = 1e-3 TRS2 = -6.5e-6)
.MODEL DPLCAPMOD D (CJO = 4.6e-10 IS = 1e-30 N = 10 M = 0.6)
.MODEL MMEDMOD NMOS (VTO = 2.2 KP = 2.0 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 3.0)
.MODEL MSTROMOD NMOS (VTO = 2.66 KP = 40 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u LAMBDA=.01)
.MODEL MWEAKMOD NMOS (VTO = 1.90 KP = 0.03 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 30 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.0e-3 TC2 = -1.0e-6)
.MODEL RDRAINMOD RES (TC1 = 2.1e-2 TC2 = 6.5e-5)
.MODEL RSLCMOD RES (TC1 = 3.5e-3 TC2 = 2e-6)
.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)
.MODEL RVTHRESMOD RES (TC1 = -1.9e-3 TC2 = -6.0e-6)
.MODEL RVTEMPMOD RES (TC1 = -1.8e-3 TC2 = 0)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.5 VOFF= -1.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.5 VOFF= -4.5)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.5 VOFF= 0)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0 VOFF= -0.5)

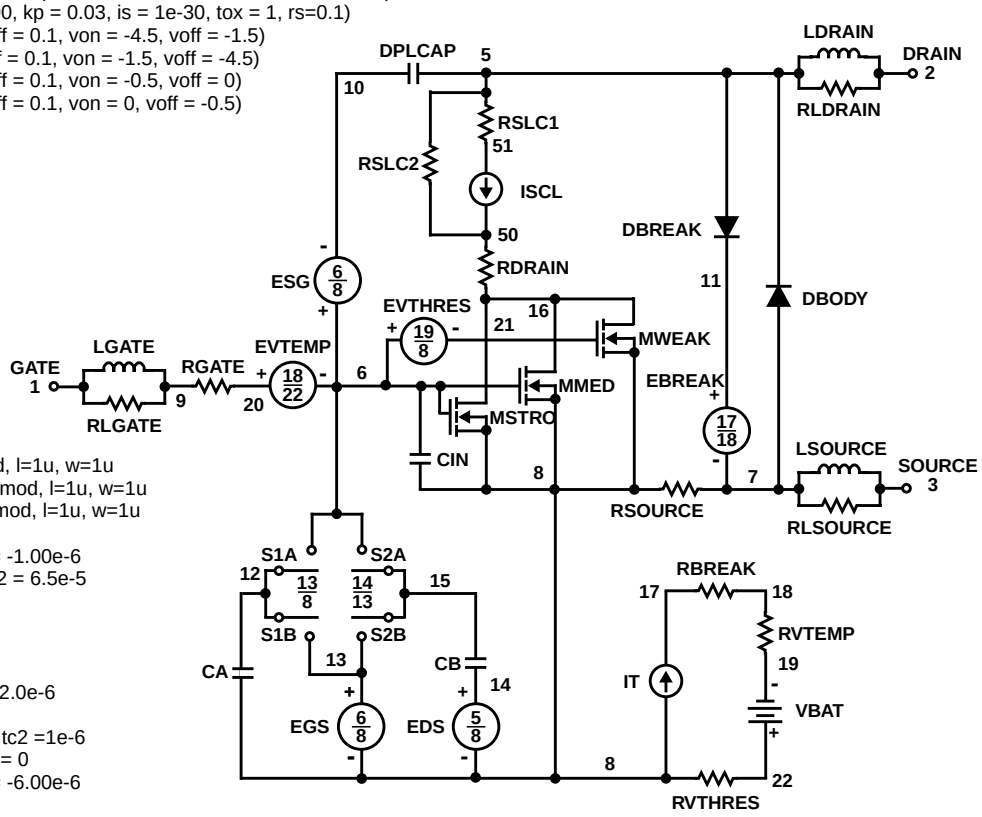
.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

SABER Electrical Model

REV 23March2000

```
template huf76013p3 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod =  (isl = 5.4e-13, rs = 1.15e-2, trs1 = 7.0e-5, trs2 = -1e-6, cjo = 12.3e-10, tt = 2.93e-8, m = 0.40)
dp..model dbreakmod = (rs = 3.50e-1, trs1 = 1e-3, trs2 = -6.5e-6)
dp..model dplcapmod =  (cjo = 4.60e-10, isl = 10e-30,nl=10, m = 0.6)
m..model mmedmod = (type=_n, vto = 2.2, kp = 2.0, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 2.66, kp = 40, lamda=0.01, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 1.90, kp = 0.03, is = 1e-30, tox = 1, rs=0.1)
sw_vcsp..model s1amod =  (ron = 1e-5, roff = 0.1, von = -4.5, voff = -1.5)
sw_vcsp..model s1bmod =  (ron =1e-5, roff = 0.1, von = -1.5, voff = -4.5)
sw_vcsp..model s2amod =  (ron = 1e-5, roff = 0.1, von = -0.5, voff = 0)
sw_vcsp..model s2bmod =  (ron = 1e-5, roff = 0.1, von = 0, voff = -0.5)

c.ca n12 n8 = 6.50e-10
c.cb n15 n14 = 7.0e-10
c.cin n6 n8 = 5.60e-10

dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1.00e-9
l.lgate n1 n9 = 4.9e-9
l.lsource n3 n7 = 4.9e-9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18  = 1, tc1 = 1.0e-3, tc2 = -1.00e-6
res.rdrain n50 n16  = 1e-3, tc1 = 2.1e-2, tc2 = 6.5e-5
res.rgate n9 n20 = 3.0
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 49
res.rlsource n3 n7 = 49
res.rslc1 n5 n51= 1e-6, tc1 = 3.5e-3, tc2 = 2.0e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 12.5e-3, tc1 = 1.0e-3, tc2 =1e-6
res.rvtemp n18 n19  = 1, tc1 = -1.8e-3, tc2 = 0
res.rvthres n22 n8  = 1, tc1 = -1.9e-3, tc2 = -6.00e-6

spe.ebreak n11 n7 n17 n18 = 26
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/175))** 2.5))
}
}
```



SPICE Thermal Model

REV 23March 2000

HUF76013T

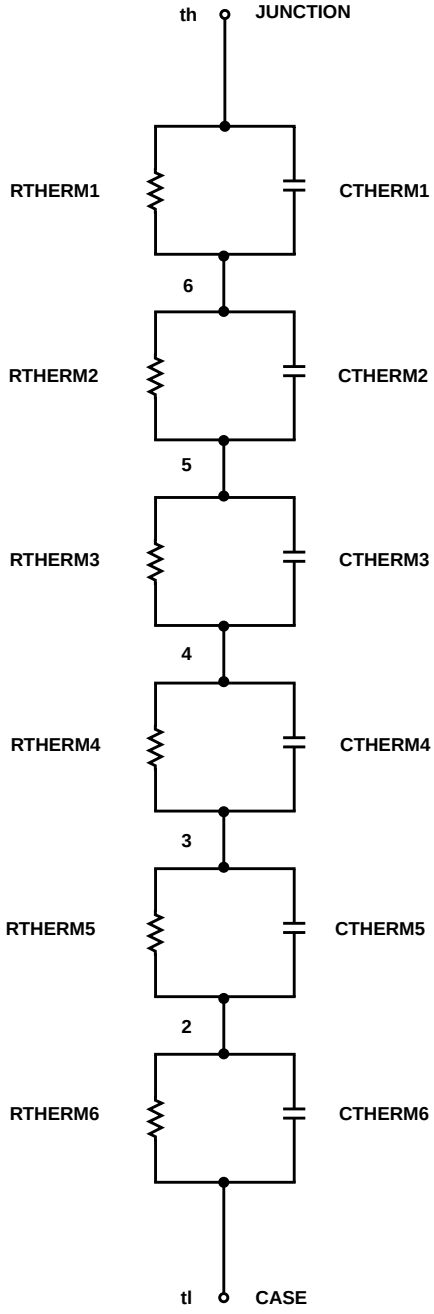
CTHERM1 th 6 1.0e-3
CTHERM2 6 5 2.80e-3
CTHERM3 5 4 3.00e-3
CTHERM4 4 3 3.40e-3
CTHERM5 3 2 6.40e-3
CTHERM6 2 tl 9.50e-2

RTHERM1 th 6 1.85e-2
RTHERM2 6 5 4.61e-2
RTHERM3 5 4 1.30e-1
RTHERM4 4 3 7.29e-1
RTHERM5 3 2 1.10
RTHERM6 2 tl 1.46e-1

SABER Thermal Model

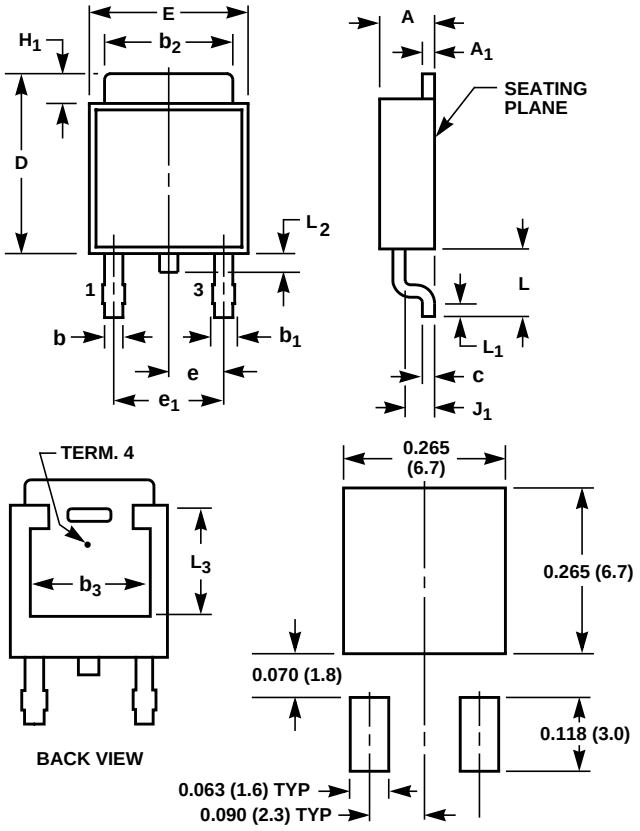
SABER thermal model HUF76013T

```
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 1.0e-3
ctherm.ctherm2 6 5 = 2.80e-3
ctherm.ctherm3 5 4 = 3.00e-3
ctherm.ctherm4 4 3 = 3.40e-3
ctherm.ctherm5 3 2 = 6.40e-3
ctherm.ctherm6 2 tl = 9.50e-2

rtherm.rtherm1 th 6 =1.85e-2
rtherm.rtherm2 6 5 = 4.61e-2
rtherm.rtherm3 5 4 = 1.30e-1
rtherm.rtherm4 4 3 = 7.29e-1
rtherm.rtherm5 3 2 = 1.10
rtherm.rtherm6 2 tl = 1.46e-1
}
```



TO-252AA

SURFACE MOUNT JEDEC TO-252AA PLASTIC PACKAGE



MINIMUM PAD SIZE RECOMMENDED FOR SURFACE-MOUNTED APPLICATIONS

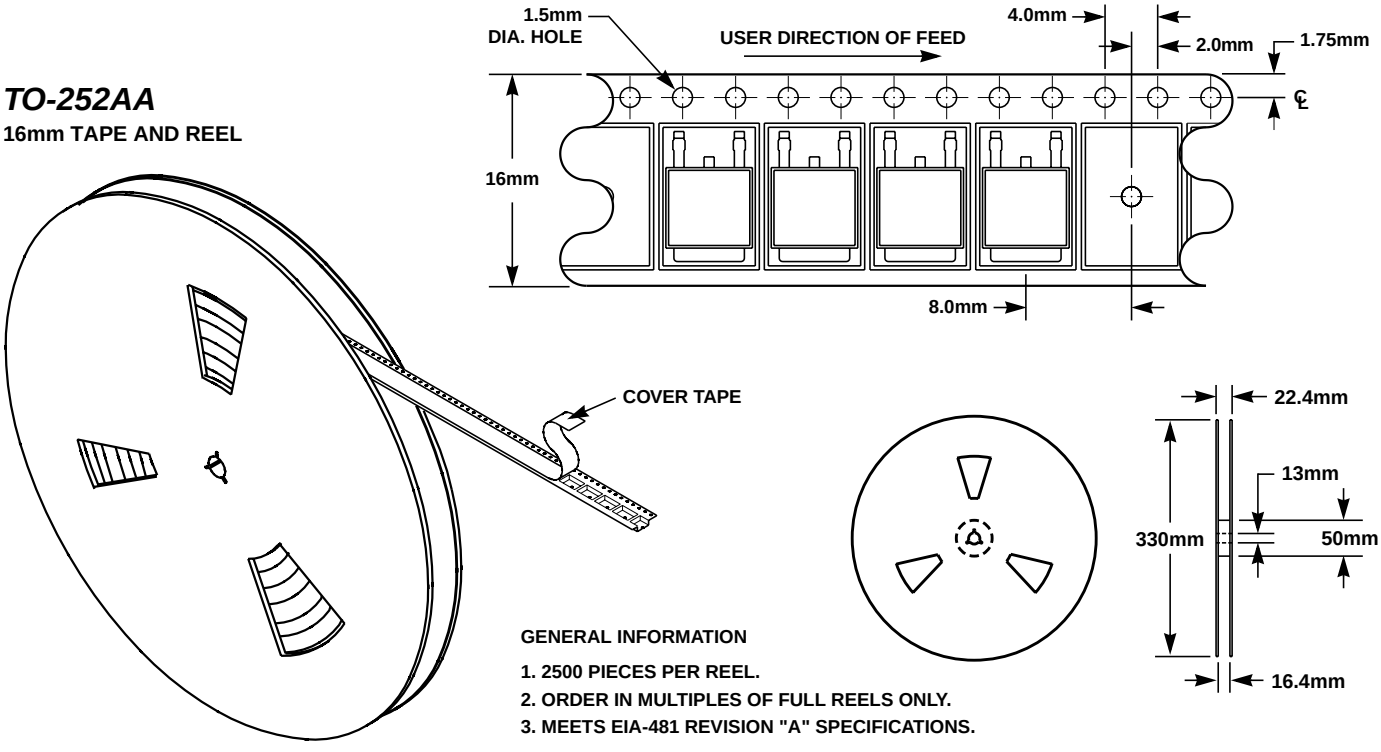
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.086	0.094	2.19	2.38	-
A_1	0.018	0.022	0.46	0.55	4, 5
b	0.028	0.032	0.72	0.81	4, 5
b_1	0.033	0.045	0.84	1.14	4
b_2	0.205	0.215	5.21	5.46	4, 5
b_3	0.190	-	4.83	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.270	0.295	6.86	7.49	-
E	0.250	0.265	6.35	6.73	-
e	0.090 TYP		2.28 TYP		7
e_1	0.180 BSC		4.57 BSC		7
H_1	0.035	0.045	0.89	1.14	-
J_1	0.040	0.045	1.02	1.14	-
L	0.100	0.115	2.54	2.92	-
L_1	0.020	-	0.51	-	4, 6
L_2	0.025	0.040	0.64	1.01	3
L_3	0.170	-	4.32	-	2

NOTES:

1. These dimensions are within allowable dimensions of Rev. B of JEDEC TO-252AA outline dated 9-88.
2. L_3 and b_3 dimensions establish a minimum mounting surface for terminal 4.
3. Solder finish uncontrolled in this area.
4. Dimension (without solder).
5. Add typically 0.002 inches (0.05mm) for solder plating.
6. L_1 is the terminal length for soldering.
7. Position of lead to be measured 0.090 inches (2.28mm) from bottom of dimension D.
8. Controlling dimension: Inch.
9. Revision 11 dated 1-00.

TO-252AA

16mm TAPE AND REEL



GENERAL INFORMATION

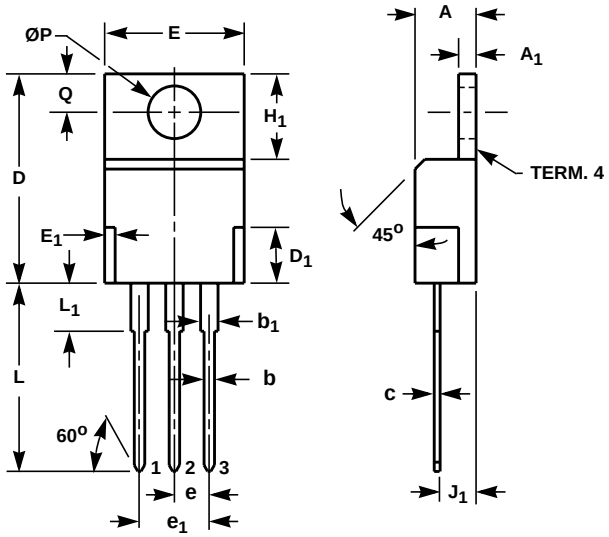
1. 2500 PIECES PER REEL.

2. ORDER IN MULTIPLES OF FULL REELS ONLY.

3. MEETS EIA-481 REVISION "A" SPECIFICATIONS.

TO-220AB

3 LEAD JEDEC TO-220AB PLASTIC PACKAGE



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A_1	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b_1	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D_1	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E_1	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e_1	0.200 BSC		5.08 BSC		5
H_1	0.235	0.255	5.97	6.47	-
J_1	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L_1	0.130	0.150	3.31	3.81	2
ØP	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L_1.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 7-97.

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