

July 1999

# FDG6303N Dual N-Channel, Digital FET

### **General Description**

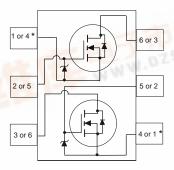
These dual N-Channel logic level enhancement mode field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance. This device has been designed especially for low voltage applications as a replacement for bipolar digital transistors and small signal MOSFETs.

### **Features**

- Very low level gate drive requirements allowing direct operation in 3 V circuits (V<sub>GS(th)</sub> < 1.5 V).</li>
- Gate-Source Zener for ESD ruggedness (>6kV Human Body Model).
- Compact industry standard SC70-6 surface mount package.







<sup>\*</sup> The pinouts are symmetrical; pin 1 and 4 are interchangeable.

Units inside the carrier can be of either orientation and will not affect the functionality of the device.

### Absolute Maximum Ratings T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	FDG6303N	Units		
V <sub>DSS</sub>	Drain-Source Voltage	25	V		
V <sub>GSS</sub>	Gate-Source Voltage	8	V		
D	Drain/Output Current - Continuous	0.5	А		
	- Pulsed	1.5			
<b>D</b> D	Maximum Power Dissipation (Note 1)	0.3			
T <sub>J</sub> ,T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to 150			
ESD	Electrostatic Discharge Rating MIL-STD-883D Human Body Model (100 pF / 1500 Ω)	6.0	kV		
THERMA	L CHARACTERISTICS				
R <sub>eja</sub>	Thermal Resistance, Junction-to-Ambient	415	°C/W		



Symbol	Parameter	Conditions	Min	Тур	Max	Units
OFF CHAR	ACTERISTICS		I	1		.1
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$	25			V
$\Delta BV_{DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		26		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 20 \text{ V}, \ V_{GS} = 0 \text{ V}$			1	μA
		T <sub>J</sub> = 55°C			10	μA
I <sub>GSS</sub>	Gate - Body Leakage Current	$V_{GS} = 8 \text{ V}, \ V_{DS} = 0 \text{ V}$			100	nA
ON CHARAC	CTERISTICS (Note 2)		•			
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$	0.65	0.8	1.5	V
$\Delta V_{GS(th)}/\Delta T_{J}$	Gate Threshold Voltage Temp.Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C		-2.6		mV/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 4.5 \text{ V}, \ I_{D} = 0.5 \text{ A}$		0.34	0.45	Ω
		T <sub>J</sub> =125°C		0.55	0.77	1
		$V_{GS} = 2.7 \text{ V}, I_D = 0.2 \text{ A}$		0.44	0.6	1
I <sub>D(ON)</sub>	On-State Drain Current	$V_{GS} = 2.7 \text{ V}, \ V_{DS} = 5 \text{ V}$	0.5			Α
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_{D} = 0.5 \text{ A}$		1.45		S
DYNAMIC CI	HARACTERISTICS					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 10 \text{ V}, \ V_{GS} = 0 \text{ V},$ f = 1.0 MHz		50		pF
C <sub>oss</sub>	Output Capacitance	† = 1.0 MHz		28		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			9		рF
SWITCHING	CHARACTERISTICS (Note 2)					
t <sub>D(on)</sub>	Turn - On Delay Time	$V_{DD} = 5 \text{ V}, I_{D} = 0.5 \text{ A},$		3	6	ns
ţ	Turn - On Rise Time	$V_{GS} = 4.5 \text{ V}, R_{GEN} = 50 \Omega$		8.5	18	ns
t <sub>D(off)</sub>	Turn - Off Delay Time			17	30	ns
t <sub>f</sub>	Turn - Off Fall Time			13	25	ns
$Q_g$	Total Gate Charge	$V_{DS} = 5 \text{ V}, I_{D} = 0.5 \text{ A}, V_{GS} = 4.5 \text{ V}$		1.64	2.3	nC
$Q_{gs}$	Gate-Source Charge	V <sub>GS</sub> = 4.5 V		0.38		nC
$Q_{gd}$	Gate-Drain Charge			0.45		nC
	RCE DIODE CHARACTERISTICS AND MAXIM	IUM RATINGS	T .	I .		
l <sub>s</sub>	Maximum Continuous Source Current				0.25	Α
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 0.25 \text{ A (Note 2)}$		0.8	1.2	V

Notes:

1. R<sub>BJA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>BJC</sub> is guaranteed by design while  $R_{\text{loch}}$  is determined by the user's board design.  $R_{\text{loch}} = 415^{\circ}\text{C/W}$  on minimum pad mounting on FR-4 board in still air. 2. Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

### **Typical Electrical Characteristics**

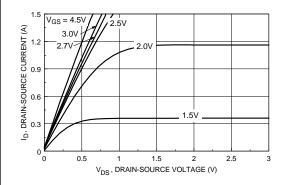


Figure 1. On-Region Characteristics.

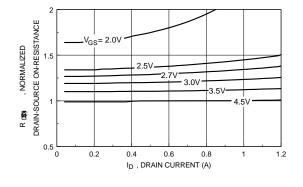


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

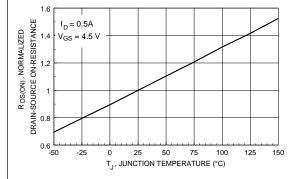


Figure 3. On-Resistance Variation with Temperature.

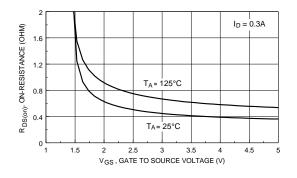


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

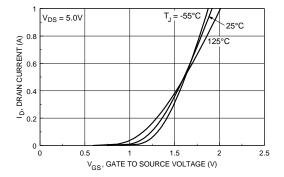


Figure 5. Transfer Characteristics.

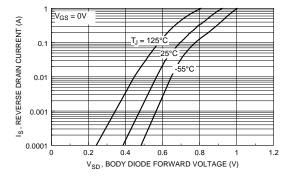


Figure 6 . Body Diode Forward Voltage
Variation with Source Current
and Temperature.

### **Typical Electrical Characteristics (continued)**

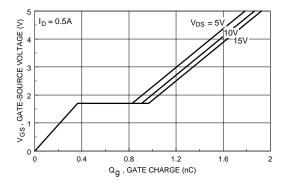


Figure 7. Gate Charge Characteristics.

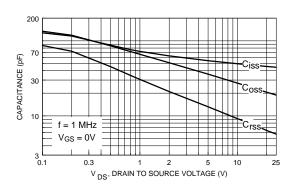


Figure 8. Capacitance Characteristics.

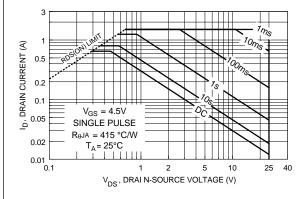


Figure 9. Maximum Safe Operating Area.

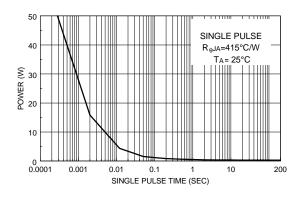


Figure 10. Single Pulse Maximum Power Dissipation.

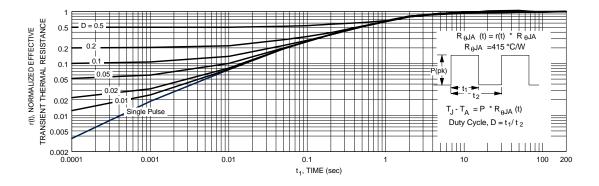


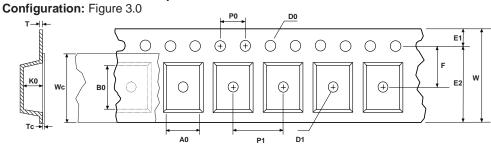
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in note 1. Transient thermal response will change depending on the circuit board design.

#### SC70-6 Tape and Reel Data and Package Dimensions FAIRCHILD SEMICONDUCTOR TM SC70-6 Packaging Configuration: Figure 1.0 Packaging Description: **Customized Label** Packaging Description: SC70-6 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 7" or 177cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 10,000 units per 13" or 330cm diameter reel. This and some other options are described in the Packaging Information table. Antistatic Cover Tape These full reels are individually barcode labeled and Inese full reels are individually barcooe aloeleed and placed inside a pizza box (illustrated in figure 1.0) made of recyclable corrugated brown paper with a Fairchild logo printing. One pizza box contains three reels maximum. And these pizza boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped. F63TNR Static Dissipative Label **Embossed Carrier Tape** 10. 11. 10 • 21 SC70-6 Packaging Information Packaging Option D87Z no flow code **SC70-6 Unit Orientation** TNR Packaging type TNR Qtv per Reel/Tube/Bag 10.000 3.000 7" Dia 13" Reel Size Box Dimension (mm) 184x187x47 343x343x64 9,000 30,000 Max qty per Box 343mm x 342mm x 64mm F63TNR Barcode Label Weight per unit (gm) 0.0055 0.0055 Intermediate box for D87Z Option Weight per Reel (kg) 0.1140 0.3960 Note/Comments F63TNR Label F63TNR Label sample 184mm x 187mm x 47mm Label Pizza Box for Standard Option D/C1: D9842 D/C2: QTY1: QTY2: N/F: F (F63TNR)3 SC70-6 Tape Leader and Trailer Configuration: Figure 2.0 0 0 0 0 0 0 0 0 $\bigcirc$ 0 0 $\bigcirc$ $\bigcirc$ $\bigcirc$ 0 0 5-----7 Carrier Tane Components Cover Tape Trailer Tape Leader Tape 300mm minimum or 500mm minimum or 75 empty pockets 125 empty pockets



# SC70-6 Embossed Carrier Tape



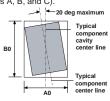
User Direction of Feed	
	⇁

Dimensions are in millimeter														
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
<b>SC70-6</b> (8mm)	2.24 +/-0.10	2.34 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.125 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.20 +/-0.10	0.255 +/-0.150	5.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

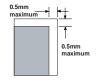


Sketch A (Side or Front Sectional View)
Component Rotation



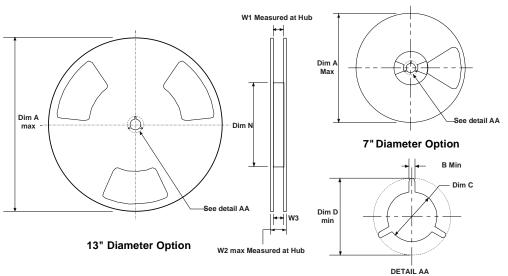
Sketch B (Top View)

Component Rotation



Sketch C (Top View)
Component lateral movement

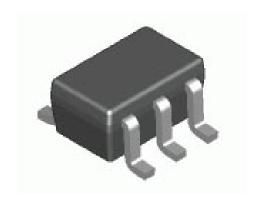
## SC70-6 Reel Configuration: Figure 4.0

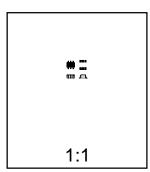


Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
8mm	7" Dia	7.00 177.8	0.059 1.5	0.512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9
8mm	13" Dia	13.00 330	0.059 1.5	0.512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9

# SC70-6 Tape and Reel Data and Package Dimensions, continued

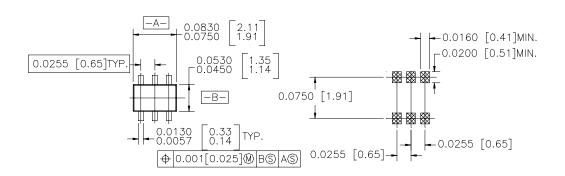
# SC70-6 (FS PKG Code 76)



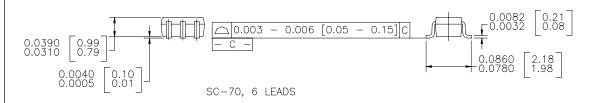


Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0055



### LAND PATTERN RECOMMENDATION



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FACT™ QFET™ FACT Quiet Series™ QS™

 $\begin{array}{lll} \mathsf{FAST}^{\circledast} & \mathsf{Quiet\,Series^{\mathsf{TM}}} \\ \mathsf{FASTr^{\mathsf{TM}}} & \mathsf{SuperSOT^{\mathsf{TM}}\text{-}3} \\ \mathsf{GTO^{\mathsf{TM}}} & \mathsf{SuperSOT^{\mathsf{TM}}\text{-}6} \\ \mathsf{HiSeC^{\mathsf{TM}}} & \mathsf{SuperSOT^{\mathsf{TM}}\text{-}8} \\ \end{array}$ 

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#### **Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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