FAIRCHILD SEMICONDUCTOR®

February 2005

# FDJ1032C
# Complementary PowerTrench® MOSFET

## Features

- **Q1** –2.8 A, –20 V. $R_{DS(ON)}$ = 160 mΩ @ $V_{GS}$ = –4.5 V
  $R_{DS(ON)}$ = 230 mΩ @ $V_{GS}$ = –2.5 V
  $R_{DS(ON)}$ = 390 mΩ @ $V_{GS}$ = –1.8 V
- **Q2** 3.2 A, 20 V. $R_{DS(ON)}$ = 90 mΩ @ $V_{GS}$ = 4.5 V
  $R_{DS(ON)}$ = 130 mΩ @ $V_{GS}$ = 2.5 V
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- FLMP SC75 package: Enhanced thermal performance in industry-standard package size

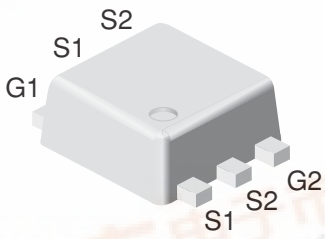
## General Description

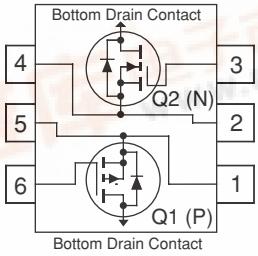
These N & P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

## Applications

- DC/DC converter
- Load switch
- Motor Driving




## Absolute Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | Q1 | Q2 | Units |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | –20 | 20 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±8 | ±12 | V |
| $I_D$ | Drain Current – Continuous | (Note 1a) | –2.8 | 3.2 | A |
| | – Pulsed | | –12 | 12 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1a) | 1.5 | | W |
| | | (Note 1b) | 0.9 | | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | | °C |
| **Thermal Characteristics** | | | | | |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 80 | | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1a) | 5 | | |

## Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|---|---|---|---|---|
| .H | FDJ1032C | 7" | 8mm | 3000 units |

## Electrical Characteristics

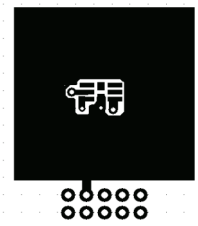
| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = –250 µA<br>$V_{GS}$ = 0 V, $I_D$ = 250 µA | Q1<br>Q2 | –20<br>20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = –250 µA, Referenced to 25°C<br>$I_D$ = 250 µA, Referenced to 25°C | Q1<br>Q2 | | –13<br>13 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = –16 V, $V_{GS}$ = 0 V<br>$V_{DS}$ = 16 V, $V_{GS}$ = 0 V | Q1<br>Q2 | | | –1<br>1 | µA |
| $I_{GSS}$ | Gate-Body Leakage | $V_{GS}$ = ±8 V, $V_{DS}$ = 0 V<br>$V_{GS}$ = ±12 V, $V_{DS}$ = 0 V | Q1<br>Q2 | | | ±100<br>±100 | nA |
| **On Characteristics** (Note 2) | | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 µA<br>$V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | Q1<br>Q2 | –0.4<br>0.6 | –0.8<br>1.0 | –1.5<br>1.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = –250 µA, Referenced to 25°C<br>$I_D$ = 250 µA, Referenced to 25°C | Q1<br>Q2 | | 3<br>–3 | | mV/°C |
| $R_{DS(on)}$ | Static Drain-Source On-Resistance | $V_{GS}$ = –4.5 V, $I_D$ = –2.8 A<br>$V_{GS}$ = –2.5 V, $I_D$ = –2.2 A<br>$V_{GS}$ = –1.8 V, $I_D$ = –1.7 A<br>$V_{GS}$ = –4.5 V, $I_D$ =2.8A, $T_J$ = 125°C | Q1 | | 108<br>163<br>283<br>150 | 160<br>230<br>390<br>238 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 3.2 A<br>$V_{GS}$ = 2.5 V, $I_D$ = 2.7 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 3.2, $T_J$ = 125°C | Q2 | | 70<br>100<br>83 | 90<br>130<br>132 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = –5 V, $I_D$ = – 2.8 A<br>$V_{DS}$ = 5 V, $I_D$ = 3.2 A | Q1<br>Q2 | | 5<br>7.5 | | S |
| **Dynamic Characteristics** | | | | | | | |
| $C_{iss}$ | Input Capacitance | Q1:<br>$V_{DS}$ = –10 V, $V_{GS}$ = 0 V, f = 1.0 MHz<br>Q2:<br>$V_{DS}$ = 10 V, $V_{GS}$ = 0 V, f = 1.0 MHz | Q1<br>Q2 | | 290<br>200 | | pF |
| $C_{oss}$ | Output Capacitance | | Q1<br>Q2 | | 55<br>50 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | Q1<br>Q2 | | 29<br>30 | | pF |
| $R_G$ | Gate Resistance | $V_{GS}$ = 15mV, f = 1.0 MHz | Q1<br>Q2 | | 18<br>10 | | Ω |
| **Switching Characteristics** | | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | Q1:<br>$V_{DD}$ = –10 V, $I_D$ = –1 A,<br>$V_{GS}$ = –4.5 V, $R_{GEN}$ = 6 Ω<br>Q2:<br>$V_{DD}$ = 10 V, $I_D$ = 1 A,<br>$V_{GS}$ = 4.5V, $R_{GEN}$ = 6 Ω | Q1<br>Q2 | | 8<br>7 | 16<br>14 | ns |
| $t_r$ | Turn-On Rise Time | | Q1<br>Q2 | | 13<br>8 | 23<br>16 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | Q1<br>Q2 | | 13<br>11 | 23<br>20 | ns |
| $t_f$ | Turn-Off Fall Time | | Q1<br>Q2 | | 18<br>2 | 32<br>4 | ns |

## Electrical Characteristics (Continued)

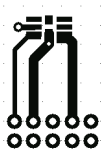
| Symbol | Parameter | Test Conditions | Type | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| $Q_g$ | Total Gate Charge | Q1:<br>$V_{DS}$ = –10 V, $I_D$ = –2.8 A, $V_{GS}$= –4.5V | Q1<br>Q2 | | 3<br>2 | 4<br>3 | nC |
| $Q_{gs}$ | Gate-Source Charge | Q2:<br>$V_{DS}$ = 10 V, $I_D$ = 3.2 A, $V_{GS}$ = 4.5 V | Q1<br>Q2 | | 0.65<br>0.4 | | nC |
| $Q_{gd}$ | Gate-Drain Charge | | Q1<br>Q2 | | 0.75<br>1.0 | | nC |
| **Drain-Source Diode Characteristics and Maximum Ratings** | | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | Q1<br>Q2 | | | –1.25<br>1.25 | A |
| $V_{SD}$ | Drain-Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = –1.3 A (Note 2)<br>$V_{GS}$ = 0 V, $I_S$ = 1.3 A (Note 2) | Q1<br>Q2 | | –0.8<br>0.8 | –1.2<br>1.2 | V |
| $t_{rr}$ | Diode Reverse Recovery Time | $I_F$ = –4.2A, $d_{IF}/d_t$ = 100 A/µs<br>$I_F$ = 5.9A, $d_{IF}/d_t$ = 100 A/µs | Q1<br>Q2 | | 14<br>11 | | nS |
| $Q_{rr}$ | Diode Reverse Recovery Charge | $I_F$ = –4.2A, $d_{IF}/d_t$ = 100 A/µs<br>$I_F$ = 5.9A, $d_{IF}/d_t$ = 100 A/µs | Q1<br>Q2 | | 4<br>2.5 | | nC |

**Notes:**

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 80°C/W when mounted on a $1in^2$ pad of 2 oz copper (Single Operation).



b) 140°C/W when mounted on a minimum pad of 2 oz copper (Single Operation).

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

## Typical Characteristics : Q1

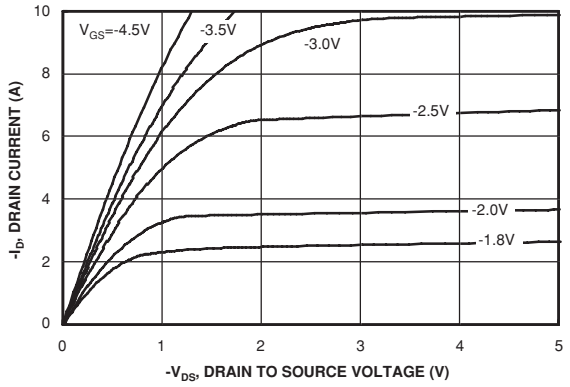



**Figure 1. On-Region Characteristics.**

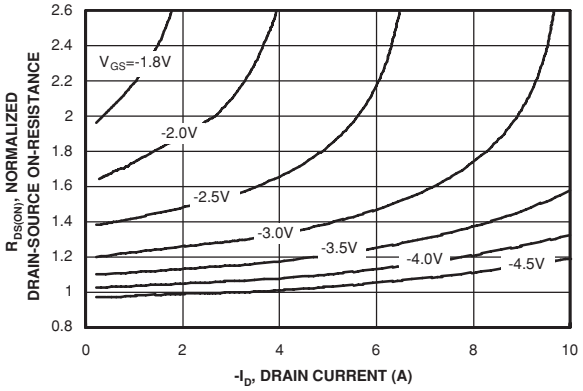



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

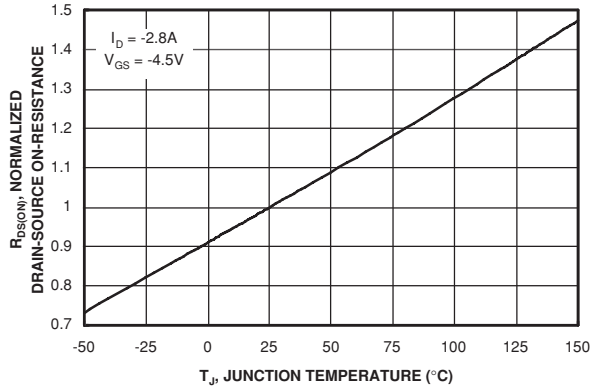



**Figure 3. On-Resistance Variation with Temperature.**

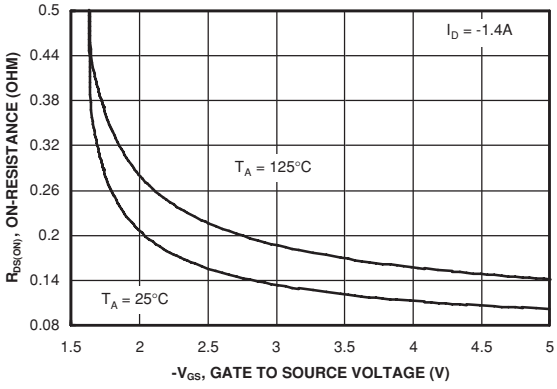



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

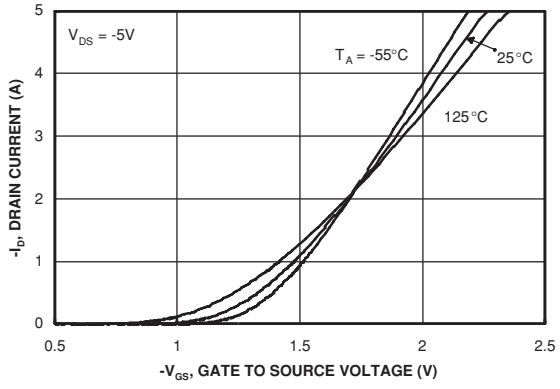



**Figure 5. Transfer Characteristics.**

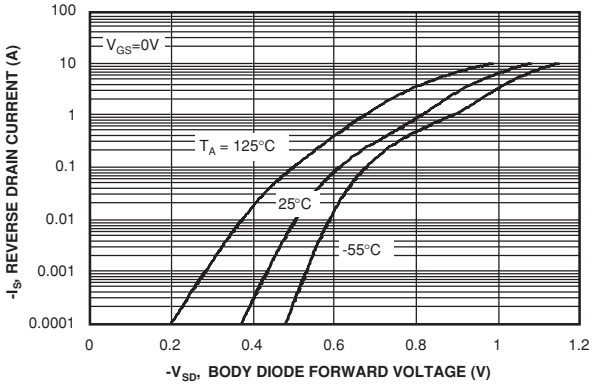



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics : Q1

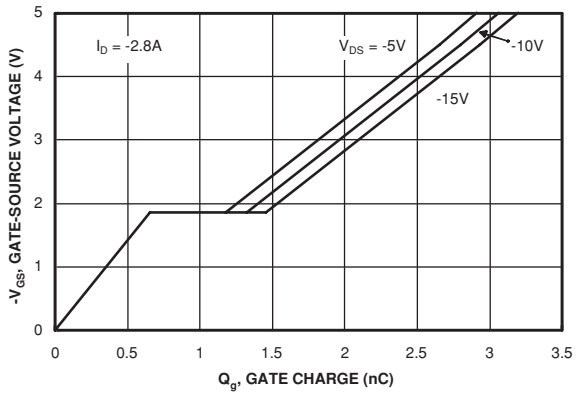



Figure 7. Gate Charge Characteristics.

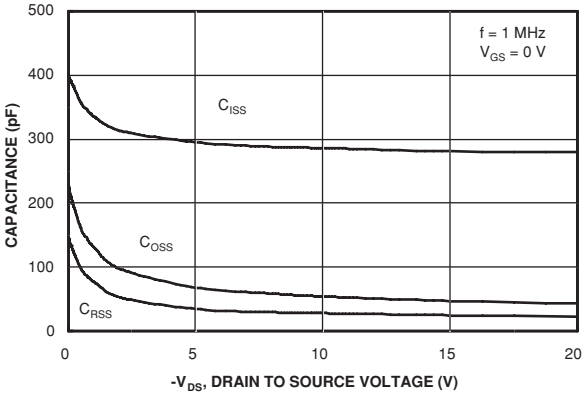



Figure 8. Capacitance Characteristics.

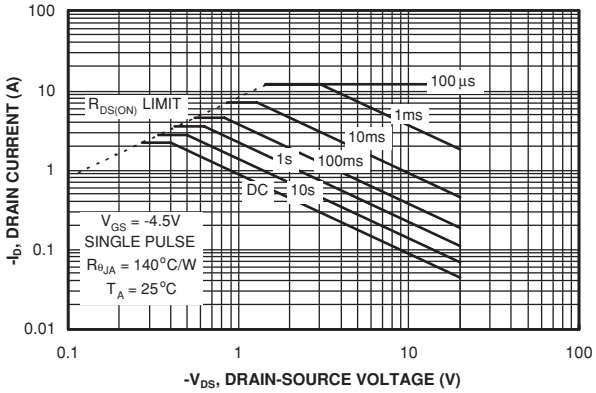



Figure 9. Maximum Safe Operating Area.

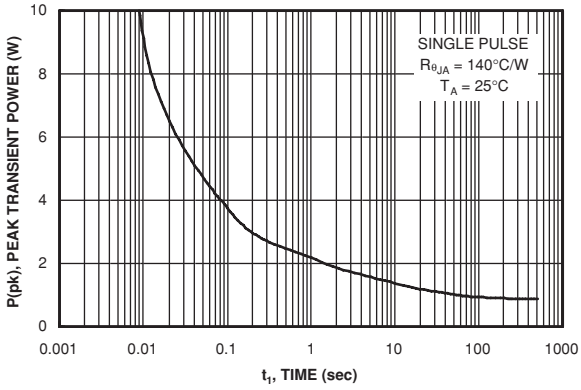



Figure 10. Single Pulse Maximum Power Dissipation.

## Typical Characteristics : Q2

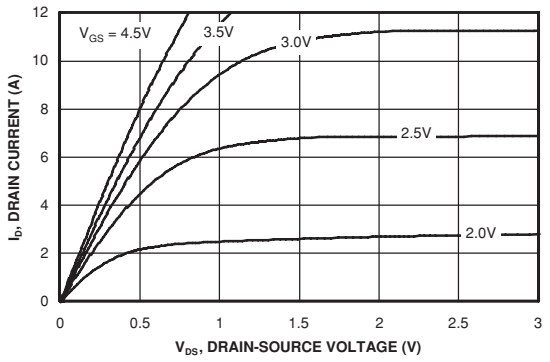



**Figure 11. On-Region Characteristics.**

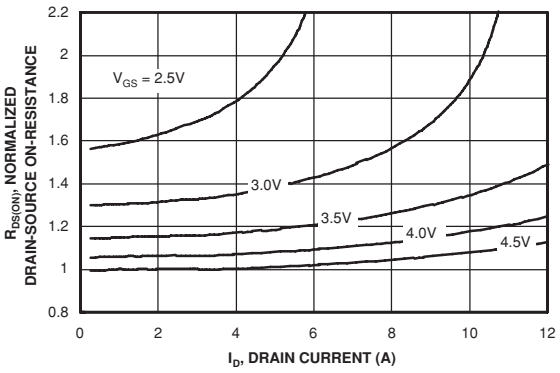



**Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.**

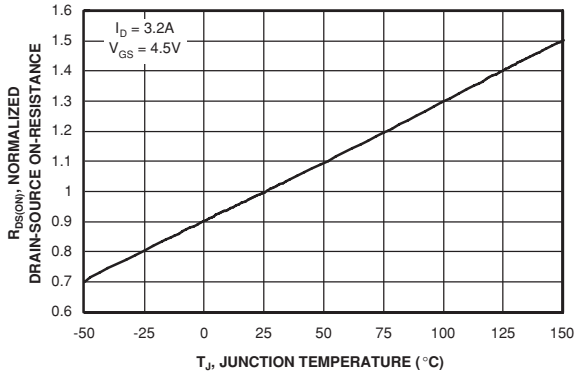



**Figure 13. On-Resistance Variation with Temperature.**

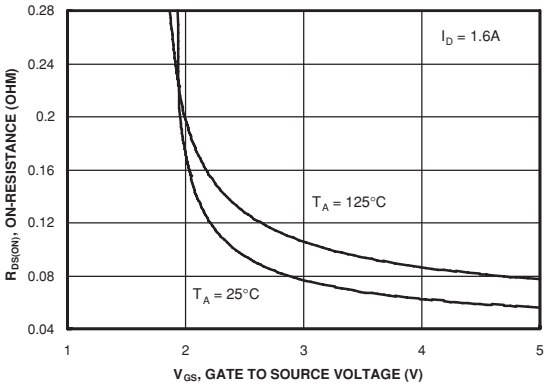



**Figure 14. On-Resistance Variation with Gate-to-Source Voltage.**

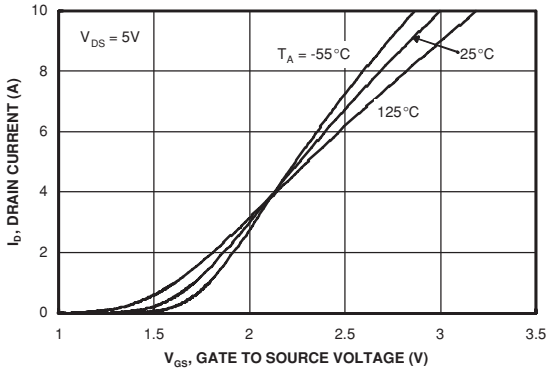



**Figure 15. Transfer Characteristics.**

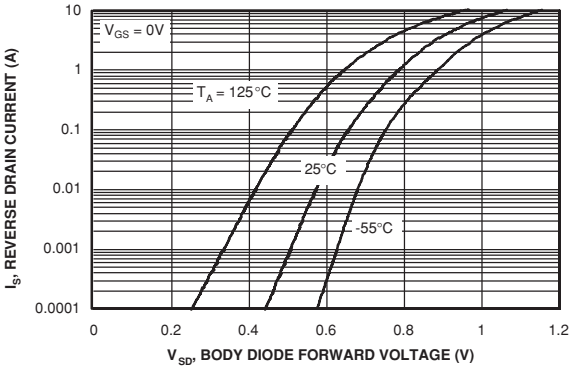



**Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics : Q2

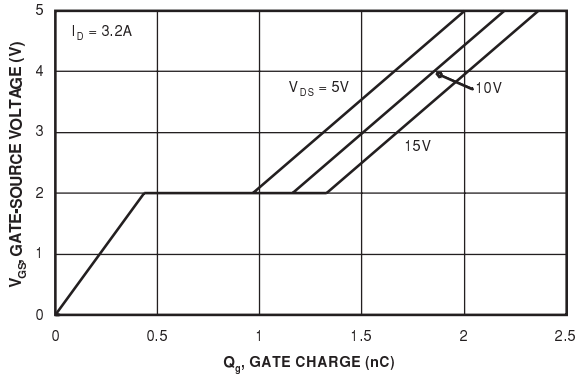



Figure 17. Gate Charge Characteristics.

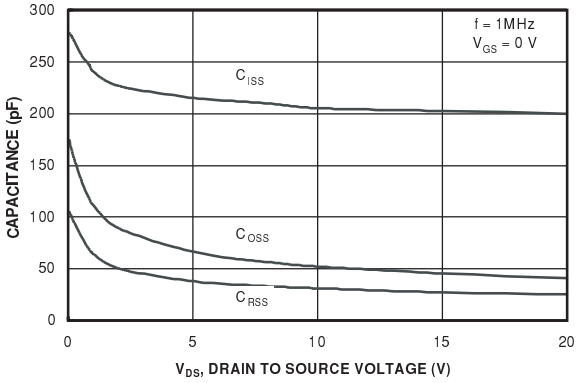



Figure 18. Capacitance Characteristics.

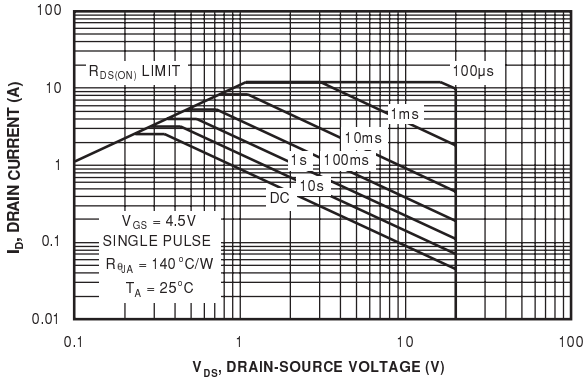



Figure 19. Maximum Safe Operating Area.

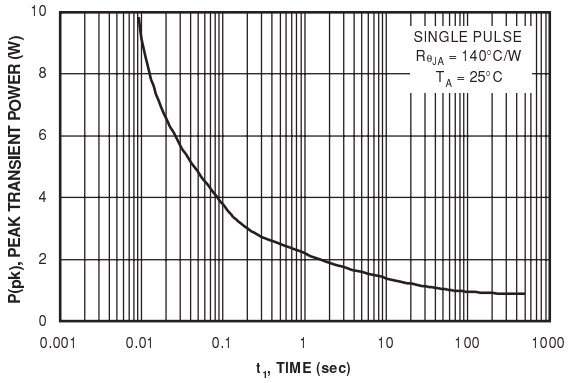



Figure 20. Single Pulse Maximum Power Dissipation.

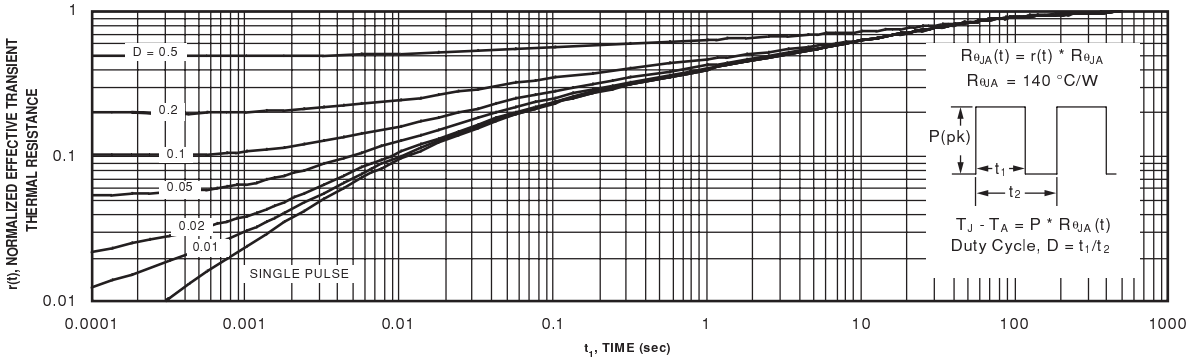
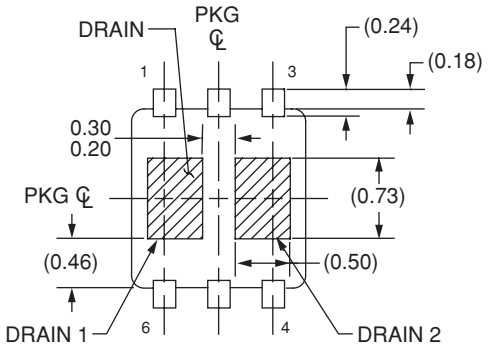


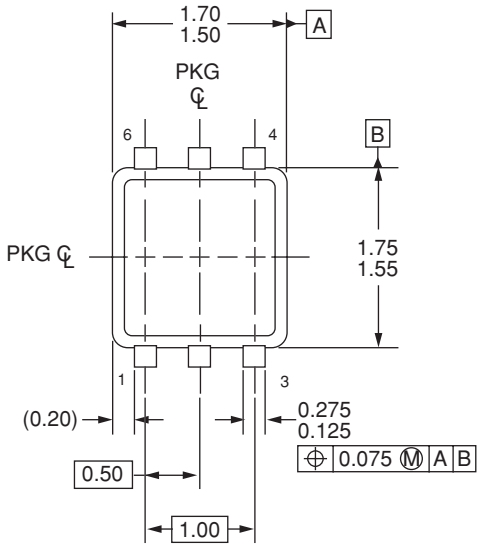

Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

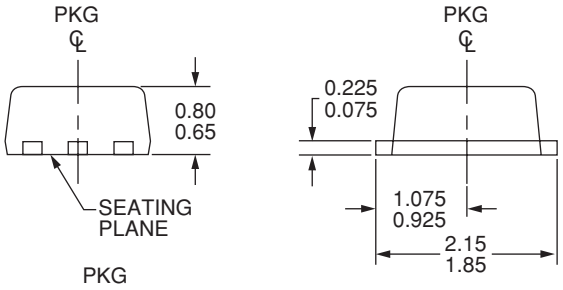
## Dimensional Outline and Pad Layout

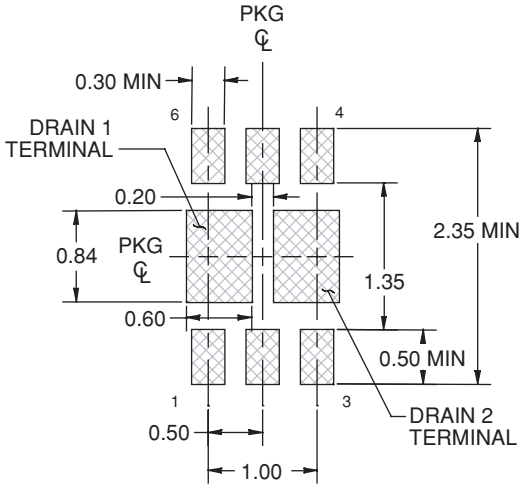



**Bottom View**




**Top View**




**Recommended Landing Pattern**

Notes: Unless otherwise specified all dimensions are in millimeters.

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| ActiveArray™ | FASTr™ | ISOPLANAR™ | Power247™ | Stealth™ |
| Bottomless™ | FPS™ | LittleFET™ | PowerEdge™ | SuperFET™ |
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| *CROSSVOLT*™ | GlobalOptoisolator™ | MicroFET™ | PowerTrench® | SuperSOT™-6 |
| DOME™ | GTO™ | MicroPak™ | QFET® | SuperSOT™-8 |
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| E²CMOS™ | I²C™ | MSX™ | QT Optoelectronics™ | TinyLogic® |
| EnSigna™ | *i-Lo*™ | MSXPro™ | Quiet Series™ | TINYOPTO™ |
| FACT™ | ImpliedDisconnect™ | OCX™ | RapidConfigure™ | TruTranslation™ |
| FACT Quiet Series™ | | OCXPro™ | RapidConnect™ | UHC™ |
| Across the board. Around the world.™ | | OPTOLOGIC® | µSerDes™ | UltraFET® |
| The Power Franchise® | | OPTOPLANAR™ | SILENT SWITCHER® | UniFET™ |
| Programmable Active Droop™ | | PACMAN™ | SMART START™ | VCX™ |

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

### PRODUCT STATUS DEFINITIONS

**Definition of Terms**

| Datasheet Identification | Product Status | Definition |
|---|---|---|
| Advance Information | Formative or In Design | This datasheet contains the design specifications for product development. Specifications may change in any manner without notice. |
| Preliminary | First Production | This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
| No Identification Needed | Full Production | This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design. |
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