



November 1999  
ADVANCE INFORMATION

# FDZ201N

## N-Channel 2.5V Specified PowerTrench™ BGA MOSFET

### General Description

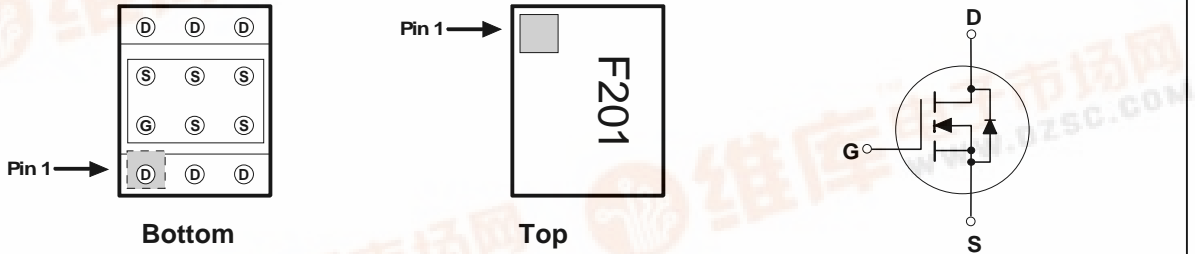
Combining Fairchild's advanced 2.5V specified PowerTrench process with state of the art BGA packaging, the FDZ201N minimizes both PCB space and  $R_{DS(ON)}$ . This BGA MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultra-low profile packaging, low gate charge, and low  $R_{DS(ON)}$ .

### Applications

- Battery management
- Load switch
- Battery protection

### Features

- 9 A, 20 V.  $R_{DS(ON)} = 0.018 \Omega @ V_{GS} = 4.5 V$   
 $R_{DS(ON)} = 0.030 \Omega @ V_{GS} = 2.5 V$ .
- Occupies only 5 mm<sup>2</sup> of PCB area. Only 55% of the area of SSOT-6
- Ultra-thin package: less than 0.70 mm height when mounted to PCB
- Outstanding thermal transfer characteristics: 4 times better than SSOT-6
- Ultra-low  $Q_g \times R_{DS(ON)}$  figure-of-merit.
- High power and current handling capability.



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage	20	V
V <sub>GSS</sub>	Gate-Source Voltage	±12	V
I <sub>D</sub>	Drain Current – Continuous (Note 1a)	9	A
	– Pulsed	20	
P <sub>D</sub>	Power Dissipation (Steady State) (Note 1a)	2.7	W
T <sub>J</sub> , T <sub>stg</sub>	Operating and Storage Junction Temperature Range	-55 to +175	°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	55	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	12	°C/W

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
F201	FDZ201N	TBD	TBD	TBD



**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		14		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage Current, Forward	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate–Body Leakage Current, Reverse	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
<b>On Characteristics (Note 2)</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.4	0.9	1.5	V
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 9\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 6.5\text{ A}$			0.018 0.030	$\Omega$
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain–Source Diode Forward Current				2.3	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.3\text{ A}$ (Note 2)		0.77	1.2	V

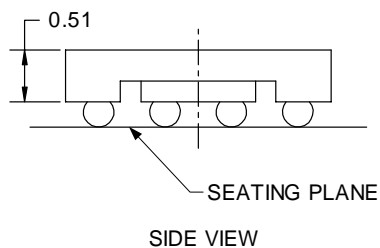
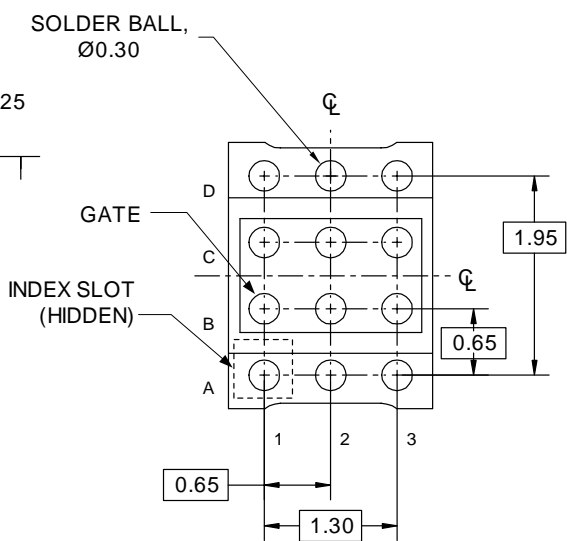
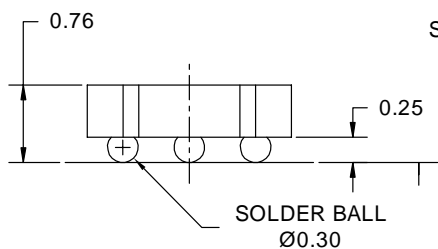
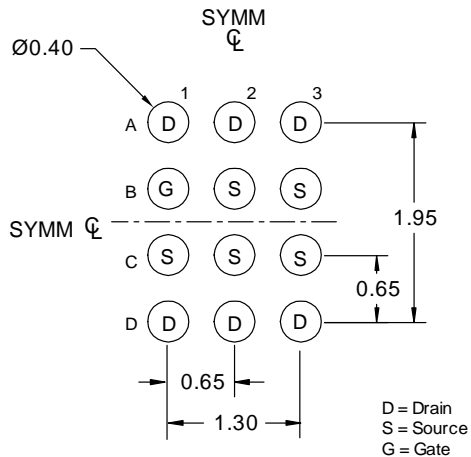
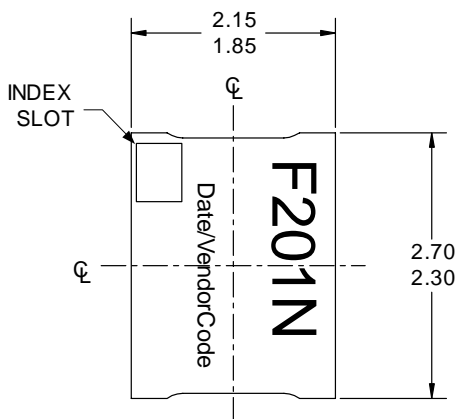
**Notes:**

- $R_{\theta JA}$  is a function of the junction-to-case ( $R_{\theta JC}$ ), case-to-ambient ( $R_{\theta CA}$ ) and the PC Board ( $R_{\theta BA}$ ) thermal resistance where the case thermal reference is defined the top surface of the package.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  and  $R_{\theta BA}$  are determined by the user's design.

(a).  $R_{\theta JA} = 55^\circ\text{C/W}$  (steady-state) when mounted on 1 in<sup>2</sup> of 2 oz. copper.

- Pulse Test: Pulse Width < 300 $\mu\text{s}$ , Duty Cycle < 2.0%

**Dimensional Outline and Pad Layout**



NOTES: UNLESS OTHERWISE SPECIFIED

- A) ALL DIMENSIONS ARE IN MILLIMETERS.
- B) NO JEDEC REGISTRATION REFERENCE AS OF JULY 1999.

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FACT™	QFET™	
FACT Quiet Series™	QS™	
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FASTr™	SuperSOT™-3	
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