FAIRCHILD SEMICONDUCTOR®

December 2004

FDZ7064AS
30V N-Channel PowerTrench® SyncFET™ BGA MOSFET

Features

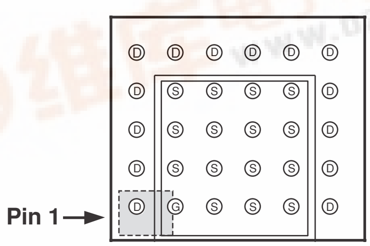
- 13.5 A, 30 V. $R_{DS(ON)}$ = 5.6 mΩ @ V_{GS} = 10 V
  $R_{DS(ON)}$ = 7.1 mΩ @ V_{GS} = 4.5 V
- Occupies only 14 mm^2 of PCB area. Only 42% of the area of SO-8
- Ultra-thin package: less than 0.76 mm height when mounted to PCB
- 3.5 x 4 mm^2 Footprint
- High power and current handling capability.

Applications

- DC/DC converters

General Description

This MOSFET is designed to replace a single MOSFET and parallel Schottky diode in synchronous DC:DC power supplies. Combining Fairchild's 30V PowerTrench SyncFET process with state of the art BGA packaging, the FDZ7064AS minimizes both PCB space and $R_{DS(ON)}$. This BGA SyncFET embodies a breakthrough in both packaging and power MOSFET integration which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultra-low profile packaging, low gate charge, ultra-low reverse recovery charge and low $R_{DS(ON)}$.



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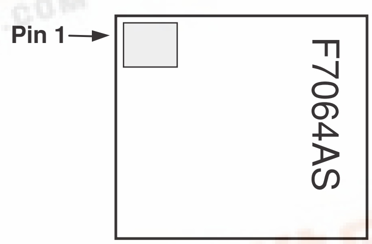

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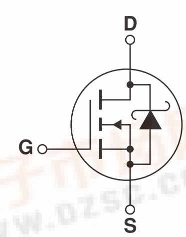


Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain-Source Voltage		30	V
V_{GSS}	Gate-Source Voltage		±20	V
I_D	Drain Current	– Continuous (Note 1a)	13.5	A
		– Pulsed	60	
P_D	Power Dissipation (Steady State) (Note 1a)		2.2	W
T_J, T_{stg}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	56	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Ball (Note 1)	4.5	
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	0.6	

Package Marking and Ordering Information

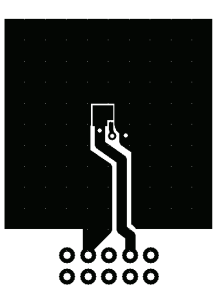
Device Marking	Device	Reel Size	Tape width	Quantity
7064AS	FDZ7064AS	13"	12mm	3000

Electrical Characteristics T_A = 25˚C unless otherwise noted

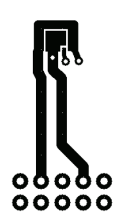
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1mA	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 10mA, Referenced to 25°C		25		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V			500	uA
I_{GSS}	Gate–Body Leakage	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1mA	1	1.4	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 10mA, Referenced to 25°C		–0.3		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 13.5 A V_{GS} = 4.5 V, I_D = 12 A V_{GS}=10 V, I_D=13.5A, T_J =125°C		4.6 5.7 5.9	5.6 7.1 7.4	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = 10 V,V_{DS} = 5 V	60			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 13.5 A		61		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1.0 MHz		1960		pF
C_{oss}	Output Capacitance			570		pF
C_{rss}	Reverse Transfer Capacitance			210		pF
R_G	Gate Resistance	V_{GS} = 15 mV, I_D = 6 A		1.4		W
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DS} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		9	18	nS
t_r	Turn–On Rise Time			12	22	nS
$t_{d(off)}$	Turn–Off Delay Time			39	62	nS
t_f	Turn–Off Fall Time			18	33	nS
$Q_{g(TOT)}$	Total Gate Charge, Vgs = 10V	V_{DS} = 15 V, I_D = 13.5A		36	51	nC
Q_g	Total Gate Charge, Vgs = 5V			20	28	nC
Q_{gs}	Gate–Source Charge			5		nC
Q_{gd}	Gate–Drain Charge			6		nC
Drain–Source Diode Characteristics						
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 3.2 A (Note 1)		0.4	0.7	V
t_{rr}	Diode Reverse Recovery Time	I_F = 13.5 A, d_{iF}/d_t = 300 A/µs See Diode Characteristic, page 5		23		nS
Q_{rr}	Diode Reverse Recovery Charge			21		nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 2 oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. The thermal resistance from the junction to the circuit board side of the solder ball, $R_{\theta JB}$, is defined for reference. For $R_{\theta JC}$, the thermal reference point for the case is defined as the top surface of the copper chip carrier. $R_{\theta JC}$ and $R_{\theta JB}$ are guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a) 56˚C/W when mounted on a 1in^2 pad of 2 oz copper



b) 119˚C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

Typical Characteristics

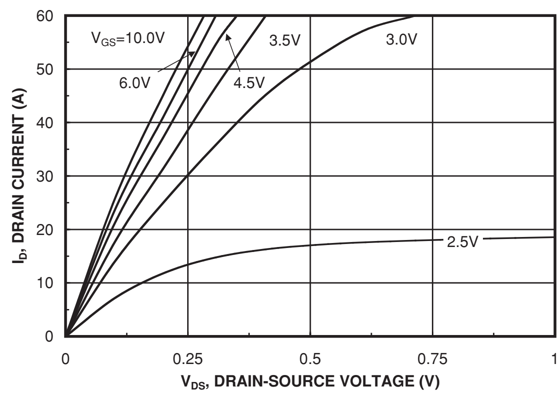


Figure 1. On-Region Characteristics.

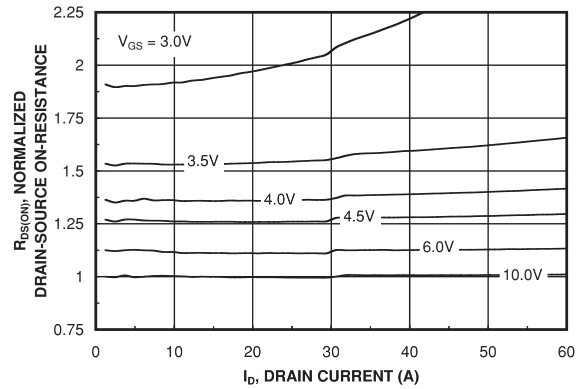


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

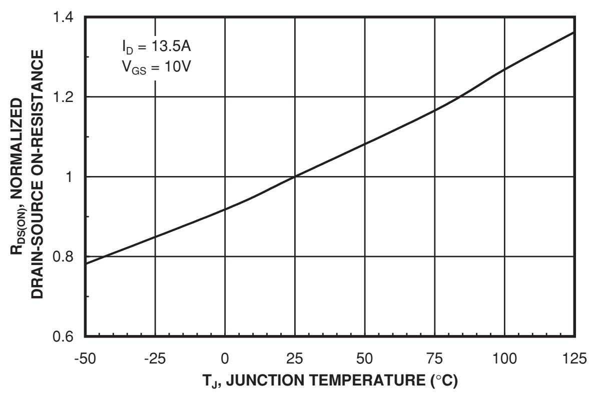


Figure 3. On-Resistance Variation with Temperature.

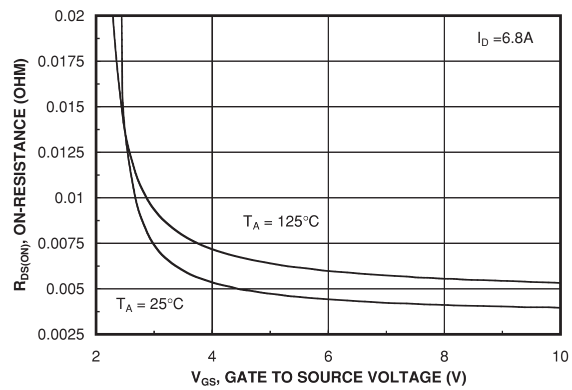


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

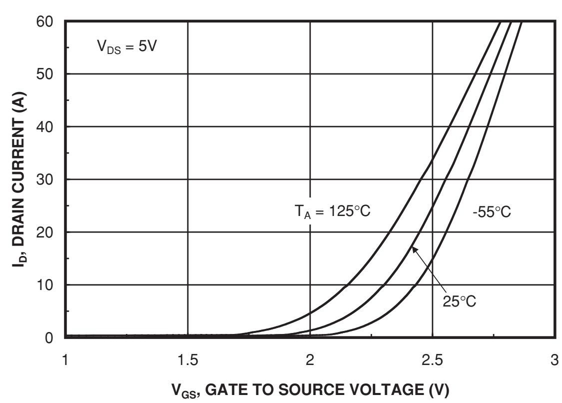


Figure 5. Transfer Characteristics.

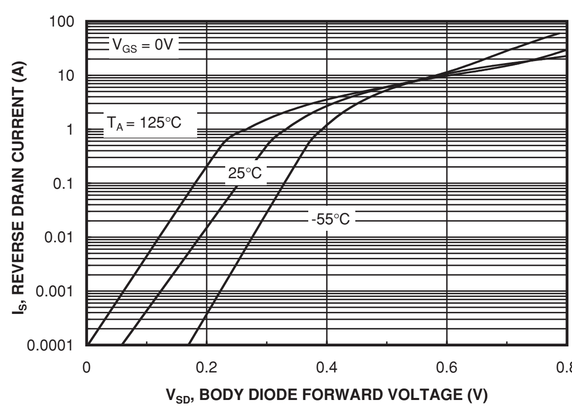


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

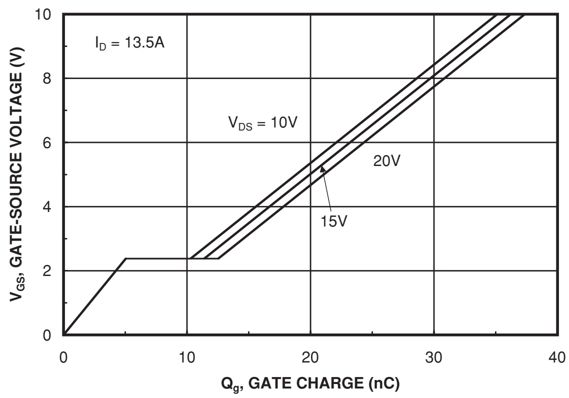


Figure 7. Gate Charge Characteristics.

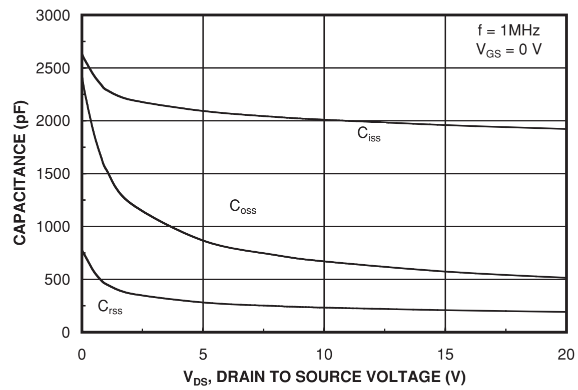


Figure 8. Capacitance Characteristics.

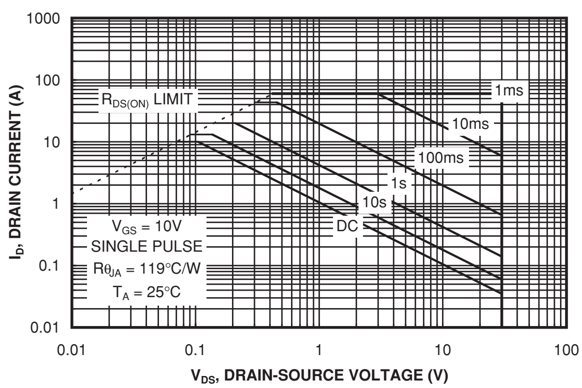


Figure 9. Maximum Safe Operating Area.

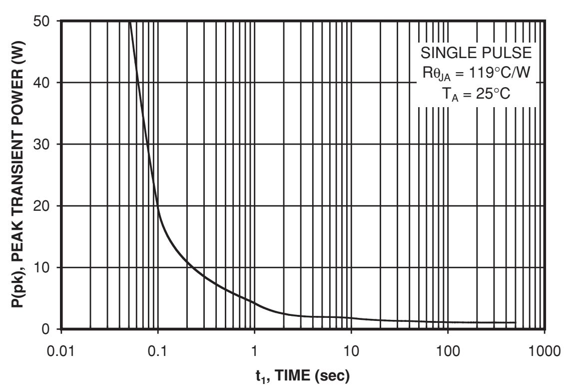


Figure 10. Single Pulse Maximum Power Dissipation.

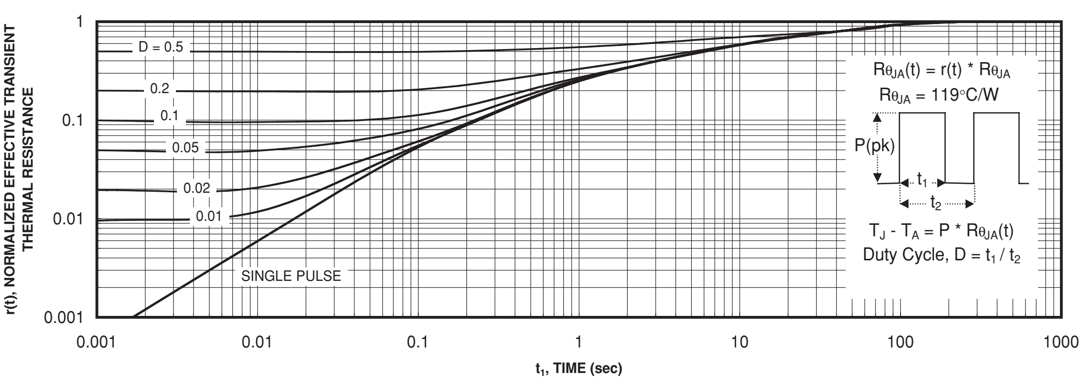


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.

Typical Characteristics

SyncFET Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 12 FDZ7064AS.

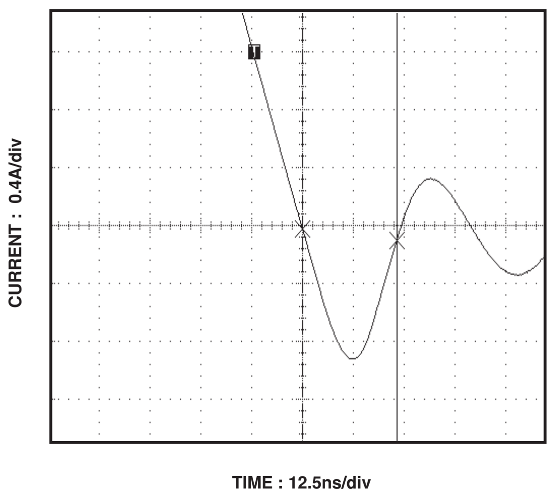


Figure 12. FDZ7064AS SyncFET body diode reverse recovery characteristic.

For comparison purposes, Figure 13 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET .

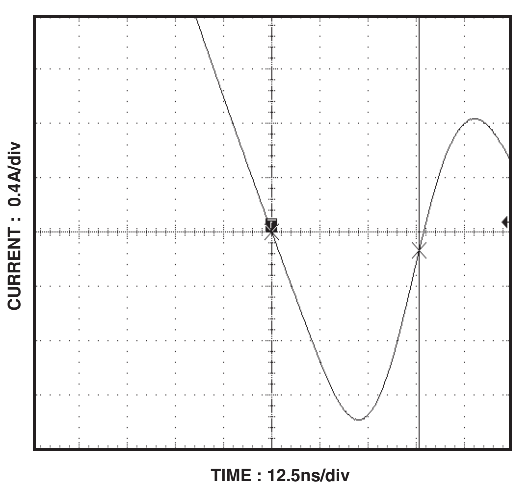


Figure 13. Non-SyncFET (FDZ7064N) body diode reverse recovery characteristic.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

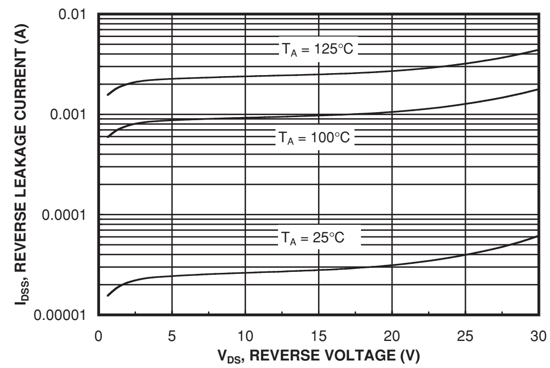
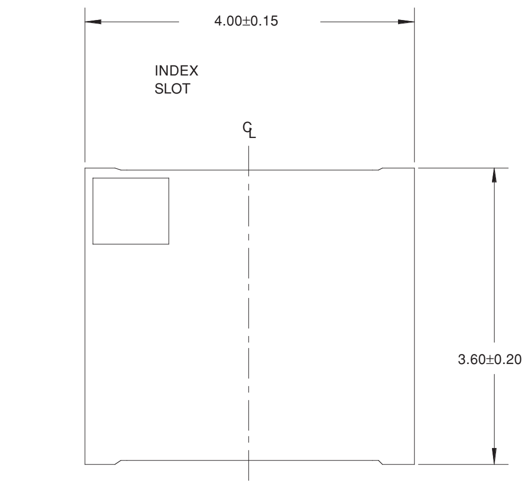
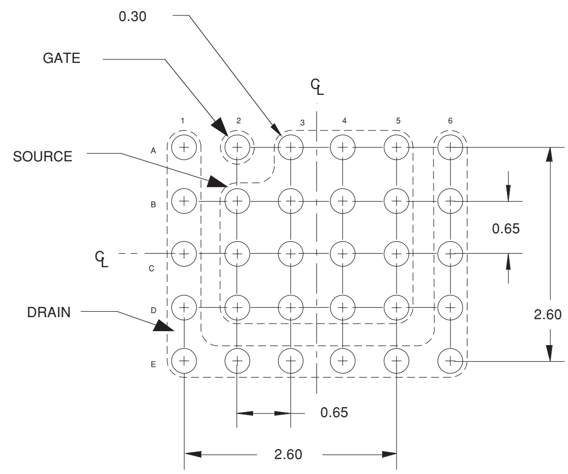


Figure 14. SyncFET diode reverse leakage versus drain-source voltage and temperature.

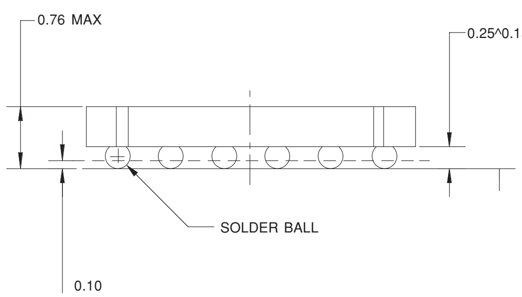
Dimensional Outline and Pad Layout



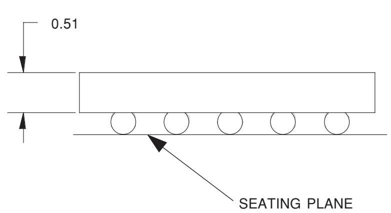
TOP VIEW



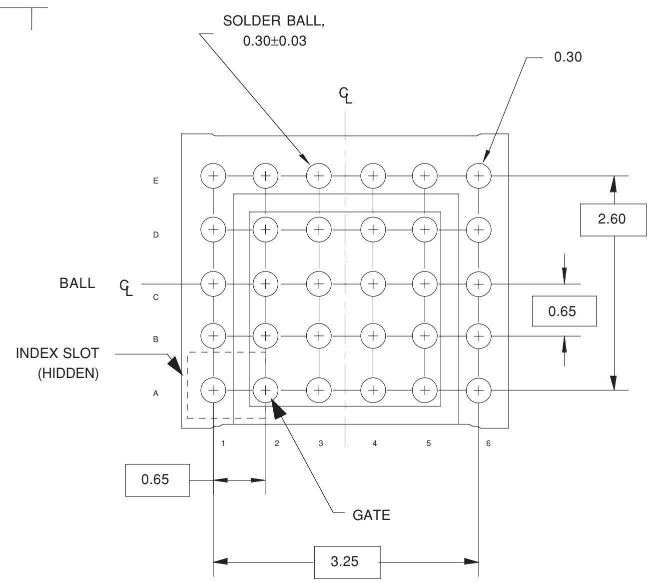
LAND PATTERN
RECOMMENDATION



FRONT VIEW



SIDE VIEW



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) NO JEDEC REGISTRATION REFERENCE AS OF JULY 1999.

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Rev. I14