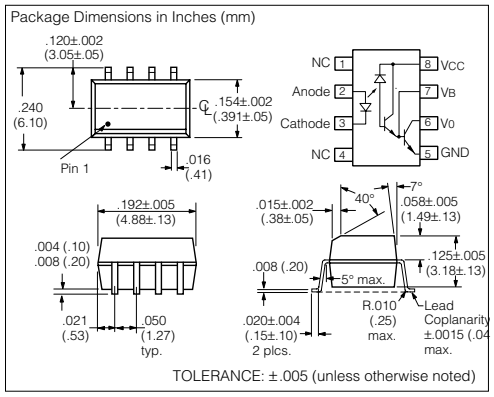
SIEMENS

NEW

SFH6318T
SFH6319T

LOW CURRENT, HIGH GAIN OPTOCOUPLER



FEATURES

- **Industry Standard SOIC-8 Surface Mountable Package**
- **High Current Transfer Ratio, 800%**
- **Low Input Current, 0.5mA**
- **High Output Current, 60mA**
- **Isolation Test Voltage, 2500 VAC_{RMS}**
- **TTL Compatible Output, V_{OL}=0.1 V**
- **Adjustable Bandwidth-Access to Base**
- **Underwriters Lab File #E52744**
- **Available in Tape and Reel (suffix T)**

APPLICATIONS

- **Logic Ground Isolation-TTL/TTL, TTL/CMOS, CMOS/CMOS, CMOS/TTL**
- **EIA RS 232C Line Receiver**
- **Low Input Current Line Receiver-Long Lines, Party Lines**
- **Telephone Ring Detector**
- **117 VAC Line Voltage Status Indication-Low Input Power Dissipation**
- **Low Power Systems-Ground Isolation**

DESCRIPTION

Very high current ratio together with 2500 VAC isolation are achieved by coupling an LED with an integrated high gain photodetector in a SOIC-8 package. Separate pins for the photodiode and output stage enable TTL compatible saturation voltages with high speed operation. Photodarlington operation is achieved by tying the VCC and VO terminals together. Access to the base terminal allows adjustment to the gain bandwidth.

The SFH6318T is ideal for TTL applications since the 300% minimum current transfer ratio with an LED current of 1.6 mA enables operation with one unit load-in and one unit load-out with a 2.2 KΩ pull-up resistor.

The SFH6319T is best suited for low power logic applications involving CMOS and low power TTL. A 400% current transfer ratio with only 0.5 mA of LED current is guaranteed from 0°C to 70°C.

Caution:
Due to the small geometries of this device, it should be handled with Electrostatic Discharge (ESD) precautions. Proper grounding would prevent damage further and/or degradation which may be induced by ESD.

Maximum Ratings (25°)

Emitter

Reverse Input Voltage ..... 3 V
Supply and Output Voltage, V_{CC} (pin 8-5), V_O (pin 6-5)
SFH6318T ..... –0.5 to 7 V
SFH6319T ..... –0.5 to 18 V
Input Power Dissipation ..... 35 mW
Derate Linearly above 50°C
Free Air Temperature ..... 0.7 mW/°C
Average Input Current ..... 20 mA
Peak Input Current ..... 40 mA
(50% Duty Cycle-1 ms pulse width)
Peak Transient Input Current
(tp≤1 µsec, 300 pps) ..... 1.0 A

Detector (Si Photodiode + Photodarlington)

Output Current I_O (pin 6) ..... 60 mA
Emitter-Base Reverse Voltage (pin 5-7) ..... 0.5 V
Output Power Dissipation ..... 150 mW
Derate Linearly from 25°C ..... 2 mW/°C

Package

Storage Temperature ..... –55°C to +125°C
Operating Temperature ..... –40°C to +85°C
Lead Soldering Temperature (t=10 sec.) ..... 260°C
Junction Temperature ..... 100°C
Ambient Temperature Range ..... –55°C to +100°C
IsolationTest Voltage between
Emitter and Detector ..... 2500 VAC_{RMS}
(refer to climate DIN 40046, part 2, Nov. 74)
Pollution Degree (DIN VDE 0110) 2
Creepage Distance ..... ≥4 mm
Clearance ..... ≥4 mm
Comparative Tracking Index
per DIN IEC 112/VDE 0303, part 1 175
Isolation Resistance
V_{IO}=500 V, T_A=25°C R_{ISOL} ..... $\geq 10^{12}\Omega$
V_{IO}=500 V, T_A=100°C R_{ISOL} ..... $\geq 10^{11}\Omega$

Electro-Optical Characteristics (T_A=0°C to 70°C, T_A=25°C-Typical, unless otherwise specified)

Parameter	Symbol	Device	Min	Typ	Max	Units	Test Conditions	Note
Current Transfer Ratio	CTR	SFH6318T	300	1600	2600	%	I_F=1.6 mA, V_O=0.4 V, V_{CC}=4.5 V	1,2
		SFH6319T	400 500	1600 2000	2600 3500	%	I_F=0.5 mA, V_O=0.4 V, V_{CC}=4.5 V I_F=1.6 mA, V_O=0.4 V, V_{CC}=4.5 V	1,2
Logic Low Output Voltage	V_{OL}	SFH6318T		0.1	0.4	V	I_F=1.6 mA, I_O=4.8 mA, V_{CC}=4.5 V	2
		SFH6319T		0.1 0.15 0.25	0.4 0.4 0.4	V	I_F=1.6 mA, I_O=8 mA, V_{CC}=4.5 V I_F=5 mA, I_O=15 mA, V_{CC}=4.5 V I_F=12 mA, I_O=24 mA, V_{CC}=4.5 V	2
Logic High Output Current	I_{OH}	SFH6318T		0.1	250	µA	I_F=0 mA, V_O=V_{CC}=7 V	2
		SFH6319T		0.05	100	µA	I_F=0 mA, V_O=V_{CC}=18 V	2
Logic Low Supply Current	I_{CCL}			0.2	1.5	mA	I_F=1.6 mA, V_O=OPEN, V_{CC}=18 V	2
Logic High Supply Current	I_{CCH}			0.01	10	µA	I_F=0 mA, V_O=OPEN, V_{CC}=18 V	2
Input Forward Voltage	V_F			1.4	1.7	V	I_F=1.6 mA, T_A=25°C	
Temperature Coefficient, Forward Voltage	$\Delta V_F/\Delta T_A$			–1.8		mV/°C	I_F=1.6 mA	
Input Capacitance	C_{IN}			25		pF	f=1 MHz, V_F=0	
Resistance (Input-Output)	R_{I-O}			10^{12} 10^{11}		Ω Ω	V_{IO}=500 VDC, T_A=25°C V_{IO}=500 VDC, T_A=100°C	3
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f=1 MHz	3

Switching Specifications (T_A=25°C)

Parameter	Symbol	Device	Min	Typ	Max	Units	Test Conditions	Note
Propagation Delay Time To Logic Low at Output	t_{PHL}	SFH6318T		2	10	µs	I_F=1.6 mA, R_L=2.2 KΩ	
		SFH6319T		6 0.6	25 1	µs	I_F=0.5 mA, R_L=4.7 KΩ I_F=12 mA, R_L=270 Ω	2,4
Propagation Delay Time To Logic High at Output	t_{PLH}	SFH6318T		2	35	µs	I_F=1.6 mA, R_L=2.2 KΩ	
		SFH6319T		4 1.5	60 7	µs	I_F=0.5 mA, R_L=4.7 KΩ I_F=12 mA, R_L=270 Ω	2,4
Common Mode Transient Immunity at Logic High Level Output	$\lvert CM_H \rvert$			1 K		V/µs	I_F=0 mA, R_L=2.2 KΩ V_{CM}=10 V_{p-p}	5,6
Common Mode Transient Immunity at Logic Low Level Output	$\lvert CM_L \rvert$			1 K		V/µs	I_F=1.6 mA, R_L=2.2 KΩ V_{CM}=10 V_{p-p}	5,6

Notes
1. DC current transfer ratio is defined as the ratio of outpput collector current, I_O, to the forward LED input current, I_F times 100%.
2. Pin 7 open.
3. Device considered a two-terminal device: pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.
4. Using a resistor between pin 5 and 7 will decrease gain and delay time.
5. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the commo-mode pulse, V_{CM}, to assure that the output will remain in a logic high state (i.e. V_O>2.0 V) common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode puse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e. V_O<0.8 V).
6. In applications where dv/dt may exceed 50,000 V/µs (such as state discharge) a series resistor, R_{CC} should be included to protect IC from destructively high surge currents. The recommended value is $R_{CC} \cong \frac{IV}{0.15\ I_F(mA)}$ kΩ. Refer to Figure 2.

Figure 1. Switching test circuit

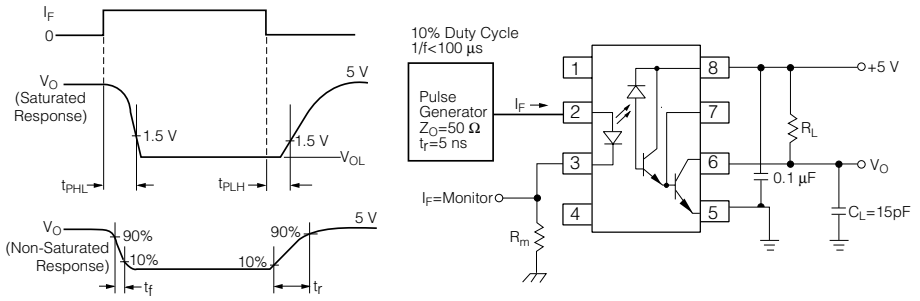


Figure 2. Test circuit for transient immunity and typical waveforms