



4, 8 MEG x 32
DRAM SODIMMs

SMALL-OUTLINE DRAM MODULE

MT2LDT432H (X)(S), MT4LDT832H (X)(S)

For the latest data sheet, please refer to the Micron Web site: www.micronsemi.com/datasheets/datasheet.html

FEATURES

- JEDEC pinout in a 72-pin, small-outline, dual in-line memory module (SODIMM)
- 16MB (4 Meg x 32) and 32MB (8 Meg x 32)
- High-performance CMOS silicon-gate process
- Single +3.3V \pm 0.3V power supply
- All inputs, outputs and clocks are TTL-compatible
- 4,096-cycle CAS#-BEFORE-RAS# (CBR) refresh distributed across 64ms
- FAST PAGE MODE (FPM) or Extended Data-Out (EDO) PAGE MODE access cycles
- Optional self refresh (S) for low-power data retention

OPTIONS

- Package
72-pin SODIMM (gold)
- Timing
50ns access
60ns access
- Access Cycles
FAST PAGE MODE
EDO PAGE MODE
- Refresh Rates
Standard Refresh
Self Refresh (128ms period)

MARKING

G

-5

-6

None

X

None

S

PART NUMBERS

EDO Operating Mode

PART NUMBER	CONFIGURATION	REFRESH
MT2LDT432HG-xX	4 Meg x 32	Standard
MT2LDT432HG-xXS	4 Meg x 32	Self
MT4LDT832HG-xX	8 Meg x 32	Standard
MT4LDT832HG-xXS	8 Meg x 32	Self

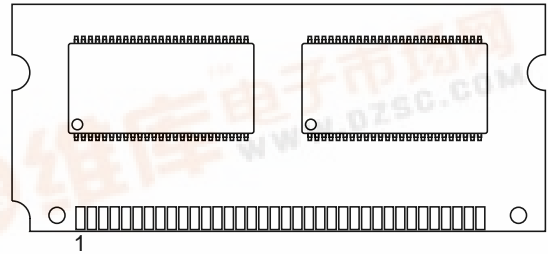
x = speed

FPM Operating Mode

PART NUMBER	CONFIGURATION	REFRESH
MT2LDT432HG-x	4 Meg x 32	Standard
MT2LDT432HG-xS	4 Meg x 32	Self
MT4LDT832HG-x	8 Meg x 32	Standard
MT4LDT832HG-xS	8 Meg x 32	Self

PIN ASSIGNMENT (Front View)

72-Pin Small-Outline DIMM



PIN	FRONT	PIN	BACK	PIN	FRONT	PIN	BACK
1	V _{SS}	2	DQ0	37	DQ16	38	DQ17
3	DQ1	4	DQ2	39	V _{SS}	40	CAS0#
5	DQ3	6	DQ4	41	CAS2#	42	CAS3#
7	DQ5	8	DQ6	43	CAS1#	44	RAS0#
9	DQ7	10	V _{DD}	45	NC/RAS1#*	46	NC (A12)
11	PRD1	12	A0	47	WE#	48	NC (A13)
13	A1	14	A2	49	DQ18	50	DQ19
15	A3	16	A4	51	DQ20	52	DQ21
17	A5	18	A6	53	DQ22	54	DQ23
19	A10	20	NC	55	NC	56	DQ24
21	DQ8	22	DQ9	57	DQ25	58	DQ26
23	DQ10	24	DQ11	59	DQ28	60	DQ27
25	DQ12	26	DQ13	61	V _{DD}	62	DQ29
27	DQ14	28	A7	63	DQ30	64	DQ31
29	A11	30	V _{DD}	65	NC	66	PRD2
31	A8	32	A9	67	PRD3	68	PRD4
33	NC/RAS3#*	34	RAS2#	69	PRD5	70	PRD6
35	DQ15	36	NC	71	PRD7	72	V _{SS}

*32MB version only

NOTE: Symbols in parentheses are not used on these modules but may be used for other modules in this product family. They are for reference only.

KEY TIMING PARAMETERS

EDO Operating Mode

SPEED	t _{RC}	t _{RAC}	t _{PC}	t _{AA}	t _{CAC}	t _{CAS}
-5	84ns	50ns	20ns	25ns	13ns	8ns
-6	104ns	60ns	25ns	30ns	15ns	10ns

FPM Operating Mode

SPEED	t _{RC}	t _{RAC}	t _{PC}	t _{AA}	t _{CAC}	t _{RP}
-5	90ns	50ns	30ns	25ns	13ns	30ns
-6	110ns	60ns	35ns	30ns	15ns	40ns



GENERAL DESCRIPTION

The MT2LDT432H (X)(S) and MT4LDT832H (X)(S) are randomly accessed 16MB and 32MB memories organized in a small-outline x32 configuration. They are specially processed to operate from 3V to 3.6V for low-voltage memory systems.

During READ or WRITE cycles, each bit is uniquely addressed through the address bits, which are entered 12 bits (A0-A11) at a time. RAS# is used to latch the first 12 bits and CAS# the latter 10 bits.

READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates read mode, while a logic LOW on WE# dictates write mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. If WE# goes LOW prior to CAS# going LOW, the output pin(s) remain open (High-Z) until the next CAS# cycle.

FAST PAGE MODE

FAST-PAGE-MODE operations allow faster data operations (READ or WRITE) within a row-address-defined page boundary. The FAST-PAGE-MODE cycle is always initiated with a row address strobed in by RAS#, followed by a column address strobed in by CAS#. Additional columns may be accessed by providing valid column addresses, strobing CAS# and holding RAS# LOW, thus executing faster memory cycles. Returning RAS# HIGH terminates the FAST-PAGE-MODE operation.

EDO PAGE MODE

EDO PAGE MODE, designated by the "X" version, is an accelerated FAST-PAGE-MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# goes back HIGH. EDO provides for CAS# precharge time (t_{CP}) to occur without the output data going invalid. This elimination of CAS# output control provides for pipelined READs.

FAST-PAGE-MODE modules have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO operates as any DRAM READ or

FAST-PAGE-MODE READ, except data will be held valid or become valid after CAS# goes HIGH, as long as RAS# and OE# are held LOW. (Refer to the 4 Meg x 16 [MT4LC4M16R6] DRAM data sheet for additional information on EDO functionality.)

REFRESH

Memory cell data is retained in its correct state by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS#-ONLY, CBR or HIDDEN) so that all combinations of RAS# addresses are executed at least every t_{REF} , regardless of sequence. The CBR REFRESH cycle will invoke the internal refresh counter for automatic RAS# addressing.

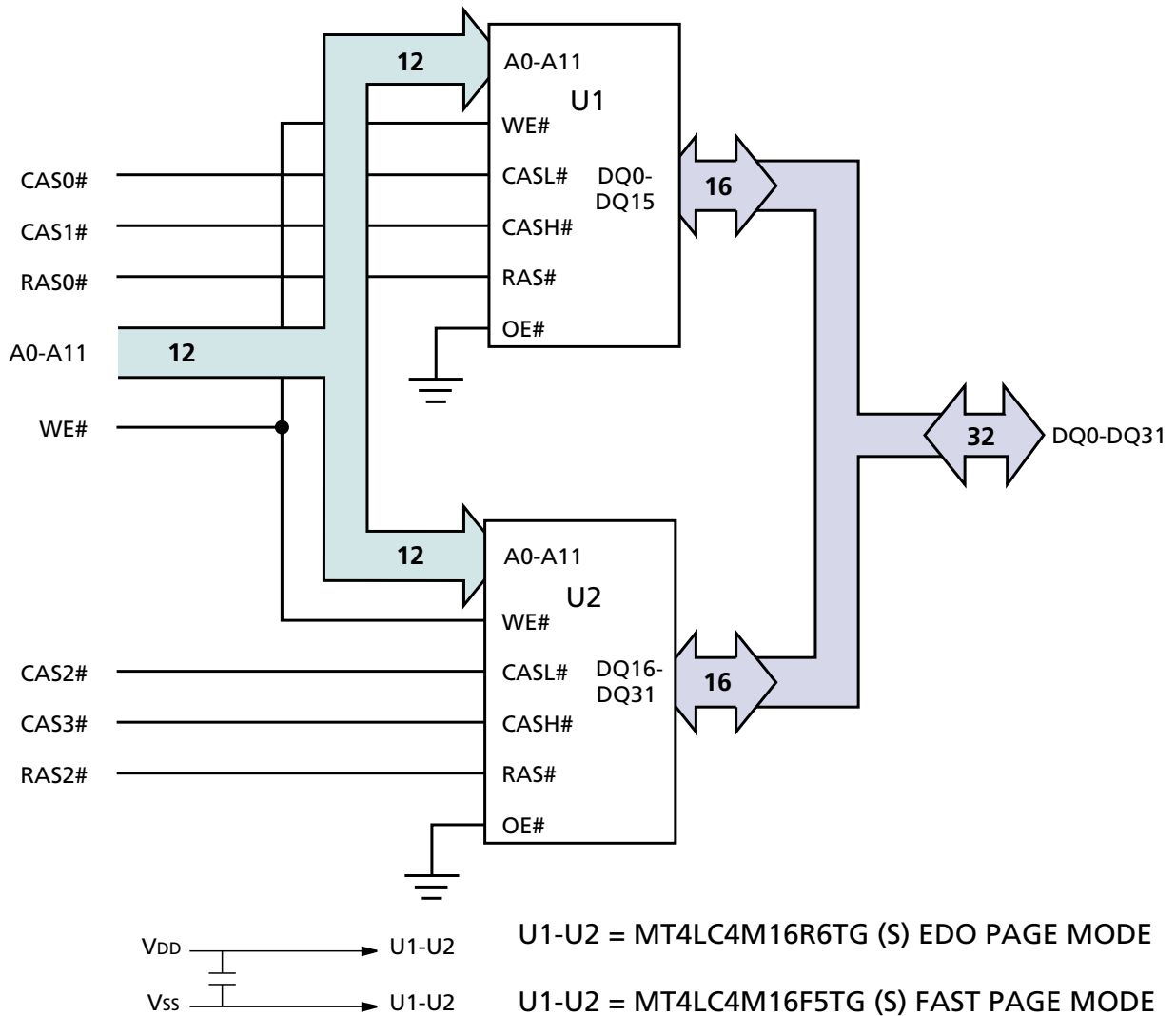
An optional self refresh mode is also available. The "S" option allows the user the choice of a fully static, low-power data retention mode or a dynamic refresh mode at the extended refresh period of 128ms. The optional self refresh feature is initiated by performing a CBR REFRESH cycle and holding RAS# LOW for the specified t_{RASS} .

The self refresh mode is terminated by driving RAS# HIGH for a minimum time of t_{RPS} . This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting self refresh. However, if the DRAM controller utilizes a RAS#-ONLY or burst refresh sequence, all rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

STANDBY

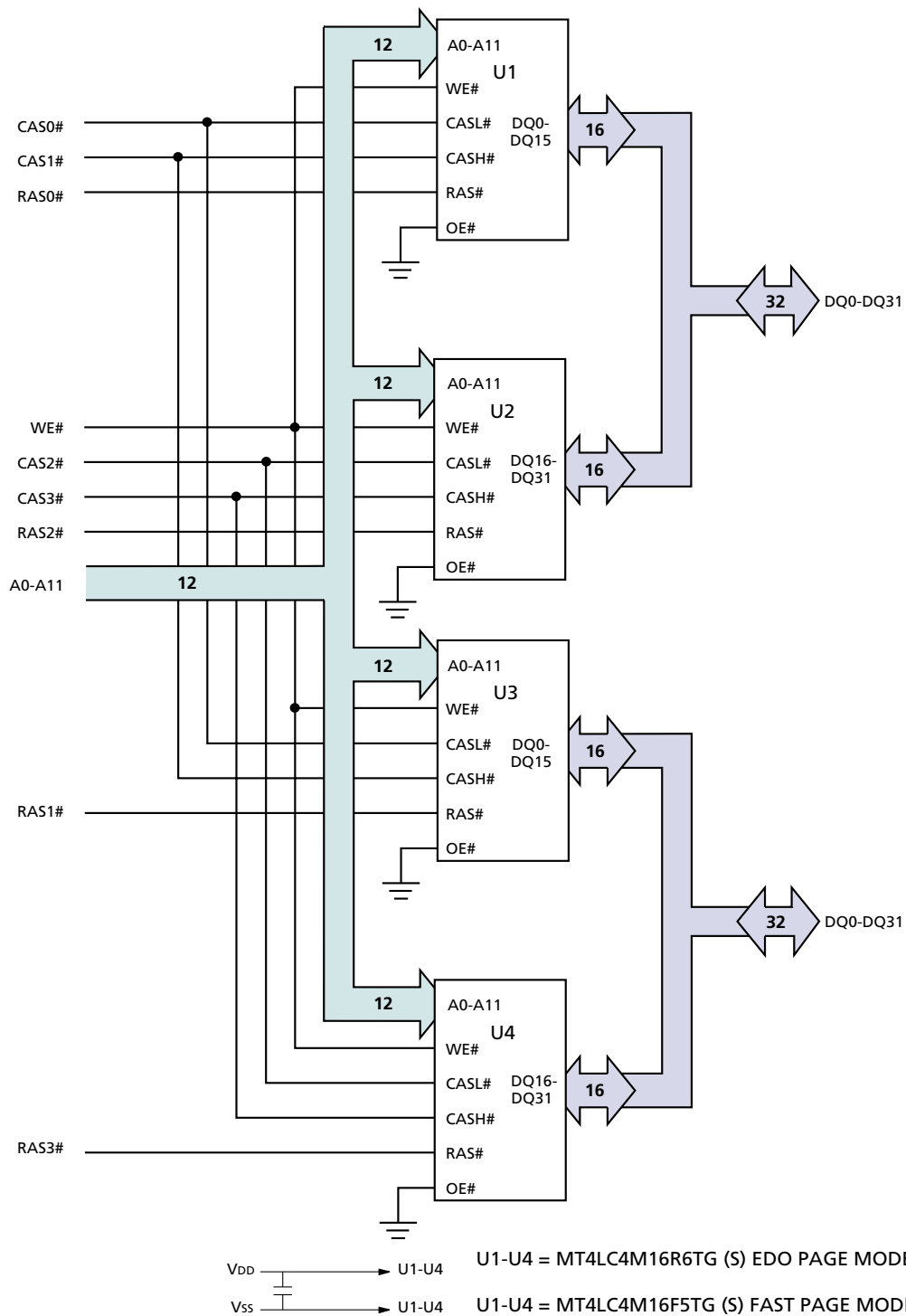
Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS# HIGH time.

**FUNCTIONAL BLOCK DIAGRAM
MT2LDT432H (X)(S) (16MB)**





**FUNCTIONAL BLOCK DIAGRAM
MT4LDT832H (X)(S) (32MB)**





**JEDEC-DEFINED
PRESENCE-DETECT – MT2LDT432H (X)(S) (16MB)**

SYMBOL	PIN	-5	-6
PRD1	11	NC	NC
PRD2	66	NC	NC
PRD3	67	V _{SS}	V _{SS}
PRD4	68	NC	NC
PRD5	69	V _{SS}	NC
PRD6	70	V _{SS}	NC
PRD7	71	X*	X*

**JEDEC-DEFINED
PRESENCE-DETECT – MT4LDT832H (X)(S) (32MB)**

SYMBOL	PIN	-5	-6
PRD1	11	NC	NC
PRD2	66	NC	NC
PRD3	67	V _{SS}	V _{SS}
PRD4	68	V _{SS}	V _{SS}
PRD5	69	V _{SS}	NC
PRD6	70	V _{SS}	NC
PRD7	71	X*	X*

*X = NC (Normal Refresh) or V_{SS} (Self Refresh)

**ABSOLUTE MAXIMUM RATINGS***Voltage on V_{DD} SupplyRelative to V_{SS} -1V to +4.6V

Voltage on Inputs or I/O Pins

Relative to V_{SS} -1V to +4.6VOperating Temperature, T_A (ambient) .. 0°C to +70°C

Storage Temperature (plastic) -55°C to +125°C

Power Dissipation 4W

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS(Notes: 1) (V_{DD} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MIN	MAX	UNITS	NOTES	
SUPPLY VOLTAGE	V _{DD}	ALL	3	3.6	V		
INPUT HIGH VOLTAGE: Valid Logic 1; All inputs	V _{IH}	ALL	2	V _{DD} + 0.3	V	26	
INPUT LOW VOLTAGE: Valid Logic 0; All inputs	V _{IL}	ALL	-0.3	0.8	V	26	
INPUT LEAKAGE CURRENT: Any input at V _{IN} (0V ≤ V _{IN} ≤ V _{DD} + 0.3V); All other pins not under test = 0V	CAS0#-CAS3#	I _{IL1}	16MB 32MB	-2 -4	2 4	μA	
	A0-A11, WE#	I _{I2}	16MB 32MB	-4 -8	4 8	μA	
	RAS0#-RAS3#	I _{I3}	16MB 32MB	-2 -2	2 2	μA	
OUTPUT LEAKAGE CURRENT: DQ is disabled; 0V ≤ V _{OUT} ≤ V _{DD} + 0.3V	DQ0-DQ31	I _{OZ}	16MB 32MB	-5 -10	5 10	μA	
OUTPUT LEVELS: Output High Voltage (I _{OUT} = -2mA) Output Low Voltage (I _{OUT} = 2mA)	V _{OH}	ALL	2.4	-	V		
	V _{OL}	ALL	-	0.4	V		



FAST PAGE MODE AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 19) ($V_{DD} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-5		-6		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX		
Access time from column address	t_{AA}		25		30	ns	
Column-address hold time (referenced to RAS#)	t_{AR}	40		45		ns	
Column-address setup time	t_{ASC}	0		0		ns	
Row-address setup time	t_{ASR}	0		0		ns	
Access time from CAS#	t_{CAC}		13		15	ns	
Column-address hold time	t_{CAH}	8		10		ns	
CAS# pulse width	t_{CAS}	13	10,000	15	10,000	ns	
CAS# LOW to "Don't Care" during Self Refresh	t_{CHD}	15		15		ns	25
CAS# hold time (CBR Refresh)	t_{CHR}	15		15		ns	4
CAS# to output in Low-Z	t_{CLZ}	3		3		ns	21
CAS# precharge time (FAST PAGE MODE)	t_{CP}	8		10		ns	13
Access time from CAS# precharge	t_{CPA}		30		35	ns	
CAS# to RAS# precharge time	t_{CRP}	5		5		ns	
CAS# hold time	t_{CSH}	50		60		ns	
CAS# setup time (CBR Refresh)	t_{CSR}	5		5		ns	4
WRITE command to CAS# lead time	t_{CWL}	13		15		ns	
Data-in hold time	t_{DH}	8		10		ns	18
Data-in setup time	t_{DS}	0		0		ns	18
Output buffer turn-off delay	t_{OFF}	3	13	3	15	ns	17, 21, 23
OE# setup prior to RAS# during HIDDEN REFRESH cycle	t_{ORD}	0		0		ns	
FAST-PAGE-MODE READ or WRITE cycle time	t_{PC}	30		35		ns	
Access time from RAS#	t_{RAC}		50		60	ns	
RAS# to column-address delay time	t_{RAD}	13		15		ns	15



FAST PAGE MODE AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 19) ($V_{DD} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - FAST PAGE MODE OPTION		-5		-6			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	UNITS	NOTES
Row-address hold time	t_{RAH}	8		10		ns	
RAS# pulse width	t_{RAS}	50	10,000	60	10,000	ns	
RAS# pulse width (Self Refresh)	t_{RASS}	100		100		μs	25
RAS# pulse width (FAST PAGE MODE)	t_{RASP}	50	125,000	60	125,000	ns	
Random READ or WRITE cycle time	t_{RC}	90		110		ns	
RAS# to CAS# delay time	t_{RCD}	18		20		ns	14
READ command hold time (referenced to CAS#)	t_{RCH}	0		0		ns	16
READ command setup time	t_{RCS}	0		0		ns	
Refresh period (4,096 cycles)	t_{REF}		64		64	ms	
Refresh period "S" version	t_{REF}		128		128	ms	25
RAS# precharge time	t_{RP}	30		40		ns	
RAS# to CAS# precharge time	t_{RPC}	0		0		ns	
RAS# precharge time (Self Refresh)	t_{RPS}	90		105		ns	25
READ command hold time (referenced to RAS#)	t_{RRH}	0		0		ns	16
RAS# hold time	t_{RSH}	13		15		ns	
WRITE command to RAS# lead time	t_{RWL}	13		15		ns	
Transition time (rise or fall)	t_T	2	50	2	50	ns	
WRITE command hold time	t_{WCH}	8		10		ns	
WRITE command hold time (referenced to RAS#)	t_{WCR}	40		45		ns	
WE# command setup time	t_{WCS}	0		0		ns	
WRITE command pulse width	t_{WCP}	8		10		ns	
WE# hold time (CBR Refresh)	t_{WRH}	10		10		ns	
WE# setup time (CBR Refresh)	t_{WRP}	10		10		ns	



EDO PAGE MODE AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 19) ($V_{DD} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX		
Access time from column address	t_{AA}		25		30	ns	
Column-address setup to CAS# precharge	t_{ACH}	12		15		ns	
Column-address hold time (referenced to RAS#)	t_{AR}	38		45		ns	
Column-address setup time	t_{ASC}	0		0		ns	
Row-address setup time	t_{ASR}	0		0		ns	
Access time from CAS#	t_{CAC}		13		15	ns	
Column-address hold time	t_{CAH}	8		10		ns	
CAS# pulse width	t_{CAS}	8	10,000	10	10,000	ns	
CAS# LOW to "Don't Care" during Self Refresh	t_{CHD}	15		15		ns	25
CAS# hold time (CBR Refresh)	t_{CHR}	8		10		ns	4
CAS# to output in Low-Z	t_{CLZ}	0		0		ns	
Data output hold after next CAS# LOW	t_{COH}	3		3		ns	
CAS# precharge time	t_{CP}	8		10		ns	13
Access time from CAS# precharge	t_{CPA}		28		35	ns	
CAS# to RAS# precharge time	t_{CRP}	5		5		ns	
CAS# hold time	t_{CSH}	38		45		ns	
CAS# setup time (CBR Refresh)	t_{CSR}	5		5		ns	4
WRITE command to CAS# lead time	t_{CWL}	8		10		ns	
Data-in hold time	t_{DH}	8		10		ns	18
Data-in setup time	t_{DS}	0		0		ns	18
Output buffer turn-off delay	t_{OFF}	0	12	0	15	ns	17, 23
EDO-PAGE-MODE READ or WRITE cycle time	t_{PC}	20		25		ns	
Access time from RAS#	t_{RAC}		50		60	ns	
RAS# to column-address delay time	t_{RAD}	9		12		ns	15
Row-address hold time	t_{RAH}	9		10		ns	
RAS# pulse width	t_{RAS}	50	10,000	60	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	t_{RASP}	50	125,000	60	125,000	ns	
RAS# pulse width during Self Refresh	t_{RASS}	100		100		μs	25
Random READ or WRITE cycle time	t_{RC}	84		104		ns	
RAS# to CAS# delay time	t_{RCD}	11		14		ns	14



EDO PAGE MODE AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 10, 11, 12, 19) ($V_{DD} = +3.3V \pm 0.3V$)

AC CHARACTERISTICS - EDO PAGE MODE OPTION		-5		-6		UNITS	NOTES
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX		
READ command hold time (referenced to CAS#)	t_{RCH}	0		0		ns	16
READ command setup time	t_{RCS}	0		0		ns	
Refresh period (4,096 cycles)	t_{REF}		64		64	ms	
Refresh period "S" version	t_{REF}		128		128	ms	25
RAS# precharge time	t_{RP}	30		40		ns	
RAS# to CAS# precharge time	t_{RPC}	5		5		ns	
RAS# precharge time exiting Self Refresh	t_{RPS}	90		105		ns	25
READ command hold time (referenced to RAS#)	t_{RRH}	0		0		ns	16
RAS# hold time	t_{RSH}	13		15		ns	
WRITE command to RAS# lead time	t_{RWL}	13		15		ns	
Transition time (rise or fall)	t_T	2	50	2	50	ns	
WRITE command hold time	t_{WCH}	8		10		ns	
WRITE command hold time (referenced to RAS#)	t_{WCR}	38		45		ns	
WE# command setup time	t_{WCS}	0		0		ns	
Output disable delay from WE#	t_{WHZ}	0	12	0	15	ns	
WRITE command pulse width	t_{WP}	5		5		ns	
WE# pulse to disable at CAS# HIGH	t_{WPZ}	10		10		ns	
WE# hold time (CBR Refresh)	t_{WRH}	8		10		ns	
WE# setup time (CBR Refresh)	t_{WRP}	8		10		ns	

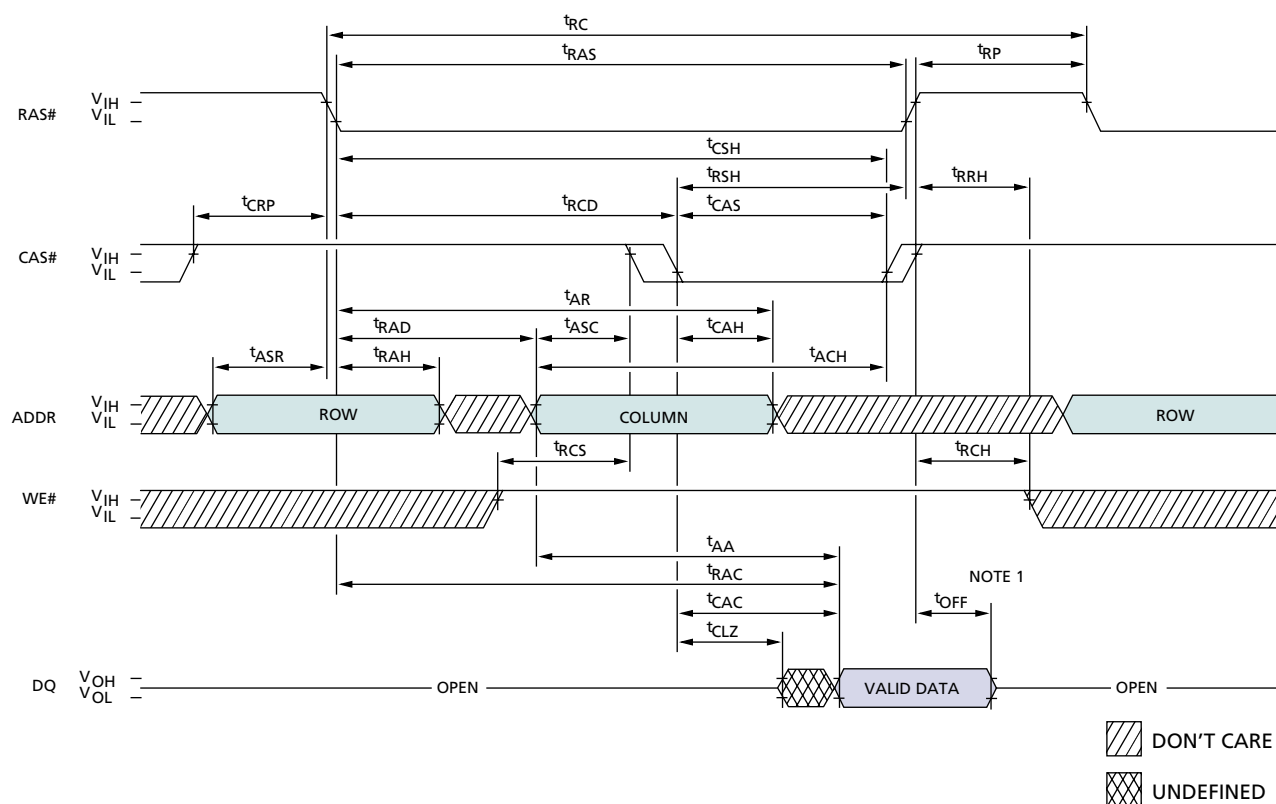


NOTES

1. All voltages referenced to V_{SS} .
2. This parameter is sampled. $V_{DD} = +3.3V$; $f = 1$ MHz.
3. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
6. An initial pause of $100\mu s$ is required after power-up, followed by eight RAS# REFRESH cycles (RAS#-ONLY or CBR with WE# HIGH), before proper device operation is ensured. The eight RAS# cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
7. AC characteristics assume $t_T = 5ns$ for FPM and $t_T = 2.5ns$ for EDO.
8. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
9. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
10. For FPM: If CAS# = V_{IH} , data output is High-Z.
For EDO: If CAS# and RAS# = V_{IH} , data output is High-Z.
11. If CAS# = V_{IL} , data output may contain data from the last valid READ cycle.
12. Measured with a load equivalent to two TTL gates and $100pF$, $V_{OL} = 0.8V$ and $V_{OH} = 2V$.
13. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for t_{CP} .
14. The t_{RCD} (MAX) limit is no longer specified. t_{RCD} (MAX) was specified as a reference point only. If t_{RCD} was greater than the specified t_{RCD} (MAX) limit, then access time was controlled exclusively by t_{CAC} (t_{RAC} [MIN] no longer applied). With or without the t_{RCD} (MAX) limit, t_{AA} and t_{CAC} must always be met.
15. The t_{RAD} (MAX) limit is no longer specified. t_{RAD} (MAX) was specified as a reference point only. If t_{RAD} was greater than the specified t_{RAD} (MAX) limit, then access time was controlled exclusively by t_{AA} (t_{RAC} and t_{CAC} no longer applied). With or without the t_{RAD} (MAX) limit, t_{AA} , t_{RAC} and t_{CAC} must always be met.
16. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
17. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL} .
18. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles.
19. OE# is tied permanently LOW; LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted.
20. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.
21. The 3ns minimum is a parameter guaranteed by design.
22. Column address changed once each cycle.
23. With the FPM option, t_{OFF} is determined by the first RAS# or CAS# signal to transition HIGH. In comparison, t_{OFF} on an EDO option is determined by the latter of the RAS# and CAS# signals to transition HIGH.
24. Applies to both FPM and EDO operating modes.
25. "S" version only.
26. V_{IH} overshoot: V_{IH} (MAX) = $V_{DD} + 2V$ for a pulse width $\leq 10ns$, and the pulse width cannot be greater than one third of the cycle rate. V_{IL} undershoot: V_{IL} (MIN) = $-2V$ for a pulse width $\leq 10ns$, and the pulse width cannot be greater than one third of the cycle rate.



READ CYCLE ²⁴



FAST PAGE MODE AND EDO PAGE MODE TIMING PARAMETERS

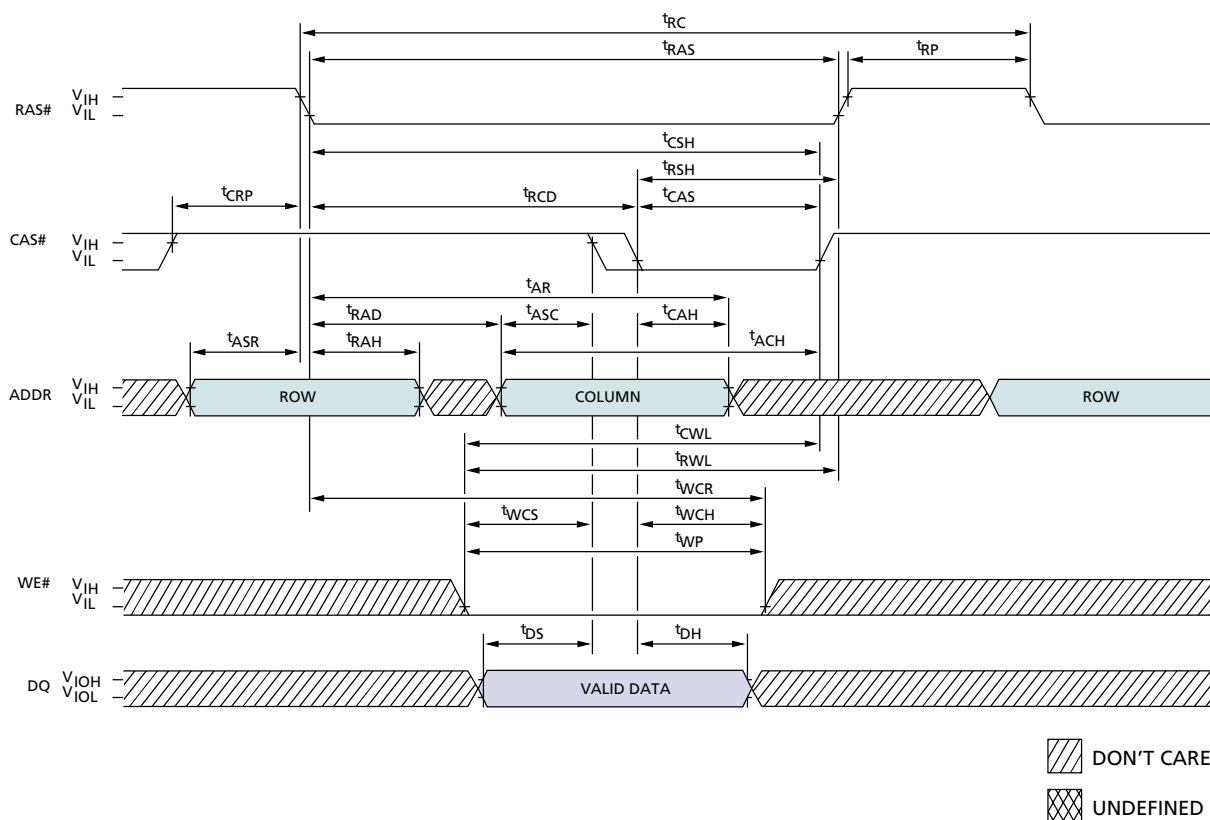
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{AA}		25		30	ns
t _{ACH} (EDO)	12		15		ns
t _{AR} (EDO)	38		45		ns
t _{AR} (FPM)	40		45		ns
t _{ASC}	0		0		ns
t _{ASR}	0		0		ns
t _{CAC}		13		15	ns
t _{CAH}	8		10		ns
t _{CAS} (EDO)	8	10,000	10	10,000	ns
t _{CAS} (FPM)	13	10,000	15	10,000	ns
t _{CLZ} (EDO)	0		0		ns
t _{CLZ} (FPM)	3		3		ns
t _{CRP}	5		5		ns
t _{CSH} (EDO)	38		45		ns
t _{CSH} (FPM)	50		60		ns
t _{OFF} (EDO)	0	12	0	15	ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{OFF} (FPM)	3	13	3	15	ns
t _{RAC}		50		60	ns
t _{RAD} (EDO)	9		12		ns
t _{RAD} (FPM)	13		15		ns
t _{RAH} (EDO)	9		10		ns
t _{RAH} (FPM)	8		10		ns
t _{RAS}	50	10,000	60	10,000	ns
t _{RC} (EDO)	84		104		ns
t _{RC} (FPM)	90		110		ns
t _{RCD} (EDO)	11		14		ns
t _{RCD} (FPM)	18		20		ns
t _{RCH}	0		0		ns
t _{RCS}	0		0		ns
t _{RP}	30		40		ns
t _{RRH}	0		0		ns
t _{RSH}	13		15		ns

NOTE: 1. For EDO, t_{OFF} is referenced from rising edge of RAS# or CAS#, whichever occurs last. For FPM, t_{OFF} is referenced from rising edge of RAS# or CAS#, whichever occurs first.



EARLY WRITE CYCLE ²⁴



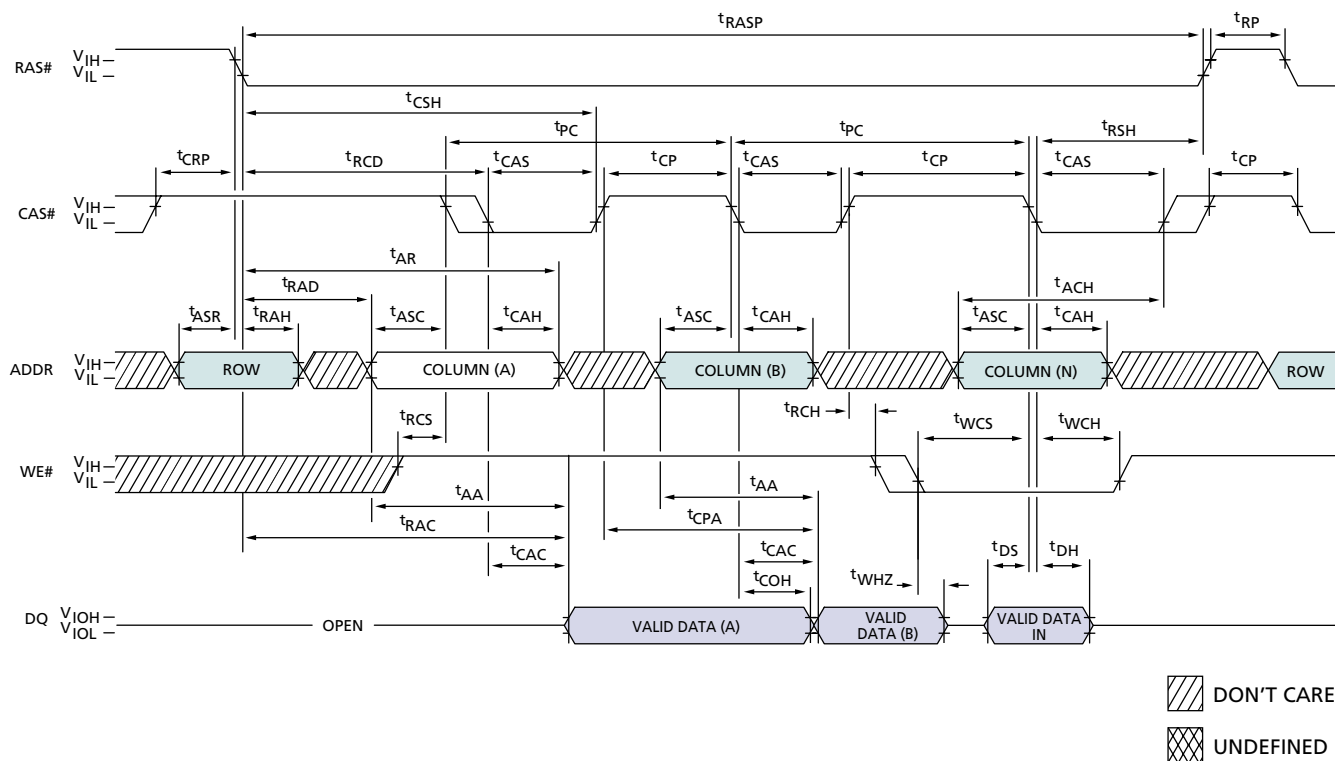
FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{ACH} (EDO)	12		15		ns
t_{AR} (EDO)	38		45		ns
t_{AR} (FPM)	40		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAH}	8		10		ns
t_{CAS} (FPM)	13	10,000	15	10,000	ns
t_{CAS} (EDO)	8	10,000	10	10,000	ns
t_{CRP}	5		5		ns
t_{CSH} (FPM)	50		60		ns
t_{CSH} (EDO)	38		45		ns
t_{CWL} (FPM)	13		15		ns
t_{CWL} (EDO)	8		10		ns
t_{DH}	8		10		ns
t_{DS}	0		0		ns
t_{RAD} (FPM)	13		15		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{RAD} (EDO)	9		12		ns
t_{RAH} (EDO)	9		10		ns
t_{RAH} (FPM)	8		10		ns
t_{RAS}	50	10,000	60	10,000	ns
t_{RC} (FPM)	90		110		ns
t_{RC} (EDO)	84		104		ns
t_{RCD} (FPM)	18		20		ns
t_{RCD} (EDO)	11		14		ns
t_{RP}	30		40		ns
t_{RSH}	13		15		ns
t_{RWL}	13		15		ns
t_{WCH}	8		10		ns
t_{WCR} (EDO)	38		45		ns
t_{WCR} (FPM)	40		45		ns
t_{WCS}	0		0		ns
t_{WP} (FPM)	8		10		ns
t_{WP} (EDO)	5		5		ns



EDO-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



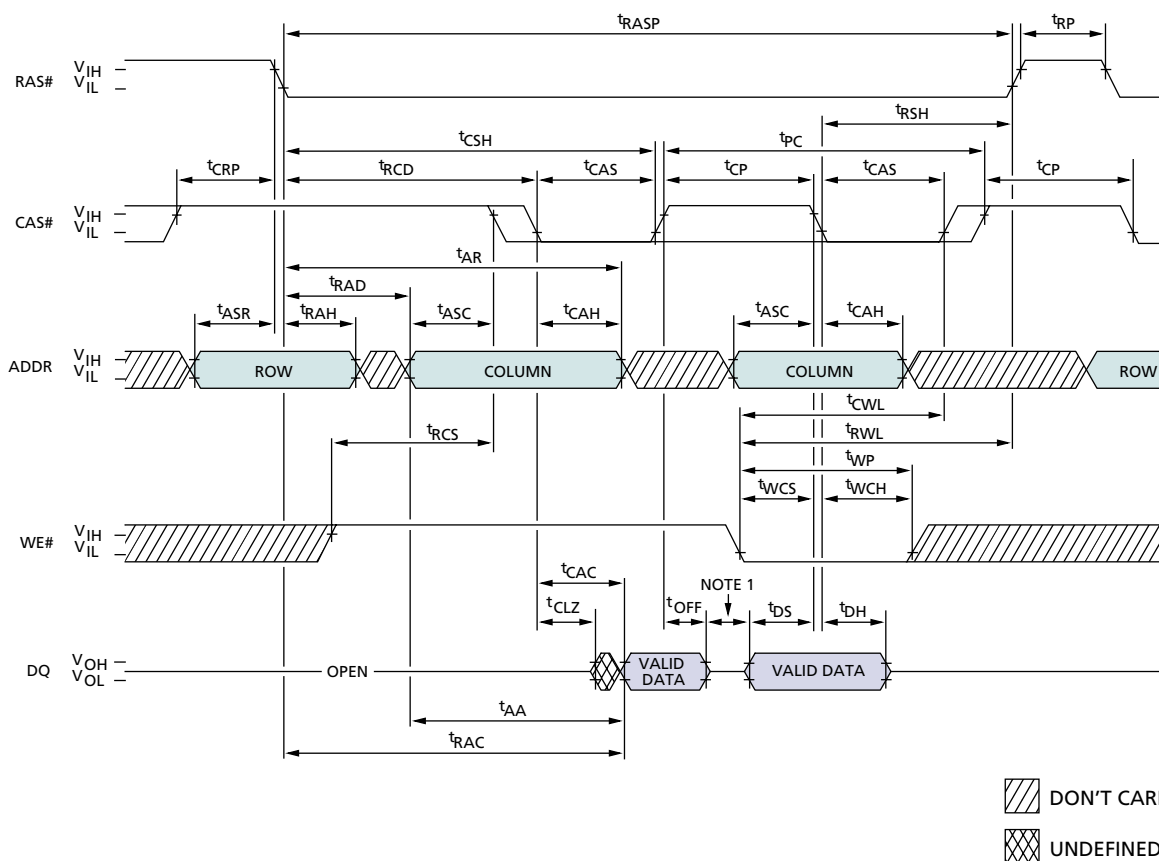
**EDO PAGE MODE
TIMING PARAMETERS**

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tAA		25		30	ns
tACH	12		15		ns
tAR	38		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	8	10,000	10	10,000	ns
tCOH	3		3		ns
tCP	8		10		ns
tCPA		28		35	ns
tCRP	5		5		ns
tCSH	38		45		ns
tDH	8		10		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tDS	0		0		ns
tPC	20		25		ns
tRAC		50		60	ns
tRAD	9		12		ns
tRAH	9		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	11		14		ns
tRCH	0		0		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWHZ	0	12	0	15	ns



**FAST-PAGE-MODE READ EARLY WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)**



**FAST PAGE MODE
TIMING PARAMETERS**

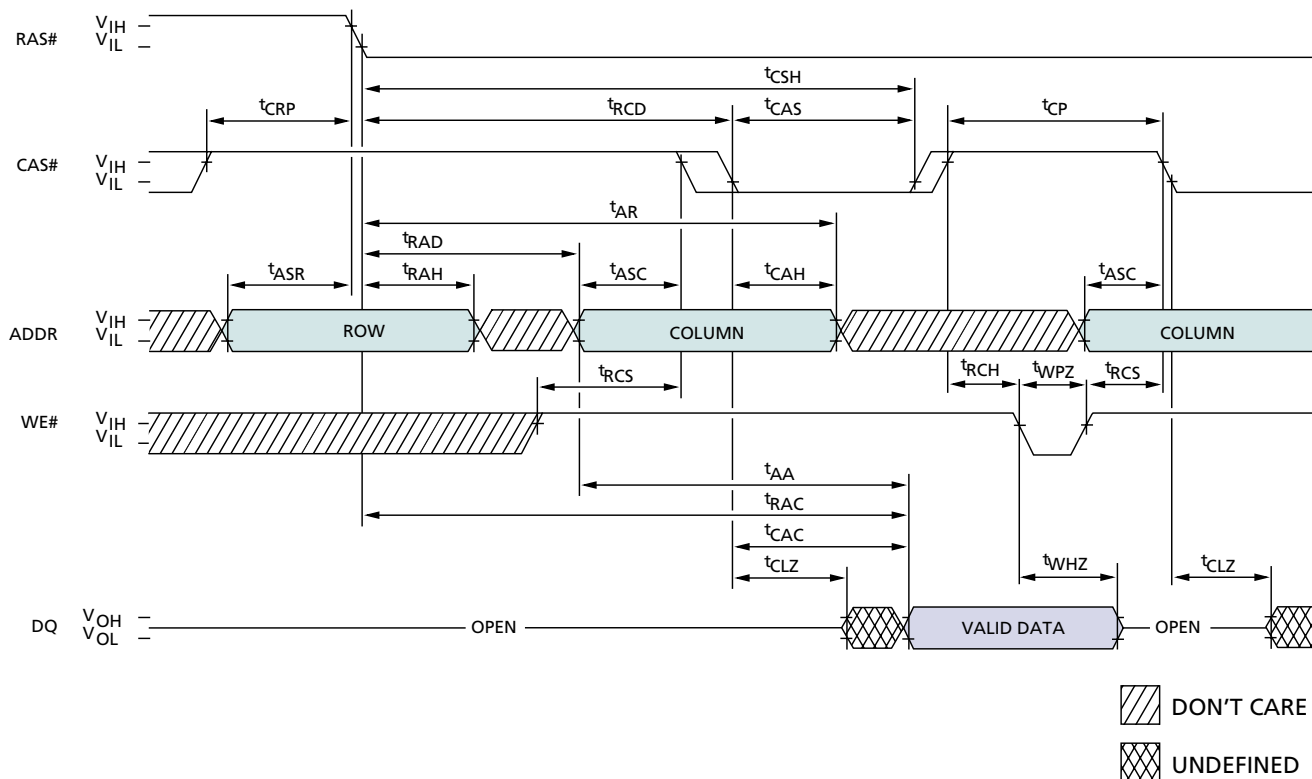
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tAA		25		30	ns
tAR	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCAS	13	10,000	15	10,000	ns
tCLZ	3		3		ns
tCP	8		10		ns
tCRP	5		5		ns
tCSH	50		60		ns
tCWL	13		15		ns
tDH	8		10		ns
tDS	0		0		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tOFF	3	13	3	15	ns
tPC	30		35		ns
tRAC		50		60	ns
tRAD	13		15		ns
tRAH	8		10		ns
tRASP	50	125,000	60	125,000	ns
tRCD	18		20		ns
tRCS	0		0		ns
tRP	30		40		ns
tRSH	13		15		ns
tRWL	13		15		ns
tWCH	8		10		ns
tWCS	0		0		ns
tWP	8		10		ns

NOTE: 1. Do not drive input data prior to output data going High-Z.



EDO READ CYCLE (with WE#-controlled disable)



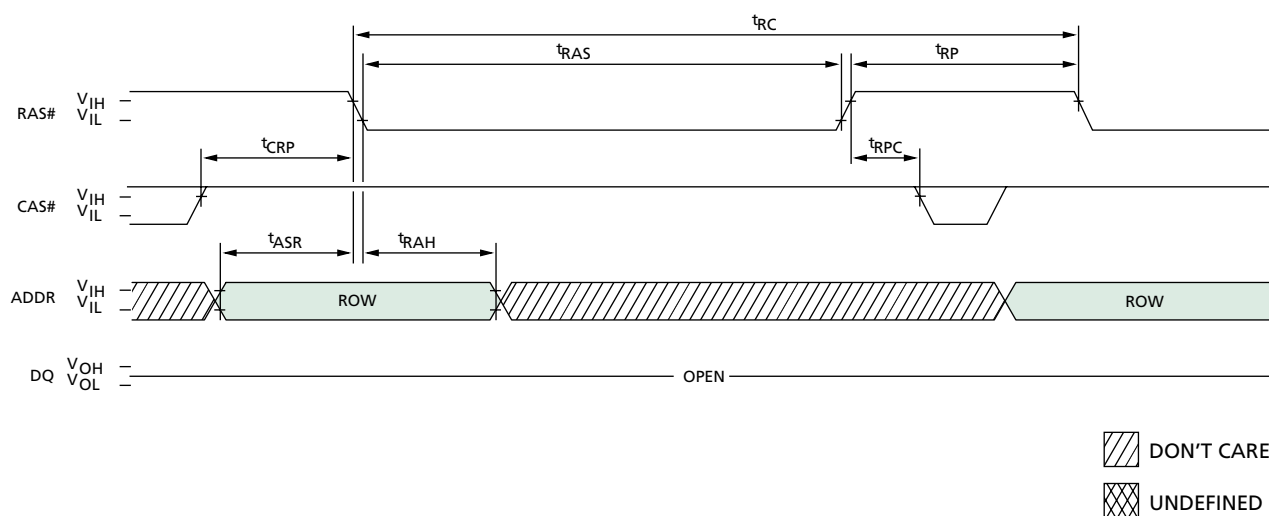
EDO PAGE MODE TIMING PARAMETERS

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{AA}		25		30	ns
t_{AR}	38		45		ns
t_{ASC}	0		0		ns
t_{ASR}	0		0		ns
t_{CAC}		13		15	ns
t_{CAH}	8		10		ns
t_{CAS}	8	10,000	10	10,000	ns
t_{CLZ}	0		0		ns
t_{CP}	8		10		ns
t_{CRP}	5		5		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t_{CSH}	38		45		ns
t_{RAC}		50		60	ns
t_{RAD}	9		12		ns
t_{RAH}	9		10		ns
t_{RCD}	11		14		ns
t_{RCH}	0		0		ns
t_{RCS}	0		0		ns
t_{WHZ}	0	12	0	15	ns
t_{WPZ}	10		10		ns



RAS#-ONLY REFRESH CYCLE²⁴
(OE# and WE# = DON'T CARE)



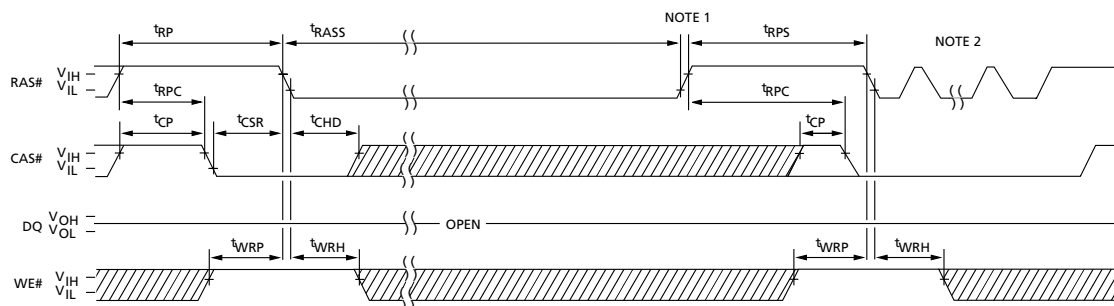
**FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS**

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{ASR}	0		0		ns
t _{CRP}	5		5		ns
t _{CSR}	5		5		ns
t _{RAH} (EDO)	9		10		ns
t _{RAH} (FPM)	8		10		ns
t _{RAS}	50	10,000	60	10,000	ns

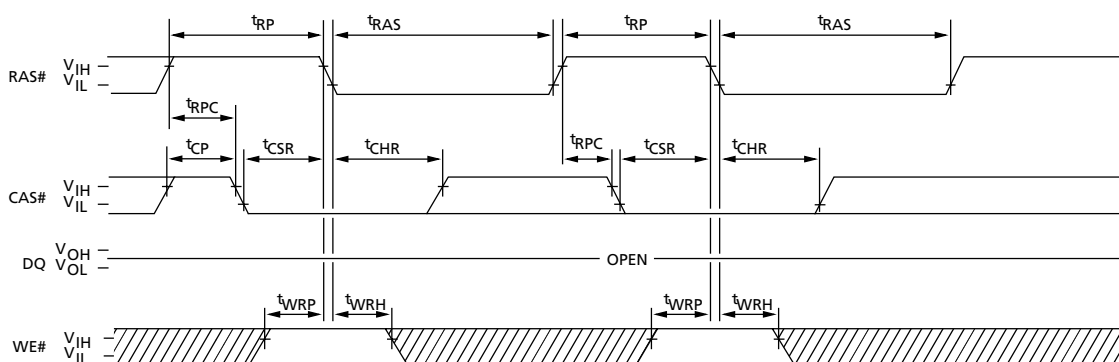
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{RC} (FPM)	90		110		ns
t _{RC} (EDO)	84		104		ns
t _{RP}	30		40		ns
t _{RPC} (FPM)	0		0		ns
t _{RPC} (EDO)	5		5		ns



SELF REFRESH CYCLE 24, 25
(Addresses = DON'T CARE)



CBR REFRESH CYCLE 24
(Addresses = DON'T CARE)



DON'T CARE
 UNDEFINED

**FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS**

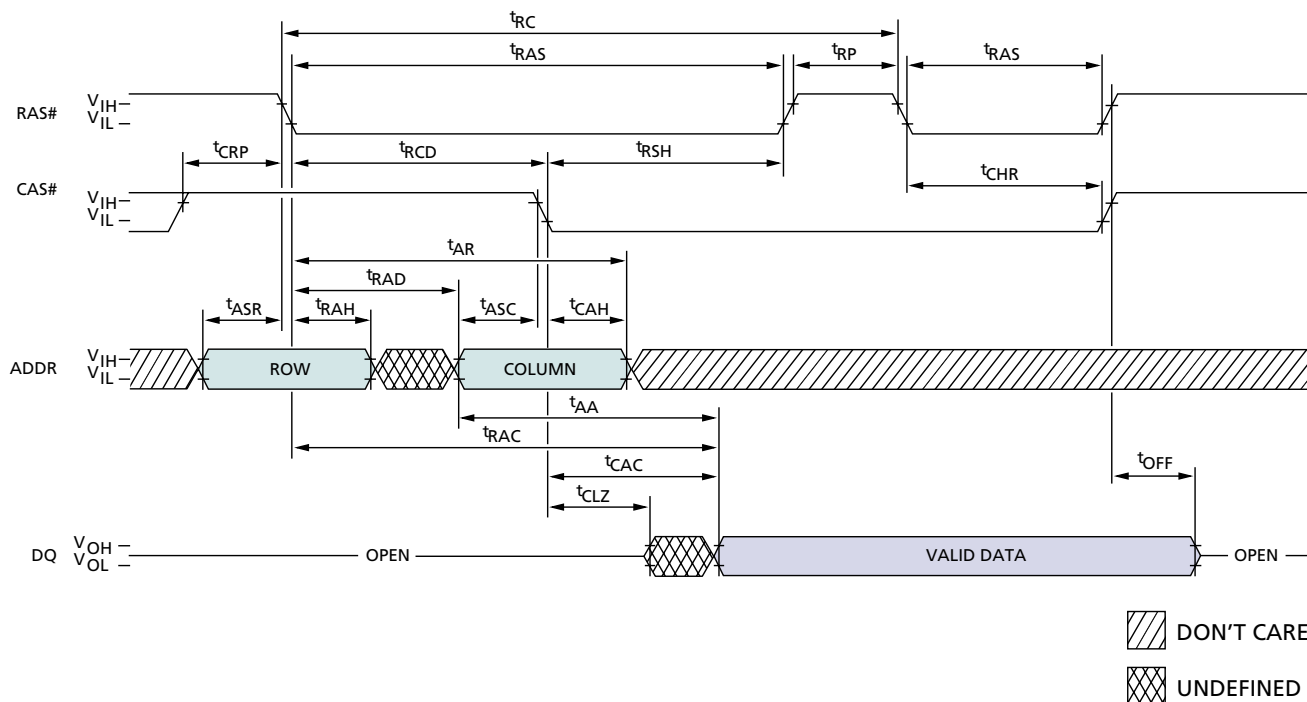
SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{CHD}	15		15		ns
t _{CHR (FPM)}	15		15		ns
t _{CHR (EDO)}	8		10		ns
t _{CP}	8		10		ns
t _{CSR}	5		5		ns
t _{RAS}	50	10,000	60	10,000	ns
t _{RASS}	100		100		μs
t _{RP}	30		40		ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
t _{RPC (FPM)}	0		0		ns
t _{RPC (EDO)}	5		5		ns
t _{RPS}	90		105		ns
t _{WRH (FPM)}	10		10		ns
t _{WRH (EDO)}	8		10		ns
t _{WRP (FPM)}	10		10		ns
t _{WRP (EDO)}	8		10		ns

NOTE: 1. Once t_{RASS} (MIN) is met and RAS# remains LOW, the DRAM will enter self refresh mode.
2. Once t_{RPS} is satisfied, a complete burst of all rows should be executed.



HIDDEN REFRESH CYCLE 20, 24
(WE# = HIGH)



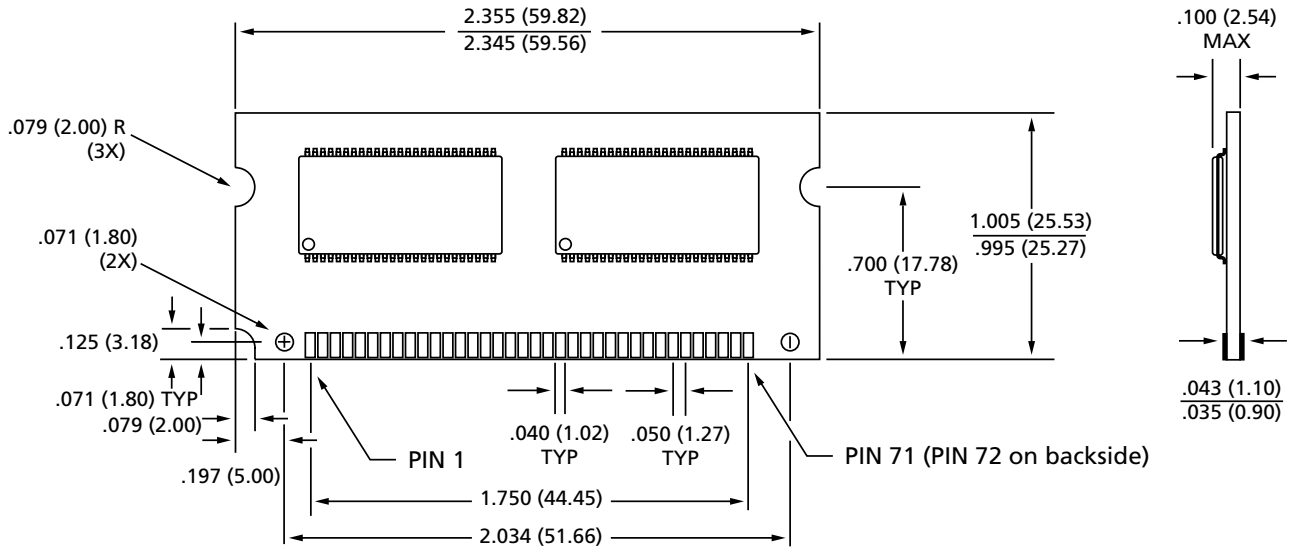
**FAST PAGE MODE AND EDO PAGE MODE
TIMING PARAMETERS**

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tAA		25		30	ns
tAR (EDO)	38		45		ns
tAR (FPM)	40		45		ns
tASC	0		0		ns
tASR	0		0		ns
tCAC		13		15	ns
tCAH	8		10		ns
tCHR (EDO)	8		10		ns
tCHR (FPM)	15		15		ns
tCLZ (EDO)	0		0		ns
tCLZ (FPM)	3		3		ns
tCRP	5		5		ns
tOFF (EDO)	0	12	0	15	ns

SYMBOL	-5		-6		UNITS
	MIN	MAX	MIN	MAX	
tOFF (FPM)	3	13	3	15	ns
tRAC		50		60	ns
tRAD (EDO)	9		12		ns
tRAD (FPM)	13		15		ns
tRAH (EDO)	9		10		ns
tRAH (FPM)	8		10		ns
tRAS	50	10,000	60	10,000	ns
tRC (EDO)	84		104		ns
tRC (FPM)	90		110		ns
tRCD (EDO)	11		14		ns
tRCD (FPM)	18		20		ns
tRP	30		40		ns
tRSH	13		15		ns

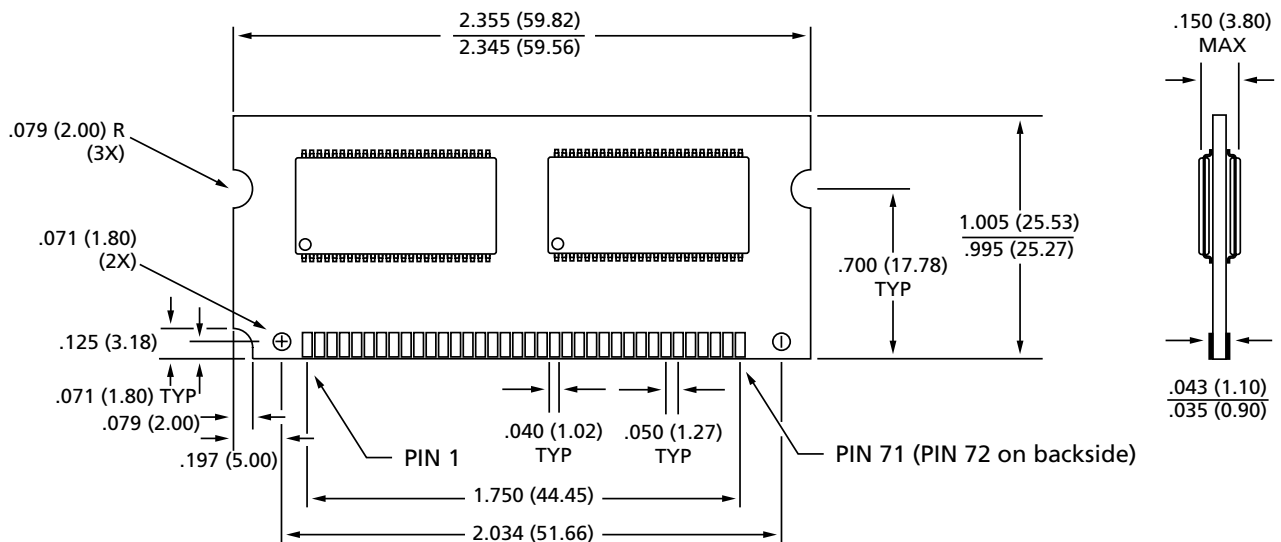
72-PIN SODIMM
(4 Meg x 32)

FRONT VIEW



72-PIN SODIMM
(8 Meg x 32)

FRONT VIEW



NOTE: All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

ADVANCE



**4, 8 MEG x 32
DRAM SODIMMs**



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