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Lattice Semiconductor Corporation

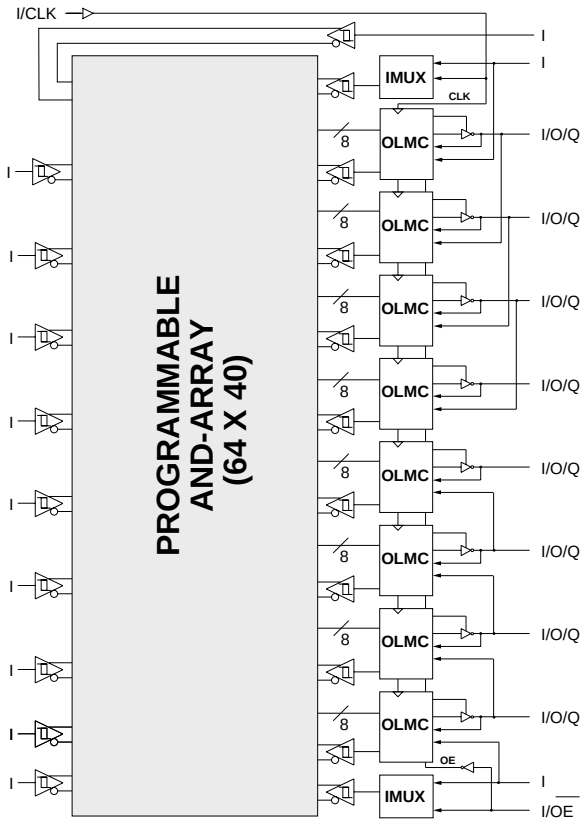
GAL20VP8

High-Speed E²CMOS PLD Generic Array Logic™

Features

- **HIGH DRIVE E²CMOS® GAL® DEVICE**
  - **— TTL Compatible 64 mA Output Drive**
  - **— 15 ns Maximum Propagation Delay**
  - **— Fmax = 80 MHz**
  - **— 10 ns Maximum from Clock Input to Data Output**
  - **— UltraMOS® Advanced CMOS Technology**
- **ENHANCED INPUT AND OUTPUT FEATURES**
  - **— Schmitt Trigger Inputs**
  - **— Programmable Open-Drain or Totem-Pole Outputs**
  - **— Active Pull-Ups on All Inputs and I/O pins**
- **E² CELL TECHNOLOGY**
  - **— Reconfigurable Logic**
  - **— Reprogrammable Cells**
  - **— 100% Tested/100% Yields**
  - **— High Speed Electrical Erasure (<100ms)**
  - **— 20 Year Data Retention**
- **EIGHT OUTPUT LOGIC MACROCELLS**
  - **— Maximum Flexibility for Complex Logic Designs**
  - **— Programmable Output Polarity**
  - **— Architecturally Compatible with Standard GAL20V8**
- **PRELOAD AND POWER-ON RESET OF ALL REGISTERS**
  - **— 100% Functional Testability**
- **APPLICATIONS INCLUDE:**
  - **— Ideal for Bus Control & Bus Arbitration Logic**
  - **— Bus Address Decode Logic**
  - **— Memory Address, Data and Control Circuits**
  - **— DMA Control**
- **ELECTRONIC SIGNATURE FOR IDENTIFICATION**

Functional Block Diagram



Description

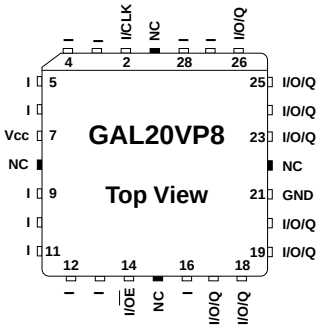
The GAL20VP8, with 64 mA drive capability and 15 ns maximum propagation delay time is ideal for Bus and Memory control applications. The GAL20VP8 is manufactured using Lattice Semiconductor's advanced E²CMOS process which combines CMOS with Electrically Erasable (E²) floating gate technology. High speed erase times (<100ms) allow the devices to be reprogrammed quickly and efficiently.

System bus and memory interfaces require control logic before driving the bus or memory interface signals. The GAL20VP8 combines the familiar GAL20V8 architecture with bus drivers as its outputs. The generic architecture provides maximum design flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user. The 64mA output drive eliminates the need for additional devices to provide bus-driving capability.

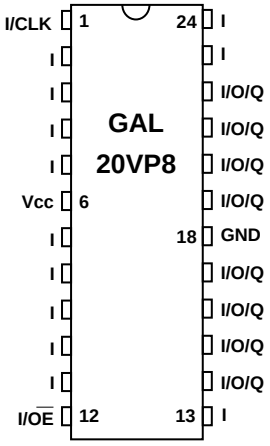
Unique test circuitry and reprogrammable cells allow complete AC, DC, and functional testing during manufacture. As a result, Lattice Semiconductor delivers 100% field programmability and functionality of all GAL products. In addition, 100 erase/write cycles and data retention in excess of 20 years are specified.

Pin Configuration

PLCC



DIP



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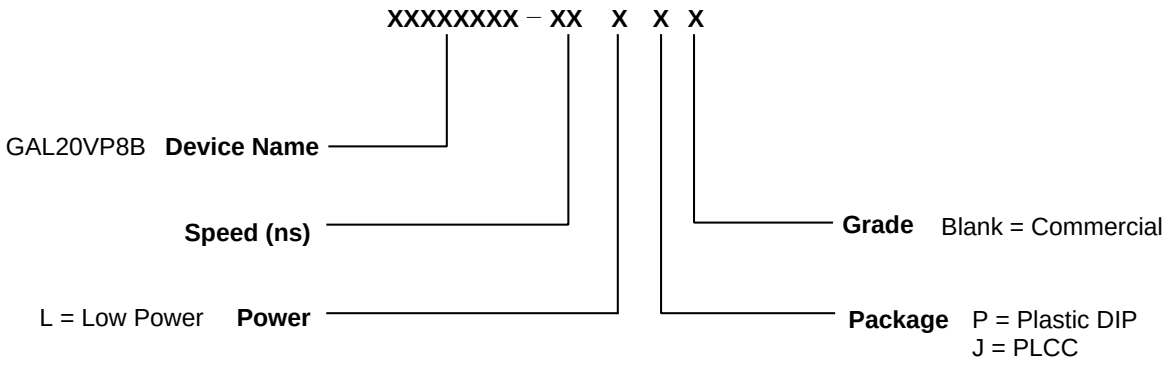
December 1997

GAL20VP8 Ordering Information

Commercial Grade Specifications

Tpd (ns)	Tsu (ns)	Tco (ns)	Icc (mA)	Ordering #	Package
15	8	10	115	GAL20VP8B-15LP	24-Pin Plastic DIP
			115	GAL20VP8B-15LJ	28-Lead PLCC
25	10	15	115	GAL20VP8B-25LP	24-Pin Plastic DIP
			115	GAL20VP8B-25LJ	28-Lead PLCC

Part Number Description



Output Logic Macrocell (OLMC)

The following discussion pertains to configuring the output logic macrocell. It should be noted that actual implementation is accomplished by development software/hardware and is completely transparent to the user.

There are three global OLMC configuration modes possible: **simple**, **complex**, and **registered**. Details of each of these modes is illustrated in the following pages. Two global bits, SYN and AC0, control the mode configuration for all macrocells. The XOR bit of each macrocell controls the polarity of the output in any of the three modes, while the AC1 and AC2 bit of each of the macrocells controls the input/output and totem-pole/open-drain configuration. These two global and 24 individual architecture bits define all possible configurations in a GAL20VP8. The information given on these architecture bits is only to give a better understanding of the device. Compiler software will transparently set these architecture bits from the pin definitions, so the user should not need to directly manipulate these architecture bits.

Compiler Support for OLMC

Software compilers support the three different global OLMC modes as different device types. Most compilers also have the ability to automatically select the device type, generally based on the register usage and output enable (OE) usage. Register usage on the device forces the software to choose the registered mode. All combinatorial outputs with OE controlled by the product term will force the software to choose the complex mode. The software will choose the simple mode only when all outputs are dedicated combinatorial without OE control. For further details, refer to the compiler software manuals.

When using compiler software to configure the device, the user must pay special attention to the following restrictions in each mode. In **registered mode** pin 1(2) and pin 12(14) are permanently configured as clock and output enable, respectively. These pins cannot be configured as dedicated inputs in the registered mode.

In **complex mode** pin 1(2) and pin 12(14) become dedicated inputs and use the feedback paths of pin 22(26) and pin 14(17) respectively. Because of this feedback path usage, pin 22(26) and pin 14(17) do not have the feedback option in this mode.

In **simple mode** all feedback paths of the output pins are routed via the adjacent pins. In doing so, the two inner most pins (pins 17(20) and 19(23)) will not have the feedback option as these pins are always configured as dedicated combinatorial output.

In addition to the architecture configurations, the logic compiler software also supports configuration of either totem-pole or open-drain outputs. The actual architecture bit configuration, again, is transparent to the user with the default configuration being the standard totem-pole output.

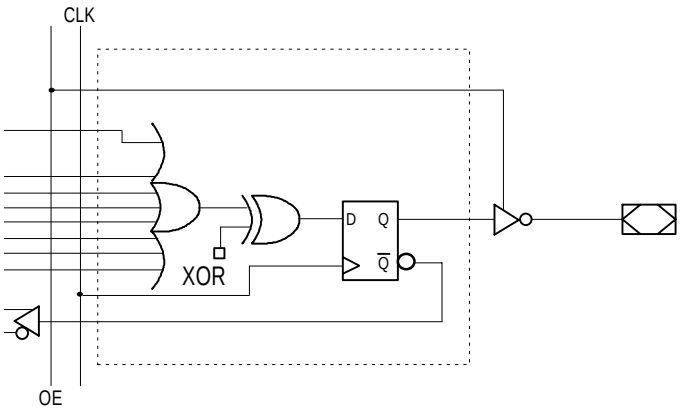
Registered Mode

In the Registered mode, macrocells are configured as dedicated registered outputs or as I/O functions.

All registered macrocells share common clock and output enable control pins. Any macrocell can be configured as registered or I/O. Up to eight registers or up to eight I/Os are possible in this mode. Dedicated input or output functions can be implemented as subsets of the I/O function.

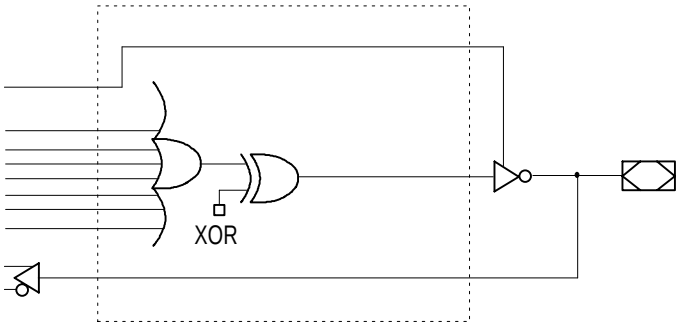
Registered outputs have eight product terms per output. I/Os have seven product terms per output.

The JEDEC fuse numbers, including the User Electronic Signature (UES) fuses and the Product Term Disable (PTD) fuses, are shown on the logic diagram on the following page.



Registered Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this output configuration.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pin 1(2) controls common CLK for the registered outputs.
- Pin 12(14) controls common $\overline{OE}$ for the registered outputs.
- Pin 1(2) & Pin 12(14) are permanently configured as CLK & $\overline{OE}$ for registered output configuration.



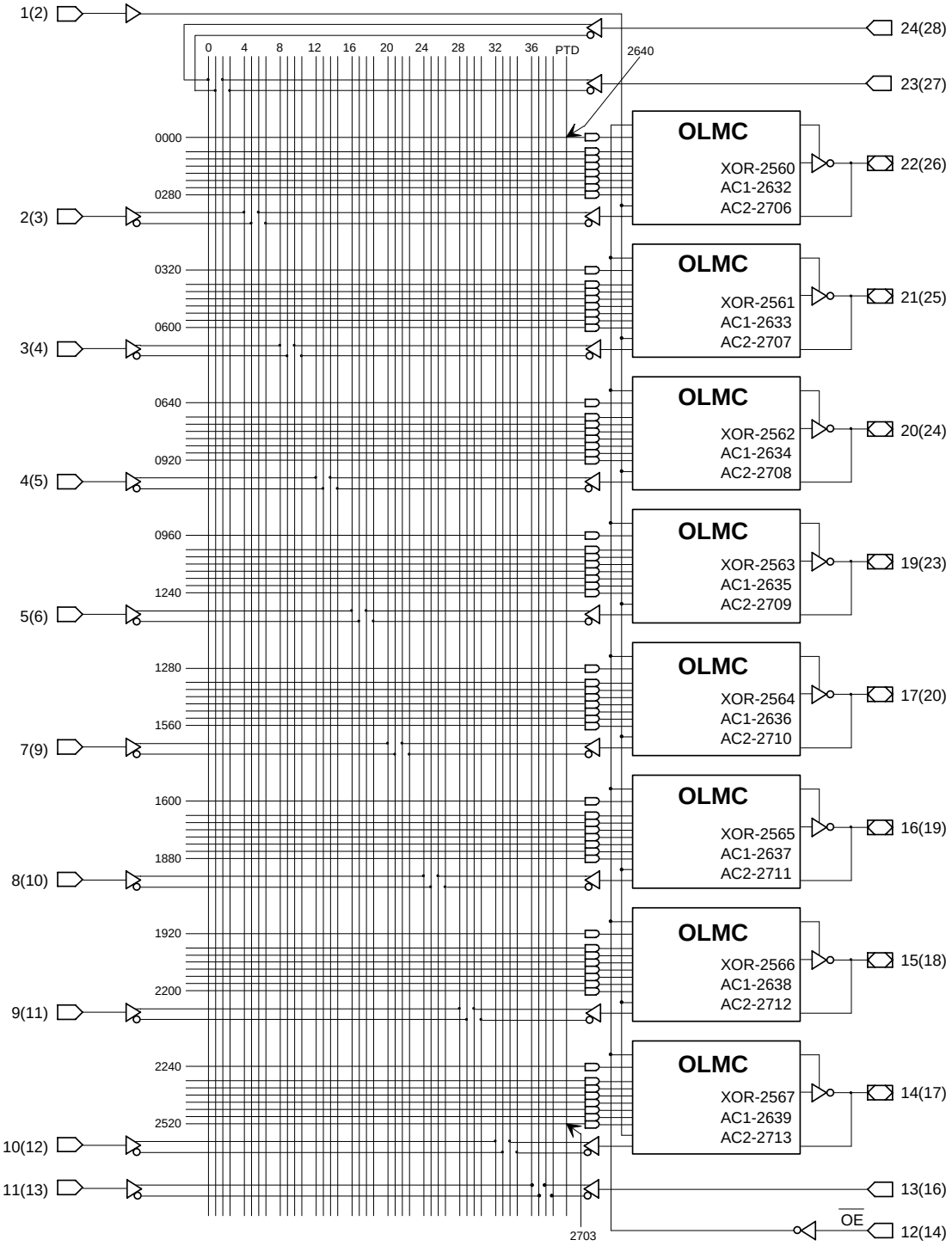
Combinatorial Configuration for Registered Mode

- SYN=0.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this output configuration.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pin 1(2) & Pin 12(14) are permanently configured as CLK & $\overline{OE}$. for registered output configuration.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Registered Mode Logic Diagram

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...		.... 2630, 2631	
Byte7	Byte6	.... Byte1	Byte0

MSB LSB

SYN-2704
AC0-2705

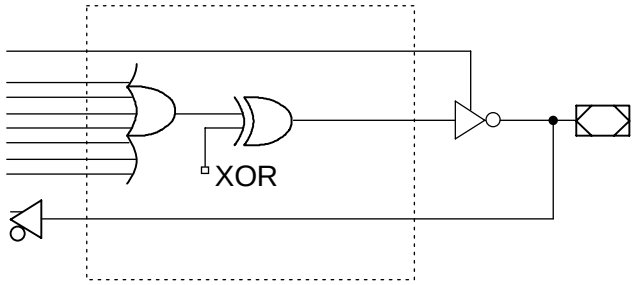
Complex Mode

In the Complex mode, macrocells are configured as output only or I/O functions.

Up to six I/Os are possible in this mode. Dedicated inputs or outputs can be implemented as subsets of the I/O function. The two outer most macrocells (pins 14(17) & 22(26)) do not have input capability. Designs requiring eight I/Os can be implemented in the Registered mode.

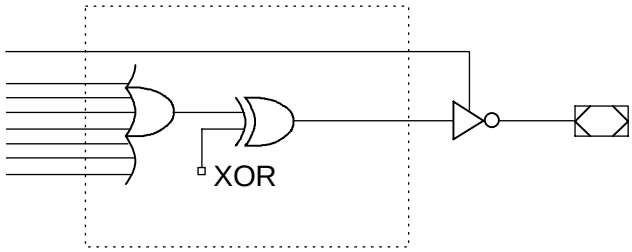
All macrocells have seven product terms per output. One product term is used for programmable output enable control. Pins 1(2) and 12(14) are always available as data inputs into the AND array.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram on the following page.



Combinatorial I/O Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pin 15(18) through Pin 21(25) are configured to this function.



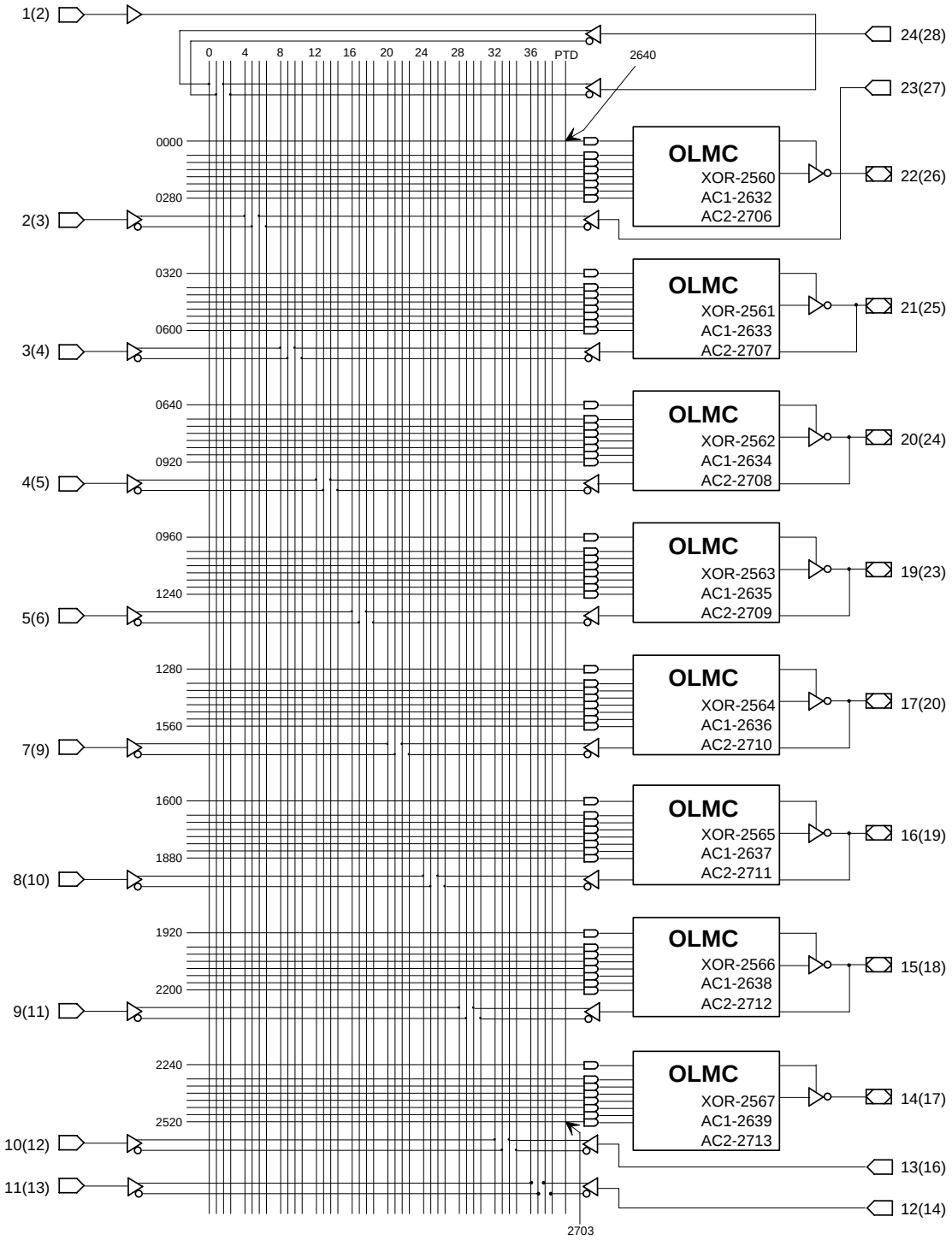
Combinatorial Output Configuration for Complex Mode

- SYN=1.
- AC0=1.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1 has no effect on this mode.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pin 14(17) and Pin 22(26) are configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Complex Mode Logic Diagram

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...		.... 2630, 2631	
Byte7	Byte6	.... Byte1	Byte0

MSB LSB

SYN-2704
AC0-2705

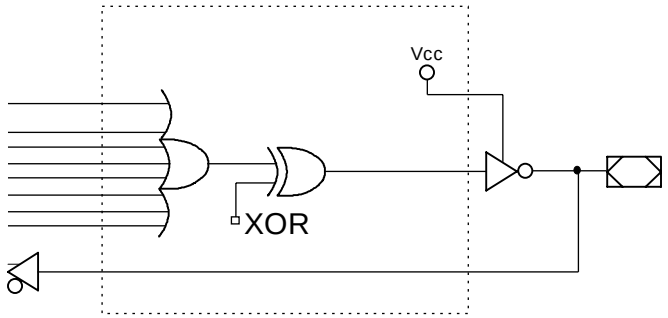
Simple Mode

In the Simple mode, macrocells are configured as dedicated inputs or as dedicated, always active, combinatorial outputs.

All outputs in the simple mode have a maximum of eight product terms that can control the logic. In addition, each output has programmable polarity.

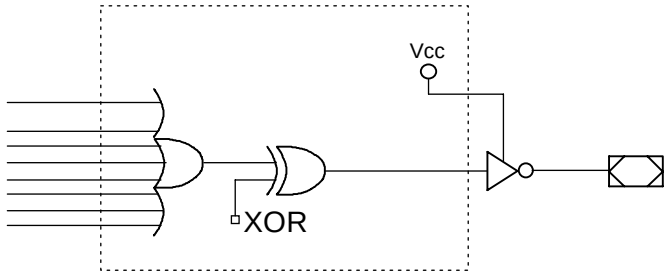
Pins 1(2) and 12(14) are always available as data inputs into the AND array. The center two macrocells (pins 17(20) & 19(23)) cannot be used in the input configuration.

The JEDEC fuse numbers including the UES fuses and PTD fuses are shown on the logic diagram.



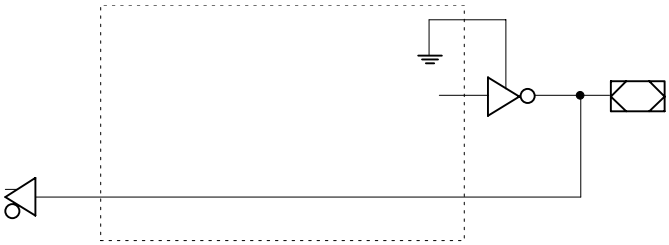
Combinatorial Output with Feedback Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- All OLMC **except** pins 17(20) & 19(23) can be configured to this function.



Combinatorial Output Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=0 defines this configuration.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- Pins 17(20) & 19(23) are permanently configured to this function.



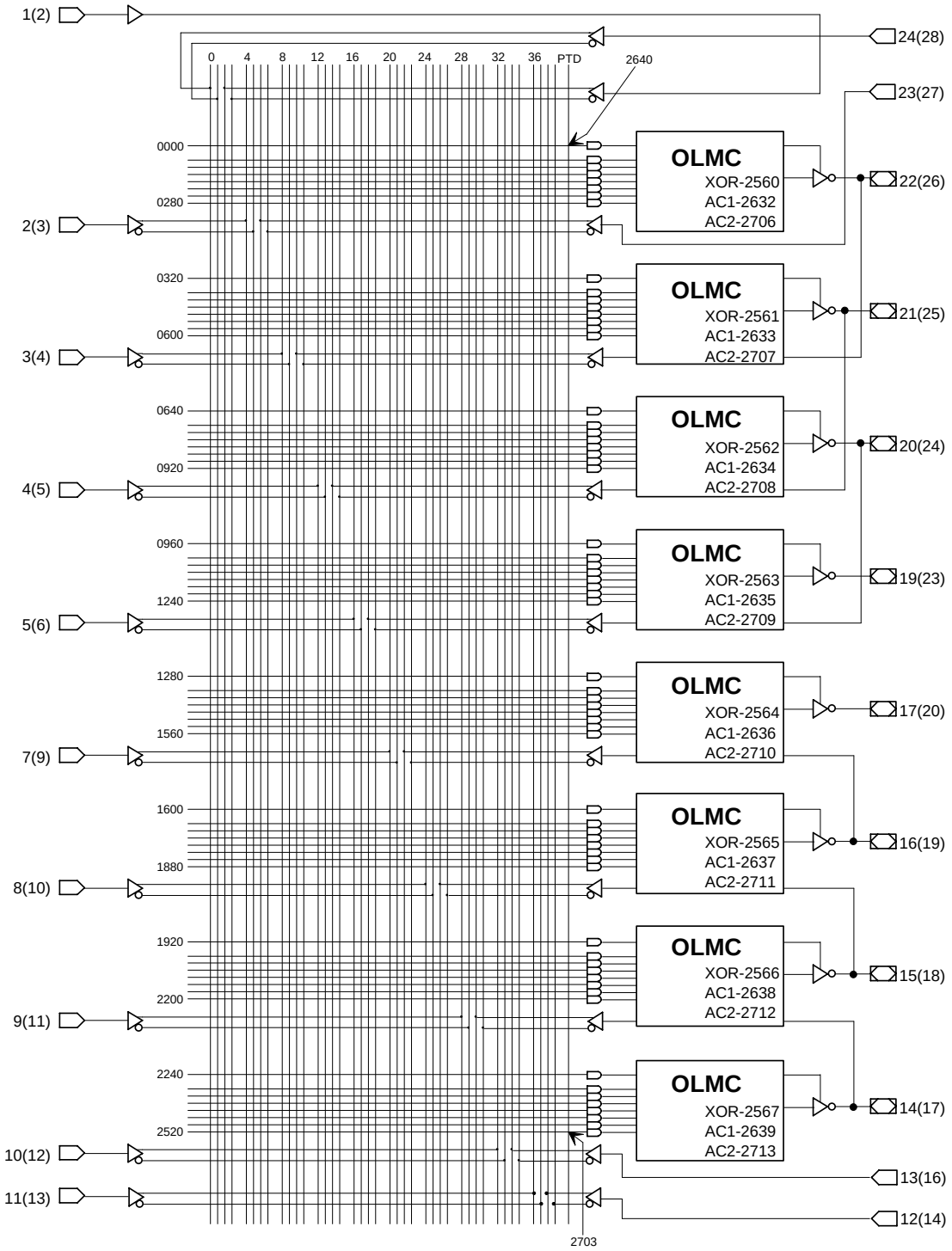
Dedicated Input Configuration for Simple Mode

- SYN=1.
- AC0=0.
- XOR=0 defines Active Low Output.
- XOR=1 defines Active High Output.
- AC1=1 defines this configuration.
- AC2=1 defines totem pole output.
- AC2=0 defines open-drain output.
- All OLMC **except** pins 17(20) & 19(23) can be configured to this function.

Note: The development software configures all of the architecture control bits and checks for proper pin usage automatically.

Simple Mode Logic Diagram

DIP (PLCC) Package Pinouts



64-USER ELECTRONIC SIGNATURE FUSES

2568, 2569, ...		.... 2630, 2631	
Byte7	Byte6	.... Byte1	Byte0

MSB LSB

SYN-2704
AC0-2705

Absolute Maximum Ratings(1)

Supply voltage V_{CC} ..... –.5 to +7V
Input voltage applied ..... –2.5 to V_{CC} +1.0V
Off-state output voltage applied ..... –2.5 to V_{CC} +1.0V
Storage Temperature ..... –65 to 150°C
Ambient Temperature with
Power Applied ..... –55 to 125°C

1. Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied (while programming, follow the programming specifications).

Recommended Operating Conditions

Commercial Devices:
Ambient Temperature (T_A) ..... 0 to 75°C
Supply voltage (V_{CC})
with Respect to Ground ..... +4.75 to +5.25V

DC Electrical Characteristics

Over Recommended Operating Conditions (Unless Otherwise Specified)

SYMBOL	PARAMETER	CONDITION	MIN.	TYP.[4]	MAX.	UNITS
V_{IL}	Input Low Voltage		Vss – 0.5	—	0.8	V
V_{IH}	Input High Voltage		2.0	—	Vcc+1	V
V_{I}[1]	Input Clamp Voltage	V_{CC} = Min. I_{IN} = –32mA	—		–1.2	V
I_{IL}[2]	Input or I/O Low Leakage Current	0V ≤ V_{IN} ≤ V_{IL} (MAX.)	—	—	–100	µA
I_{IH}	Input or I/O High Leakage Current	3.5V ≤ V_{IN} ≤ V_{CC}	—	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = MAX. Vin = V_{IL} or V_{IH}	—	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = MAX. Vin = V_{IL} or V_{IH}	2.4	—	—	V
I_{OL}	Low Level Output Current		—	—	64	mA
I_{OH}	High Level Output Current		—	—	–32	mA
I_{OS}[3]	Output Short Circuit Current	V_{CC} = 5V V_{OUT} = 0.5V T_A = 25°C	–60	—	–400	mA

COMMERCIAL

I_{CC}	Operating Power Supply Current	V_{IL} = 0.5V V_{IH} = 3.0V f_{toggle} = 15MHz Outputs Open	L -15/-25	—	90	115	mA

1) Characterized but not 100% tested.
2) The leakage current is due to the internal pull-up resistor on all pins. See Input Buffer section for more information.
3) One output at a time for a maximum duration of one second. Vout = 0.5V was selected to avoid test problems by tester ground degradation. Characterized but not 100% tested.
4) Typical values are at Vcc = 5V and T_A = 25 °C

AC Switching Characteristics

Over Recommended Operating Conditions

PARAMETER	TEST COND[1].	DESCRIPTION	COM -15 MIN.	COM -15 MAX.	COM -25 MIN.	COM -25 MAX.	UNITS
tpd	A	Input or I/O to Combinational Output	3	15	3	25	ns
tco	A	Clock to Output Delay	2	10	2	15	ns
tcf[2]	—	Clock to Feedback Delay	—	4.5	—	10	ns
tsu	—	Setup Time, Input or Feedback before Clock ↑	8	—	10	—	ns
th	—	Hold Time, Input or Feedback after Clock ↑	0	—	0	—	ns
fmax[3]	A	Maximum Clock Frequency with External Feedback, 1/(tsu + tco)	55.5	—	40	—	MHz
	A	Maximum Clock Frequency with Internal Feedback, 1/(tsu + tcf)	80	—	50	—	MHz
	A	Maximum Clock Frequency with No Feedback	80	—	50	—	MHz
twh	—	Clock Pulse Duration, High	6	—	10	—	ns
twl	—	Clock Pulse Duration, Low	6	—	10	—	ns
ten	B	Input or I/O to Output Enabled	—	15	—	20	ns
	B	$\overline{OE}$ to Output Enabled	—	12	—	15	ns
tdis	C	Input or I/O to Output Disabled	—	15	—	20	ns
	C	$\overline{OE}$ to Output Disabled	—	12	—	15	ns

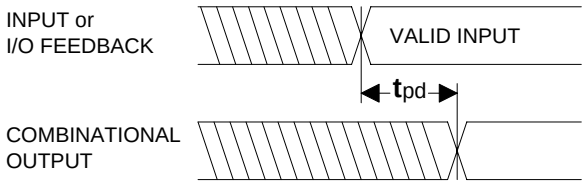
1) Refer to **Switching Test Conditions** section.
2) Calculated from **f**max with internal feedback. Refer to **fmax Specification** section.
3) Refer to **fmax Specification** section.

Capacitance (T_A = 25°C, f = 1.0 MHz)

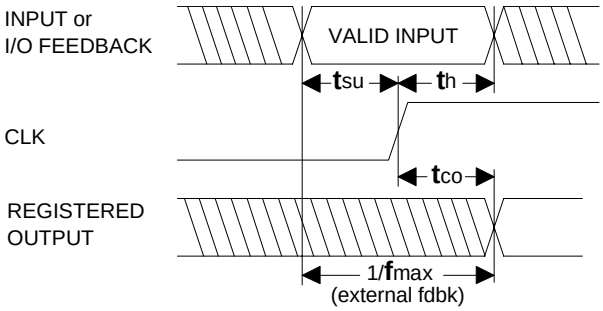
SYMBOL	PARAMETER	MAXIMUM*	UNITS	TEST CONDITIONS
C_I	Input Capacitance	10	pF	V_{CC} = 5.0V, V_I = 2.0V
$C_{I/O}$	I/O Capacitance	15	pF	V_{CC} = 5.0V, $V_{I/O}$ = 2.0V

*Characterized but not 100% tested.

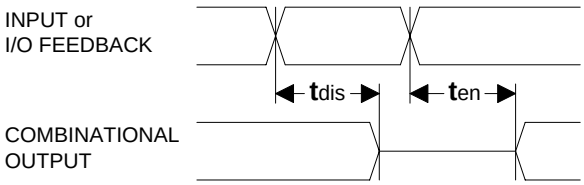
Switching Waveforms



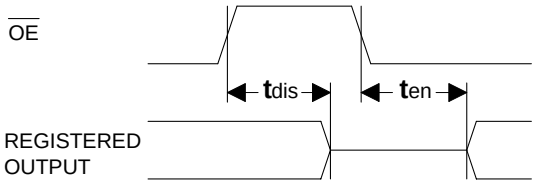
Combinatorial Output



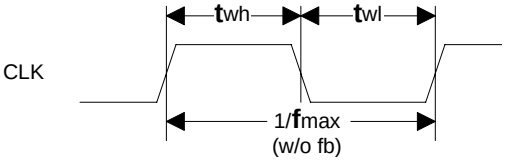
Registered Output



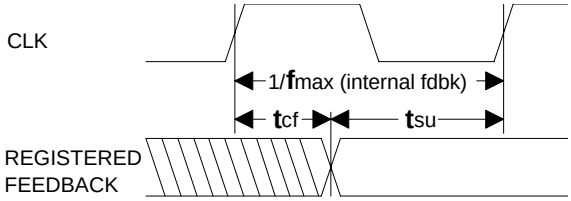
Input or I/O to Output Enable/Disable



$\overline{OE}$ to Output Enable/Disable

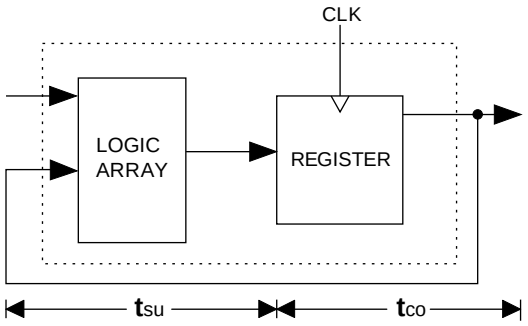


Clock Width



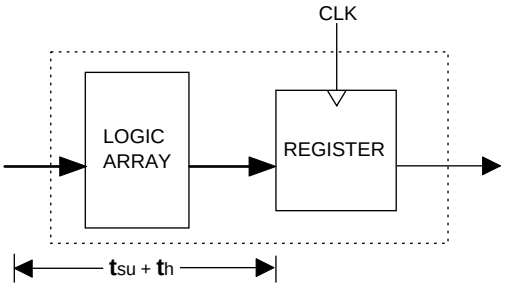
fmax with Feedback

fmax Descriptions



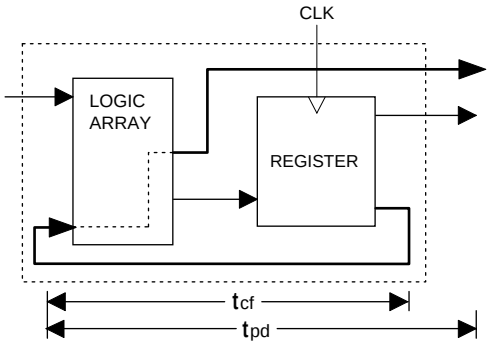
fmax with External Feedback 1/(tsu+tco)

Note: fmax with external feedback is calculated from measured tsu and tco.



fmax with No Feedback

Note: fmax with no feedback may be less than 1/(twh + twl). This is to allow for a clock duty cycle of other than 50%.



fmax with Internal Feedback 1/(tsu+tcf)

Note: tcf is a calculated value, derived by subtracting tsu from the period of fmax w/internal feedback (tcf = 1/fmax - tsu). The value of tcf is used primarily when calculating the delay from clocking a register to a combinatorial output (through registered feedback), as shown above. For example, the timing from clock to a combinatorial output is equal to tcf + tpd.

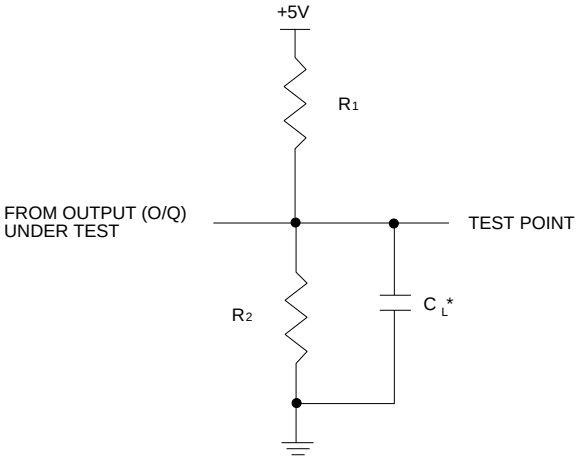
Switching Test Conditions

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns 10% – 90%
Input Timing Reference Levels	1.5V
Output Timing Reference Levels	1.5V
Output Load	See Figure

3-state levels are measured 0.5V from steady-state active level.

Output Load Conditions (see figure)

Test Condition		R_1	R_2	C_L
A		500Ω	500Ω	50pF
B	Active High	∞	500Ω	50pF
	Active Low	500Ω	500Ω	50pF
C	Active High	∞	500Ω	5pF
	Active Low	500Ω	500Ω	5pF



*C_L INCLUDES TEST FIXTURE AND PROBE CAPACITANCE

Electronic Signature

An electronic signature word is provided in every GAL20VP8 device. It contains 64 bits of reprogrammable memory that can contain user defined data. Some uses include user ID codes, revision numbers, or inventory control. The signature data is always available to the user independent of the state of the security cell.

NOTE: The electronic signature is included in checksum calculations. Changing the electronic signature will alter the checksum.

Signature Cell

The security cell is provided on all GAL20VP8 devices to prevent unauthorized copying of the array patterns. Once programmed, the circuitry enabling array is disabled, preventing further programming or verification of the array. The cell can only be erased by reprogramming the device, so the original configuration can never be examined once this cell is programmed. Signature data is always available to the user.

Latch-Up Protection

GAL20VP8 devices are designed with an on-board charge pump to negatively bias the substrate. The negative bias is of sufficient magnitude to prevent input undershoots from causing the circuitry to latch. Additionally, outputs are designed with n-channel pull-ups instead of the traditional p-channel pull-ups to eliminate any possibility of SCR induced latching.

Bulk Erase Mode

During a programming cycle, a clear function performs a bulk erase of the array and the architecture word. In addition, the electronic signature word and the security cell are erased. This mode resets a previously configured device back to its original state, which is all JEDEC ones.

Schmitt Trigger Inputs

One of the enhancements of the GAL20VP8 for bus interface logic implementation is input gysteresis. The threshold of the positive going edge is 1.5V, while the threshold of the negative going edge is 1.3V. This provides a typical hysteresis of 200mV between positive and negative transitions of the inputs.

Bulk Erase Mode

All eight outputs of the GAL20VP8 are capable of driving 64 mA loads when driving low and 32 mA loads when driving high. Near symmetrical high and low output drive capability provides small skews between high-to-low and low-to-high output transitions.

Output Register Preload

When testing state machine designs, all possible states and state transitions must be verified in the design, not just those required in the normal machine operations. This is because, in system operation, certain events occur that may throw the logic into an illegal state (power-up, line voltage glitches, brown-outs, etc.). To test a design for proper treatment of these conditions, a way must be provided to break the feedback paths, and force any desired (i.e., illegal) state into the registers. Then the machine can be sequenced and the outputs tested for correct next state conditions.

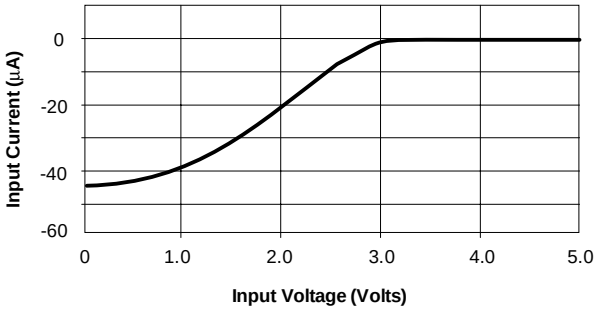
The GAL20VP8 device includes circuitry that allows each registered output to be synchronously set either high or low. Thus, any present state condition can be forced for test sequencing. If necessary, approved GAL programmers capable of executing test vectors can perform output register preload automatically.

Input Buffers

The GAL20VP8 devices are designed with TTL level compatible input buffers. These buffers have a characteristically high impedance, and present a much lighter load to the driving logic than bipolar TTL devices.

GAL20VP8 input buffers have active pull-ups within their input structure. As a result, unused inputs and I/O's will float to a TTL "high" (logical "1"). Lattice Semiconductor recommends that all unused inputs and tri-stated I/O pins for both devices be connected to another active input, V_{CC}, or GND. Doing this will tend to improve noise immunity and reduce I_{CC} for the device.

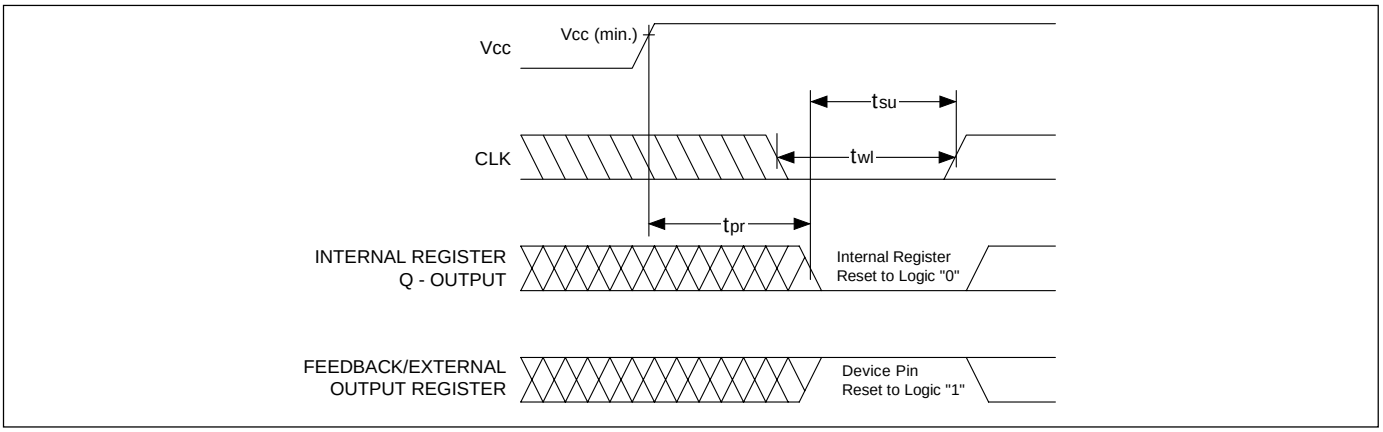
Typical Input Pull-up Characteristic



Programmable Open-Drain Outputs

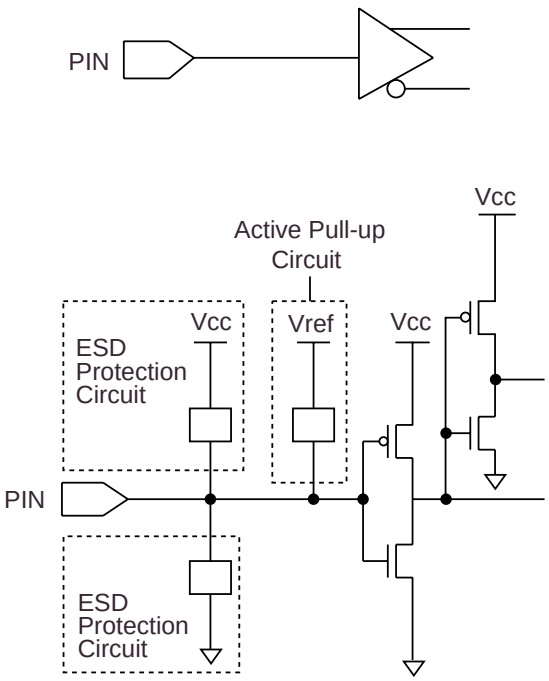
In addition to the standard GAL20V8 type configuration, the outputs of the GAL20VP8 are individually programmable either as a standard totempole output or an open-drain output. The totempole output drives the specified V_{OH} and V_{OL} levels whereas the open-drain output drives only the specified V_{OL}. The V_{OH} level on the open-drain output depends on the external loading and pull-up. This output configuration is controlled by the AC2 fuse. When AC2 cell is erased (JEDEC "1") the output is configured as a totempole output and when AC2 cell is programmed (JEDEC "0") the output is configured as an open-drain. The default configuration when the device is in bulk erased state is totempole configuration. The AC2 fuses associated with each of the outputs is included in all of the logic diagrams.

Power-Up Reset



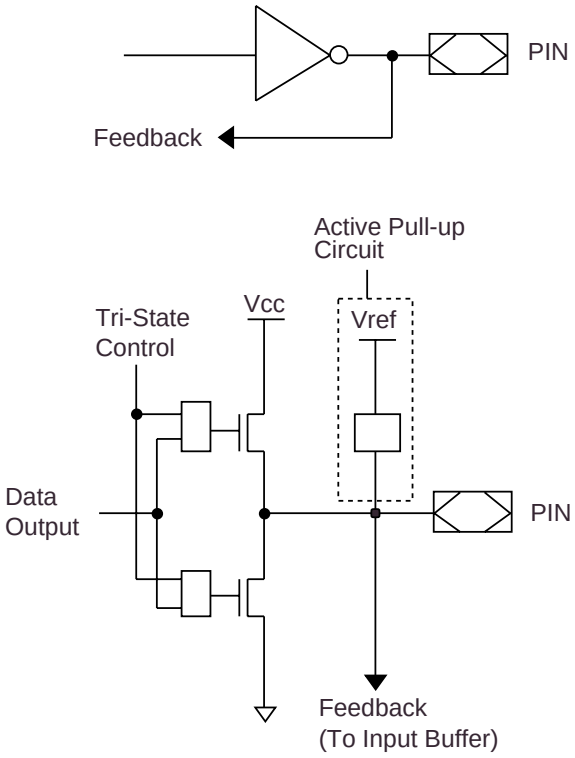
Circuitry within the GAL20VP8 provides a reset signal to all registers during power-up. All internal registers will have their Q outputs set low after a specified time (tpr, 1µs MAX). As a result, the state on the registered output pins (if they are enabled) will always be high on power-up, regardless of the programmed polarity of the output pins. This feature can greatly simplify state machine design by providing a known state on power-up. The timing diagram for power-up is shown above. Because of the asynchronous nature of system power-up, some conditions must be met to provide a valid power-up reset of the GAL20VP8. First, the V_{CC} rise must be monotonic. Second, the clock input must be at static TTL level as shown in the diagram during power up. The registers will reset within a maximum of tpr time. As in normal system operation, avoid clocking the device until all input and feedback path setup times have been met. The clock must also meet the minimum pulse width requirements.

Input/Output Equivalent Schematics



Vref = 3.1V

Typical Input

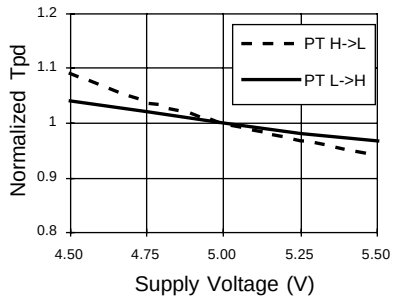


Vref = 3.1V

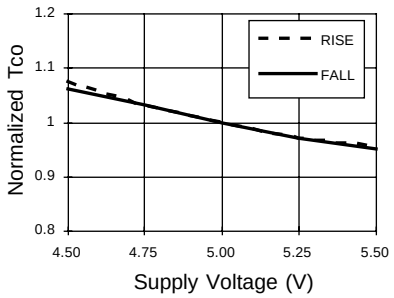
Typical Output

Typical AC and DC Characteristic Diagrams

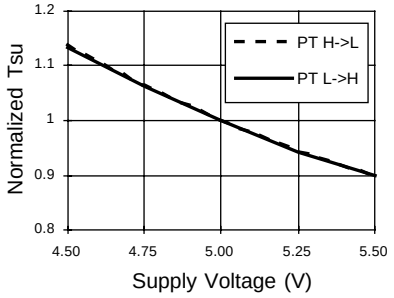
Normalized Tpd vs Vcc



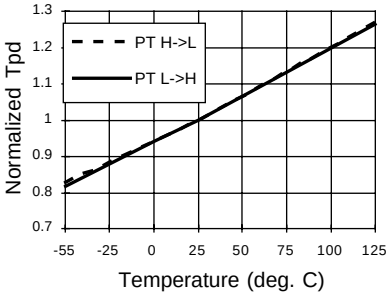
Normalized Tco vs Vcc



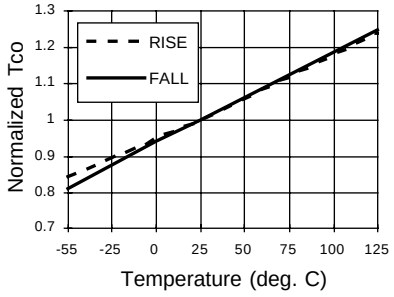
Normalized Tsu vs Vcc



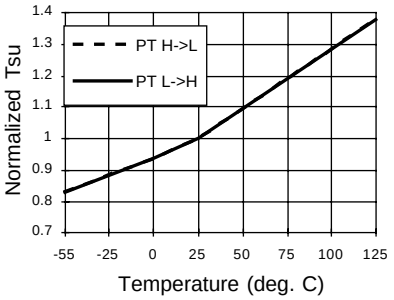
Normalized Tpd vs Temp



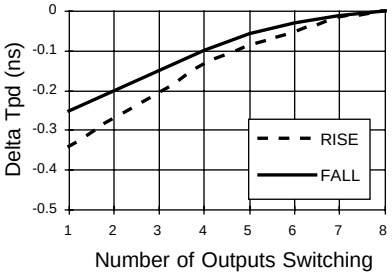
Normalized Tco vs Temp



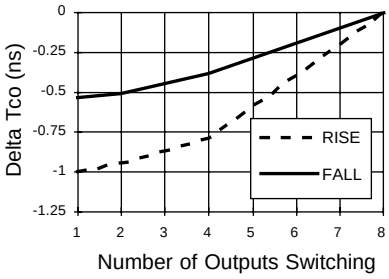
Normalized Tsu vs Temp



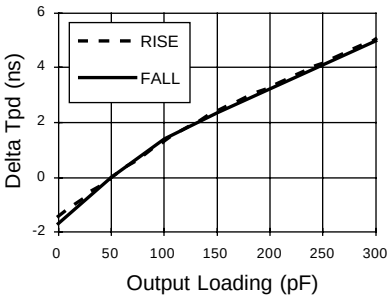
Delta Tpd vs # of Outputs Switching



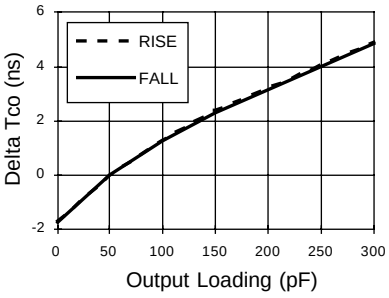
Delta Tco vs # of Outputs Switching



Delta Tpd vs Output Loading

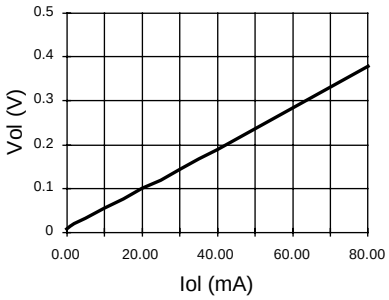


Delta Tco vs Output Loading

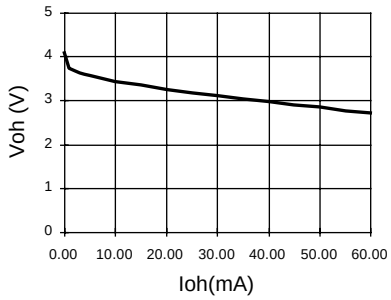


Typical AC and DC Characteristic Diagrams

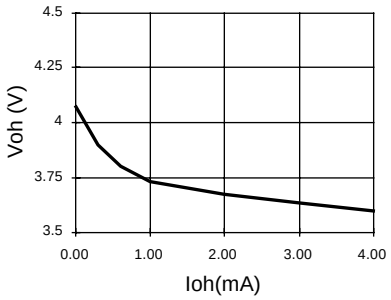
Vol vs Iol



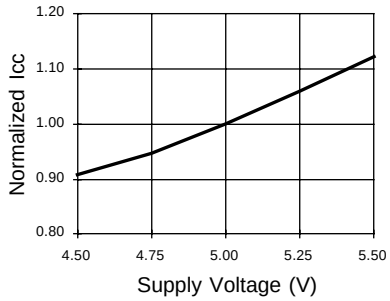
Voh vs Ioh



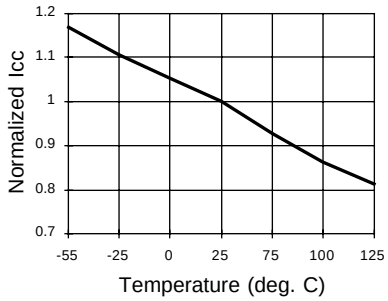
Voh vs Ioh



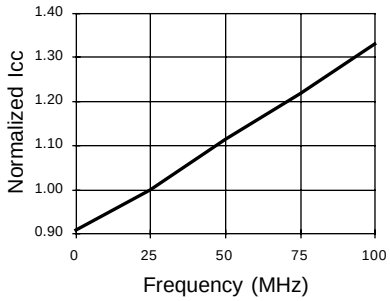
Normalized Icc vs Vcc



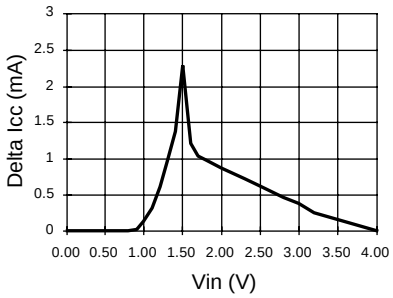
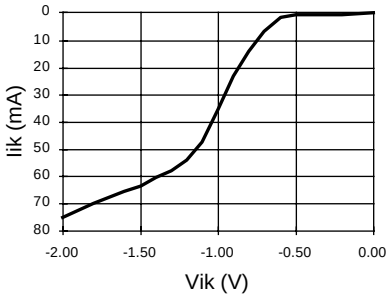
Normalized Icc vs Temp



Normalized Icc vs Freq.



Delta Icc vs Vin (1 input)



Input Clamp (Vik)