

# SN74SSTU32864 25-BIT CONFIGURABLE REGISTERED BUFFER WITH SSTL\_18 INPUTS AND OUTPUTS

SCES434 – MARCH 2003

- Member of the Texas Instruments Widebus+™ Family
- Pinout Optimizes DDR-II DIMM PCB Layout
- Configurable as 25-Bit 1:1 or 14-Bit 1:2 Registered Buffer
- Chip-Select Inputs Gate the Data Outputs from Changing State and Minimizes System Power Consumption
- Output Edge-Control Circuitry Minimizes Switching Noise in an Unterminated Line
- Supports SSTL\_18 Data Inputs
- Differential Clock (CLK and  $\overline{\text{CLK}}$ ) Inputs
- Supports LVCMOS Switching Levels on the Control and  $\overline{\text{RESET}}$  Inputs
- $\overline{\text{RESET}}$  Input Disables Differential Input Receivers, Resets All Registers, and Forces All Outputs Low
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 5000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## description/ordering information

This 25-bit 1:1 or 14-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V  $V_{CC}$  operation. In the 1:1 pinout configuration, only one device per DIMM is required to drive nine SDRAM loads. In the 1:2 pinout configuration, two devices per DIMM are required to drive 18 SDRAM loads.

All inputs are SSTL\_18, except the LVCMOS reset ( $\overline{\text{RESET}}$ ) and LVCMOS control (Cn) inputs. All outputs are edge-controlled circuits optimized for unterminated DIMM loads and meet SSTL\_18 specifications.

The SN74SSTU32864 operates from a differential clock (CLK and  $\overline{\text{CLK}}$ ). Data are registered at the crossing of CLK going high and  $\overline{\text{CLK}}$  going low.

The C0 input controls the pinout configuration of the 1:2 pinout from register-A configuration (when low) to register-B configuration (when high). The C1 input controls the pinout configuration from 25-bit 1:1 (when low) to 14-bit 1:2 (when high). C0 and C1 should not be switched during normal operation. They should be hard-wired to a valid low or high level to configure the register in the desired mode. In the 25-bit 1:1 pinout configuration, the A6, D6, and H6 terminals are driven low and should not be used.

The device supports low-power standby operation. When  $\overline{\text{RESET}}$  is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage ( $V_{REF}$ ) inputs are allowed. In addition, when  $\overline{\text{RESET}}$  is low, all registers are reset and all outputs are forced low. The LVCMOS  $\overline{\text{RESET}}$  and Cn inputs always must be held at a valid logic high or low level.

The two  $V_{REF}$  pins (A3 and T3), are connected together internally by approximately 150  $\Omega$ . However, it is necessary to connect only one of the two  $V_{REF}$  pins to the external  $V_{REF}$  power supply. An unused  $V_{REF}$  pin should be terminated with a  $V_{REF}$  coupling capacitor.

## ORDERING INFORMATION

TA	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	LFBGA – GKE	Tape and reel	SN74SSTU32864GKER	SU864

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

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# SN74SSTU32864

## 25-BIT CONFIGURABLE REGISTERED BUFFER

### WITH SSTL\_18 INPUTS AND OUTPUTS

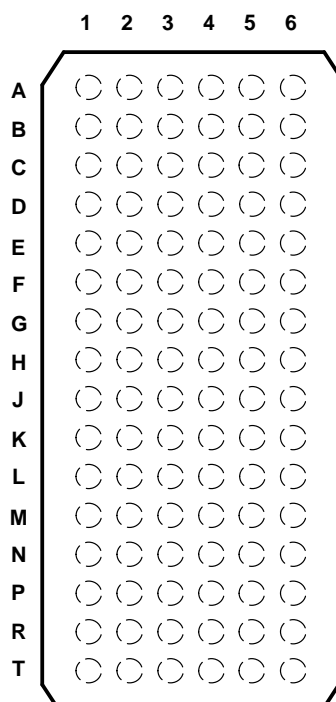
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#### description/ordering information (continued)

The device also supports low-power active operation by monitoring both system chip select ( $\overline{\text{DCS}}$  and  $\overline{\text{CSR}}$ ) inputs and will gate the Qn outputs from changing states when both  $\overline{\text{DCS}}$  and  $\overline{\text{CSR}}$  inputs are high. If either  $\overline{\text{DCS}}$  or  $\overline{\text{CSR}}$  input is low, the Qn outputs function normally. The RESET input has priority over the  $\overline{\text{DCS}}$  and  $\overline{\text{CSR}}$  control and forces the output low. If the  $\overline{\text{DCS}}$  control functionality is not desired, the  $\overline{\text{CSR}}$  input can be hard-wired to ground, in which case, the setup-time requirement for  $\overline{\text{DCS}}$  is the same as for the other D data inputs.

To ensure defined outputs from the register before a stable clock has been supplied, RESET must be held in the low state during power up.

GKE PACKAGE  
(TOP VIEW)



terminal assignments for 1:1 register (C0 = 0, C1 = 0)

	1	2	3	4	5	6
A	D1 (DCKE)	NC	VREF	VCC	Q1 (QCKE)	DNU
B	D2	D15	GND	GND	Q2	Q15
C	D3	D16	VCC	VCC	Q3	Q16
D	D4 (DODT)	NC	GND	GND	Q4 (QODT)	DNU
E	D5	D17	VCC	VCC	Q5	Q17
F	D6	D18	GND	GND	Q6	Q18
G	NC	RESET	VCC	VCC	C1	C0
H	CLK	D7 ( $\overline{\text{DCS}}$ )	GND	GND	Q7 ( $\overline{\text{QCS}}$ )	DNU
J	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	VCC	VCC	NC	NC
K	D8	D19	GND	GND	Q8	Q19
L	D9	D20	VCC	VCC	Q9	Q20
M	D10	D21	GND	GND	Q10	Q21
N	D11	D22	VCC	VCC	Q11	Q22
P	D12	D23	GND	GND	Q12	Q23
R	D13	D24	VCC	VCC	Q13	Q24
T	D14	D25	VREF	VCC	Q14	Q25

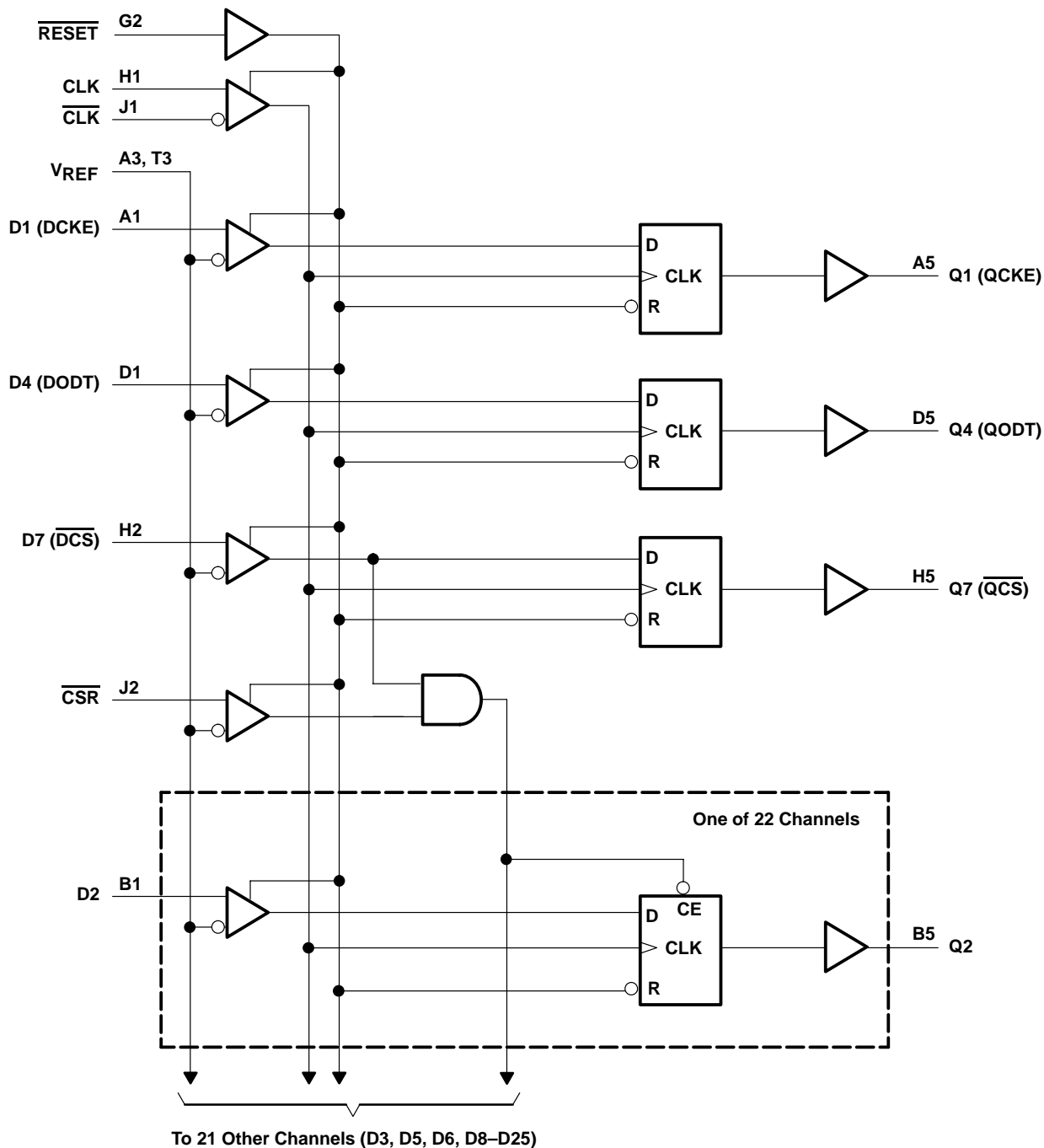
Each pin name in parentheses indicates the DDR-II DIMM signal name.

NC – No internal connection

DNU – Do not use

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logic diagram for 1:1 register configuration (positive logic)



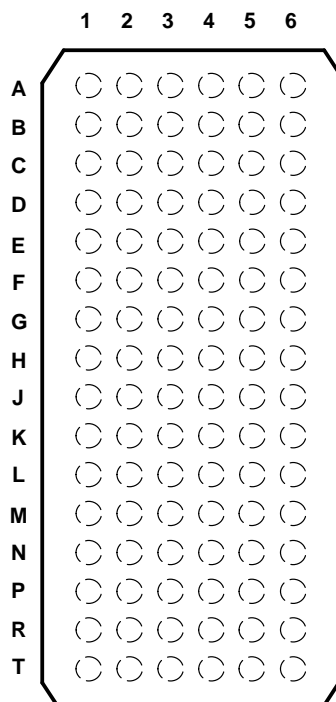
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### WITH SSTL\_18 INPUTS AND OUTPUTS

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**GKE PACKAGE  
(TOP VIEW)**



**terminal assignments for 1:2 register A (C0 = 0, C1 = 1)**

	1	2	3	4	5	6
A	D1 (DCKE)	NC	V <sub>REF</sub>	V <sub>CC</sub>	Q1A (QCKEA)	Q1B (QCKEB)
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q3A	Q3B
D	D4 (DODT)	NC	GND	GND	Q4A (QODTA)	Q4B (QODTB)
E	D5	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	$\overline{\text{RESET}}$	V <sub>CC</sub>	V <sub>CC</sub>	C1	C0
H	CLK	D7 ( $\overline{\text{DCS}}$ )	GND	GND	$\overline{\text{Q7A}}$ (QCSA)	$\overline{\text{Q7B}}$ (QCSB)
J	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	V <sub>CC</sub>	V <sub>CC</sub>	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q11A	Q11B
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	V <sub>CC</sub>	V <sub>CC</sub>	Q13A	Q13B
T	D14	DNU	V <sub>REF</sub>	V <sub>CC</sub>	Q14A	Q14B

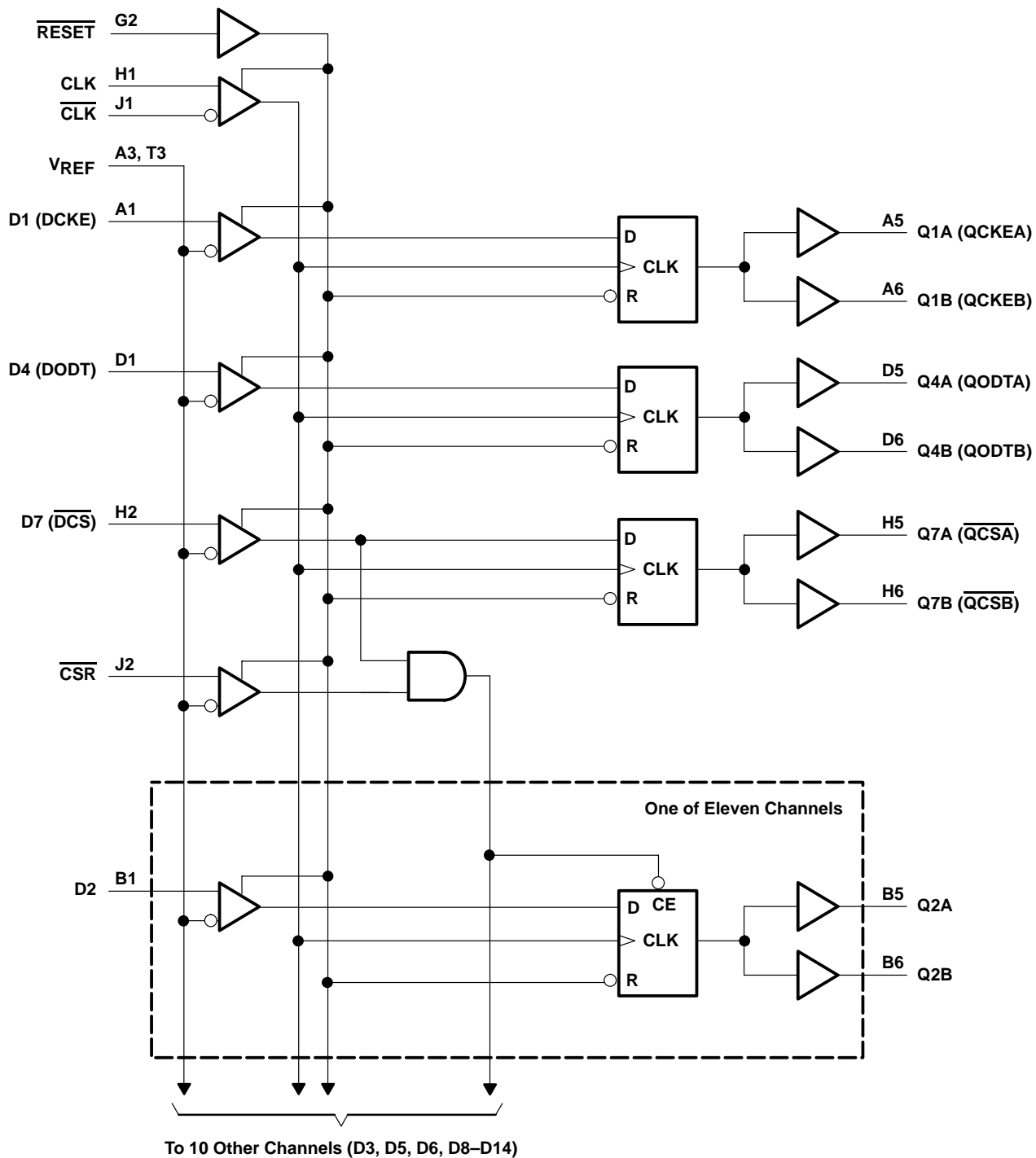
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logic diagram 1:2 register-A configuration (positive logic)



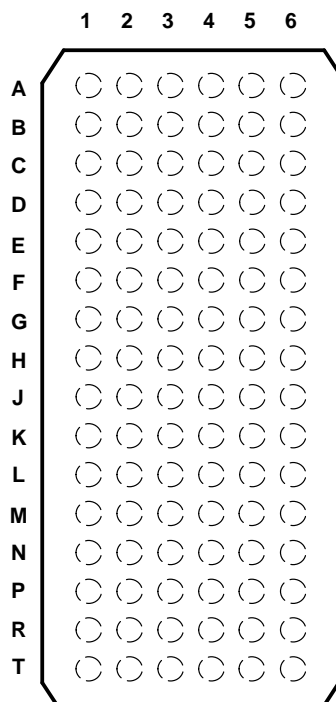
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## 25-BIT CONFIGURABLE REGISTERED BUFFER

### WITH SSTL\_18 INPUTS AND OUTPUTS

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**GKE PACKAGE  
(TOP VIEW)**



**terminal assignments for 1:2 register B (C0 = 1, C1 = 1)**

	1	2	3	4	5	6
A	D1	NC	VREF	VCC	Q1A	Q1B
B	D2	DNU	GND	GND	Q2A	Q2B
C	D3	DNU	VCC	VCC	Q3A	Q3B
D	D4	NC	GND	GND	Q4A	Q4B
E	D5	DNU	VCC	VCC	Q5A	Q5B
F	D6	DNU	GND	GND	Q6A	Q6B
G	NC	RESET	VCC	VCC	C1	C0
H	CLK	D7 ( $\overline{\text{DCS}}$ )	GND	GND	Q7A (QCSA)	Q7B (QCSB)
J	$\overline{\text{CLK}}$	$\overline{\text{CSR}}$	VCC	VCC	NC	NC
K	D8	DNU	GND	GND	Q8A	Q8B
L	D9	DNU	VCC	VCC	Q9A	Q9B
M	D10	DNU	GND	GND	Q10A	Q10B
N	D11 (DODT)	DNU	VCC	VCC	Q11A (QODTA)	Q11B (QODTB)
P	D12	DNU	GND	GND	Q12A	Q12B
R	D13	DNU	VCC	VCC	Q13A	Q13B
T	D14 (DCKE)	DNU	VREF	VCC	Q14A (QCKEA)	Q14B (QCKEB)

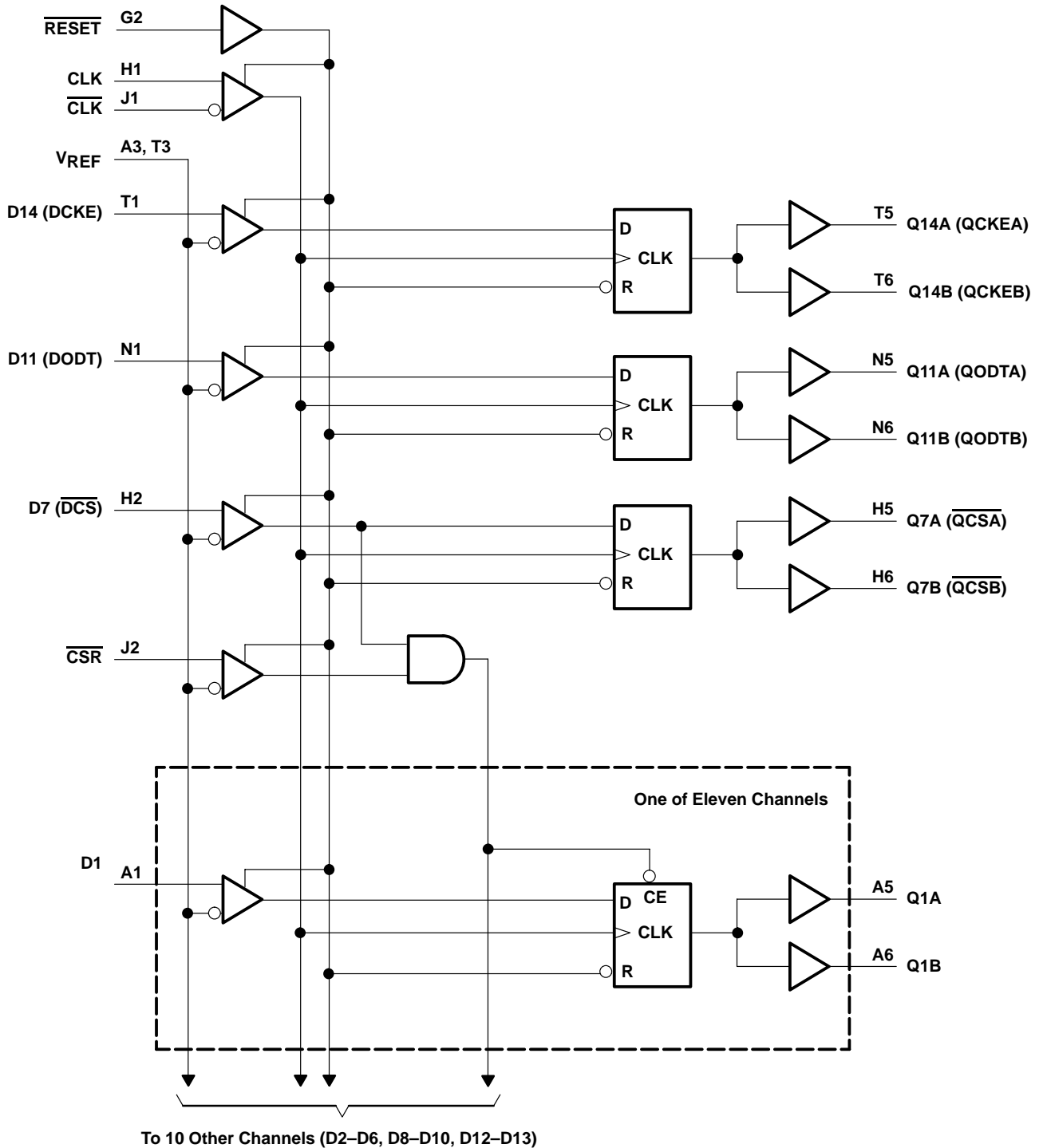
Each pin name in parentheses indicates the DDR-II DIMM signal name.

NC – No internal connection

DNU – Do not use

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logic diagram 1:2 register-B configuration (positive logic)



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#### TERMINAL FUNCTIONS

TERMINAL NAME	DESCRIPTION	ELECTRICAL CHARACTERISTICS
GND	Ground	Ground input
VCC	Power-supply voltage	1.8 V nominal
VREF	Input reference voltage	0.9 V nominal
CLK	Positive master clock input	Differential input
$\overline{\text{CLK}}$	Negative master clock input	Differential input
C0, C1	Configuration control inputs – Register A, Register B, 1:1, 1:2 select	LVC MOS inputs
$\overline{\text{RESET}}$	Asynchronous reset input – resets registers and disables VREF data and clock differential-input receivers	LVC MOS input
D1–D25	Data inputs – clocked in on the crossing of the rising edge of CLK and the falling edge of $\overline{\text{CLK}}$	SSTL_18 inputs
$\overline{\text{CSR}}, \overline{\text{DCS}}$	Chip select inputs – disables D1–D25 <sup>†</sup> outputs switching when both inputs are high	SSTL_18 inputs
DODT	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	SSTL_18 input
DCKE	The outputs of this register bit will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control.	SSTL_18 input
Q1–Q25 <sup>‡</sup>	Data outputs that are suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control	1.8 V CMOS outputs
$\overline{\text{QCS}}$	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control	1.8 V CMOS output
QODT	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control	1.8 V CMOS output
QCKE	Data output that will not be suspended by the $\overline{\text{DCS}}$ and $\overline{\text{CSR}}$ control	1.8 V CMOS output
NC	No internal connection	
DNU	Do not use – inputs are in standby-equivalent mode, and outputs are driven low.	

<sup>†</sup> Data inputs = D2, D3, D5, D6, D8–D25 when C0 = 0 and C1 = 0

Data inputs = D2, D3, D5, D6, D8–D14 when C0 = 0 and C1 = 1

Data inputs = D1–D6, D8–D10, D12, D13 when C0 = 1 and C1 = 1.

<sup>‡</sup> Data outputs = Q2, Q3, Q5, Q6, Q8–Q25 when C0 = 0 and C1 = 0

Data outputs = Q2, Q3, Q5, Q6, Q8–Q14 when C0 = 0 and C1 = 1

Data outputs = Q1–Q6, Q8–Q10, Q12, Q13 when C0 = 1 and C1 = 1.



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FUNCTION TABLES

INPUTS						OUTPUT Qn
RESET	DCS	CSR	CLK	CLK	Dn	
H	L	X	↑	↓	L	L
H	L	X	↑	↓	H	H
H	X	L	↑	↓	L	L
H	X	L	↑	↓	H	H
H	H	H	↑	↓	X	Q <sub>0</sub>
H	X	X	L or H	L or H	X	Q <sub>0</sub>
L	X or floating	X or floating	X or floating	X or floating	X or floating	L

INPUTS				OUTPUTS
RESET	CLK	CLK	DCKE, DCS, DODT	
H	↑	↓	H	H
H	↑	↓	L	L
H	L or H	L or H	X	Q <sub>0</sub>
L	X or floating	X or floating	X or floating	L

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>**

Supply voltage range, $V_{CC}$	–0.5 V to 2.5 V
Input voltage range, $V_I$ (see Notes 1 and 2)	–0.5 V to 2.5 V
Output voltage range, $V_O$ (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ )	±50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	±50 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±50 mA
Continuous current through each $V_{CC}$ or GND	±100 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3)	36°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
2. This value is limited to 2.5 V maximum.  
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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### WITH SSTL\_18 INPUTS AND OUTPUTS

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#### recommended operating conditions (see Note 4)

			MIN	NOM	MAX	UNIT
V <sub>CC</sub>	Supply voltage		1.7		1.9	V
V <sub>REF</sub>	Reference voltage		0.49 × V <sub>CC</sub>	0.5 × V <sub>CC</sub>	0.51 × V <sub>CC</sub>	V
V <sub>I</sub>	Input voltage		0		V <sub>CC</sub>	V
V <sub>IH</sub>	AC high-level input voltage	Data inputs, $\overline{\text{CSR}}$	V <sub>REF</sub> +250 mV			V
V <sub>IL</sub>	AC low-level input voltage	Data inputs, $\overline{\text{CSR}}$	V <sub>REF</sub> −250 mV			V
V <sub>IH</sub>	DC high-level input voltage	Data inputs, $\overline{\text{CSR}}$	V <sub>REF</sub> +125 mV			V
V <sub>IL</sub>	DC low-level input voltage	Data inputs, $\overline{\text{CSR}}$	V <sub>REF</sub> −125 mV			V
V <sub>IH</sub>	High-level input voltage	$\overline{\text{RESET}}$ , Cn	0.65 × V <sub>CC</sub>			V
V <sub>IL</sub>	Low-level input voltage	$\overline{\text{RESET}}$ , Cn	0.35 × V <sub>CC</sub>			V
V <sub>ICR</sub>	Common-mode input voltage range	CLK, $\overline{\text{CLK}}$	0.675		1.125	V
V <sub>I(PP)</sub>	Peak-to-peak input voltage	CLK, $\overline{\text{CLK}}$	600			mV
I <sub>OH</sub>	High-level output current		−8			mA
I <sub>OL</sub>	Low-level output current		8			
T <sub>A</sub>	Operating free-air temperature		0		70	°C

NOTE 4: The  $\overline{RESET}$  and Cn inputs of the device must be held at valid logic voltage levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless  $\overline{RESET}$  is low. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		V <sub>CC</sub>	MIN	TYP†	MAX	UNIT
V <sub>OH</sub>		I <sub>OH</sub> = −100 μA		1.7 V to 1.9 V	V <sub>CC</sub> −0.2			V
		I <sub>OH</sub> = −6 mA		1.7 V	1.2			
V <sub>OL</sub>		I <sub>OL</sub> = 100 μA		1.7 V to 1.9 V	0.2			V
		I <sub>OL</sub> = 6 mA		1.7 V	0.5			
I <sub>I</sub>	All inputs‡	V <sub>I</sub> = V <sub>CC</sub> or GND		1.9 V	±5			μA
I <sub>CC</sub>	Static standby	RESET = GND		1.9 V	100			μA
	Static operating	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH</sub> (AC) or V <sub>IL</sub> (AC)			40			mA
I <sub>CCD</sub>	Dynamic operating – clock only	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH</sub> (AC) or V <sub>IL</sub> (AC), CLK and CLK switching 50% duty cycle		1.8 V	28			μA/MHz
	Dynamic operating – per each data input, 1:1 configuration	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH</sub> (AC) or V <sub>IL</sub> (AC), CLK and CLK switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle			18			μA/clock MHz/D input
	Dynamic operating – per each data input, 1:2 configuration				36			
I <sub>CCDLP</sub>	Chip-select-enabled low-power active mode – clock only	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH</sub> (AC) or V <sub>IL</sub> (AC), CLK and CLK switching 50% duty cycle		1.8 V	27			μA/MHz
	Chip-select-enabled low-power active mode – 1:1 configuration	RESET = V <sub>CC</sub> , V <sub>I</sub> = V <sub>IH</sub> (AC) or V <sub>IL</sub> (AC), CLK and CLK switching 50% duty cycle, One data input switching at one-half clock frequency, 50% duty cycle			2			μA/clock MHz/D input
	Chip-select-enabled low-power active mode – 1:2 configuration				2			
C <sub>i</sub>	Data inputs, CSR	V <sub>I</sub> = V <sub>REF</sub> ± 250 mV		1.8 V	2.5	3	3.5	pF
	CLK, CLK	V <sub>ICR</sub> = 0.9 V, V <sub>I</sub> (PP) = 600 mV			2	3		
	RESET	V <sub>I</sub> = V <sub>CC</sub> or GND			2.5			

† All typical values are at V<sub>CC</sub> = 1.8 V, T<sub>A</sub> = 25°C.

‡ Each V<sub>REF</sub> pin (A3 or T3) should be tested independently, with the other (untested) pin open.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 and Note 5)**

		MIN	MAX	UNIT
f <sub>clock</sub>	Clock frequency		500	MHz
t <sub>w</sub>	Pulse duration, CLK, $\overline{\text{CLK}}$ high or low	1		ns
t <sub>act</sub>	Differential inputs active time (see Note 6)		10	ns
t <sub>inact</sub>	Differential inputs inactive time (see Note 7)		15	ns
t <sub>su</sub>	Setup time	$\overline{\text{DCS}}$ before CLK↑, $\overline{\text{CLK}}$ ↓, $\overline{\text{CSR}}$ high; $\overline{\text{CSR}}$ before CLK↑, $\overline{\text{CLK}}$ ↓, $\overline{\text{DCS}}$ high		0.7
		$\overline{\text{DCS}}$ before CLK↑, $\overline{\text{CLK}}$ ↓, $\overline{\text{CSR}}$ low		0.5
		DODT, DCKE, and Data before CLK↑, $\overline{\text{CLK}}$ ↓		0.5
t <sub>h</sub>	Hold time	$\overline{\text{DCS}}$ , DODT, DCKE, and Data after CLK↑, $\overline{\text{CLK}}$ ↓		0.5

NOTES: 5. All input slew rates are 1 V/ns ±20%.

6. V<sub>REF</sub> must be held at a valid input level and data inputs must be held low for a minimum time of t<sub>act</sub> max, after RESET is taken high.

7. V<sub>REF</sub>, data, and clock inputs must be held at valid voltage levels (not floating) for a minimum time of t<sub>inact</sub> max, after RESET is taken low.

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**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.1\text{ V}$		UNIT
			MIN	MAX	
$f_{\max}$			500		MHz
$t_{\text{pdm}}^{\dagger}$	CLK and $\overline{\text{CLK}}$	Q	1.4	2.5	ns
$t_{\text{pdmss}}^{\dagger}$	CLK and $\overline{\text{CLK}}$	Q		2.7	ns
$t_{\text{RPHL}}^{\dagger}$	$\overline{\text{RESET}}$	Q		3	ns

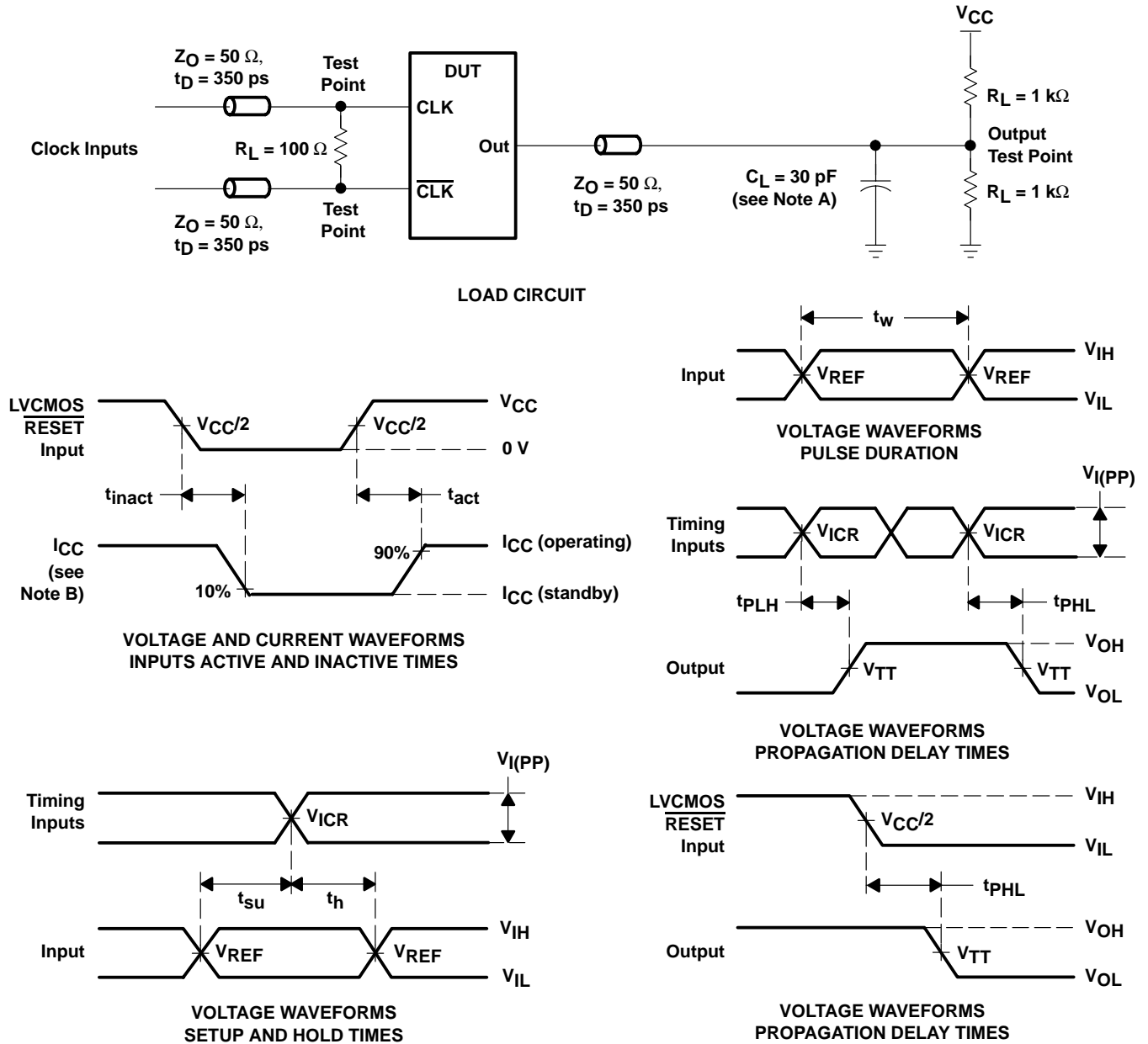
<sup>†</sup> Includes 350-ps test-load transmission-line delay

**output slew rates over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)**

PARAMETER	FROM	TO	$V_{CC} = 1.8\text{ V}$ $\pm 0.1\text{ V}$		UNIT
			MIN	MAX	
$dV/dt_r$	20%	80%	1.9	4.9	V/ns
$dV/dt_f$	80%	20%	1.9	4.9	V/ns
$dV/dt_{\Delta}^{\S}$	20% or 80%	80% or 20%		1	V/ns

<sup>§</sup> Difference between  $dV/dt_r$  (rising edge rate) and  $dV/dt_f$  (falling edge rate)

## PARAMETER MEASUREMENT INFORMATION



- NOTES:
- $C_L$  includes probe and jig capacitance.
  - $I_{CC}$  tested with clock and data inputs held at  $V_{CC}$  or GND, and  $I_O = 0\ \text{mA}$ .
  - All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\ \text{MHz}$ ,  $Z_O = 50\ \Omega$ , input slew rate =  $1\ \text{V/ns} \pm 20\%$  (unless otherwise noted).
  - The outputs are measured one at a time with one transition per measurement.
  - $V_{\text{REF}} = V_{CC}/2$
  - $V_{IH} = V_{\text{REF}} + 250\ \text{mV}$  (ac voltage levels) for differential inputs.  $V_{IH} = V_{CC}$  for LVC MOS input.
  - $V_{IL} = V_{\text{REF}} - 250\ \text{mV}$  (ac voltage levels) for differential inputs.  $V_{IL} = \text{GND}$  for LVC MOS input.
  - $V_{I(\text{PP})} = 600\ \text{mV}$
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

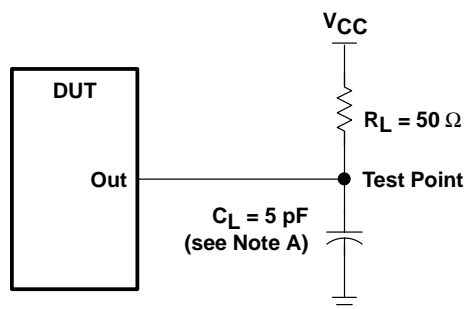
# SN74SSTU32864

## 25-BIT CONFIGURABLE REGISTERED BUFFER

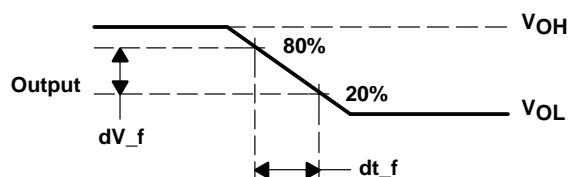
### WITH SSTL\_18 INPUTS AND OUTPUTS

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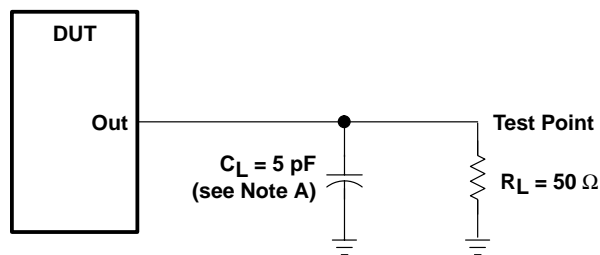
#### PARAMETER MEASUREMENT INFORMATION



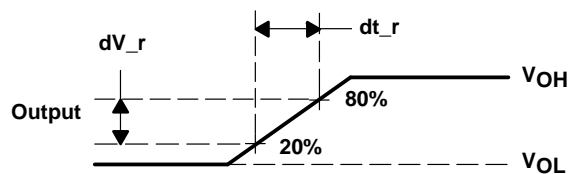
LOAD CIRCUIT  
HIGH-TO-LOW SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS  
HIGH-TO-LOW SLEW-RATE MEASUREMENT



LOAD CIRCUIT  
LOW-TO-HIGH SLEW-RATE MEASUREMENT



VOLTAGE WAVEFORMS  
LOW-TO-HIGH SLEW-RATE MEASUREMENT

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. All input pulses are supplied by generators having the following characteristics:  
PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ , input slew rate =  $1 \text{ V/ns} \pm 20\%$  (unless otherwise specified).

Figure 2. Output Slew-Rate Measurement Information

## PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74SSTU32864GKER	ACTIVE	LFBGA	GKE	96	1000	TBD	/	Level-3-220C-168 HR
SN74SSTU32864ZKER	ACTIVE	LFBGA	ZKE	96	1000	Green (RoHS & no Sb/Br)	/	Level-3-250C-1WEEK

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

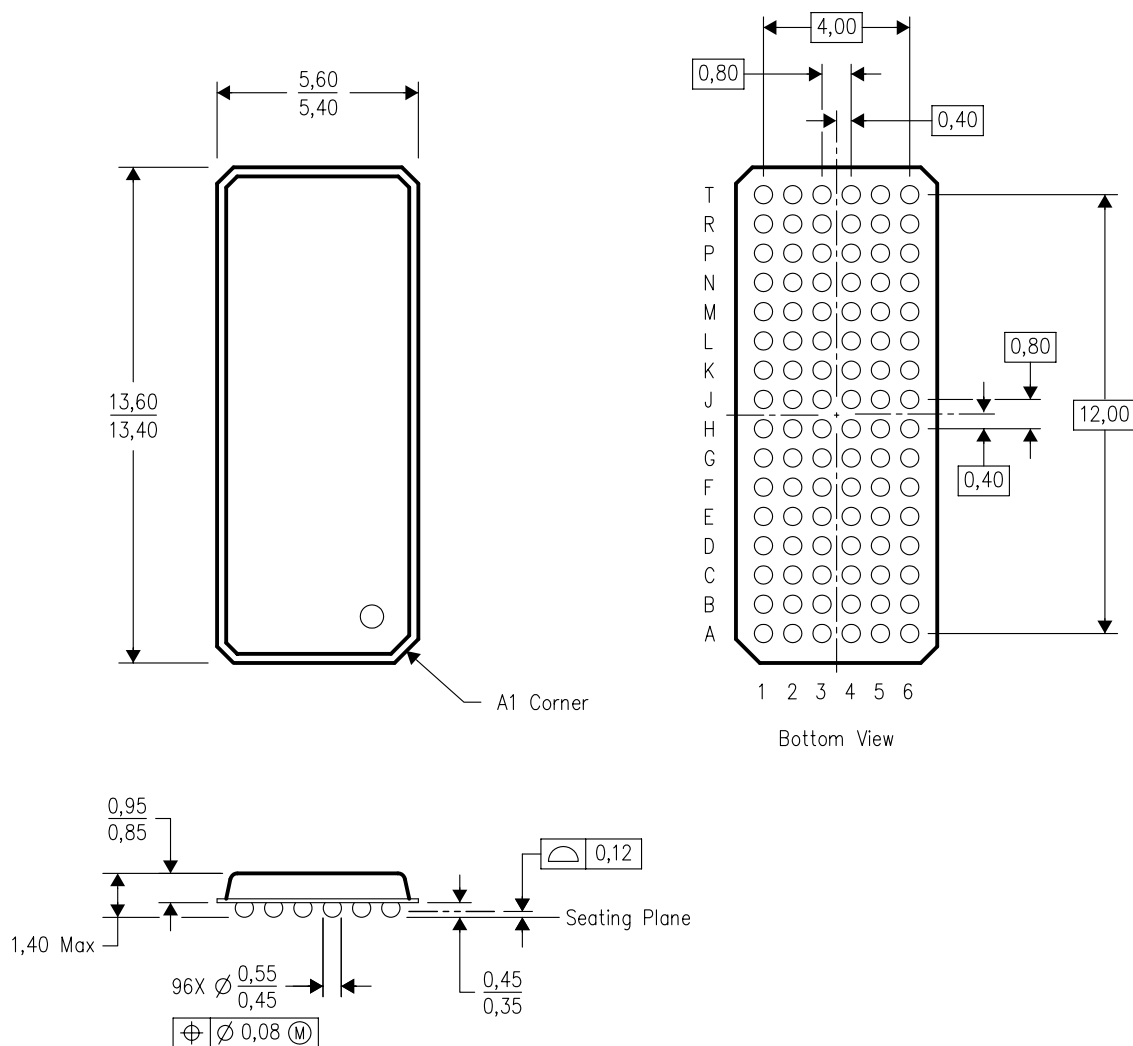
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## MECHANICAL DATA

GKE (R-PBGA-N96)

## PLASTIC BALL GRID ARRAY



4188953/F 06/04

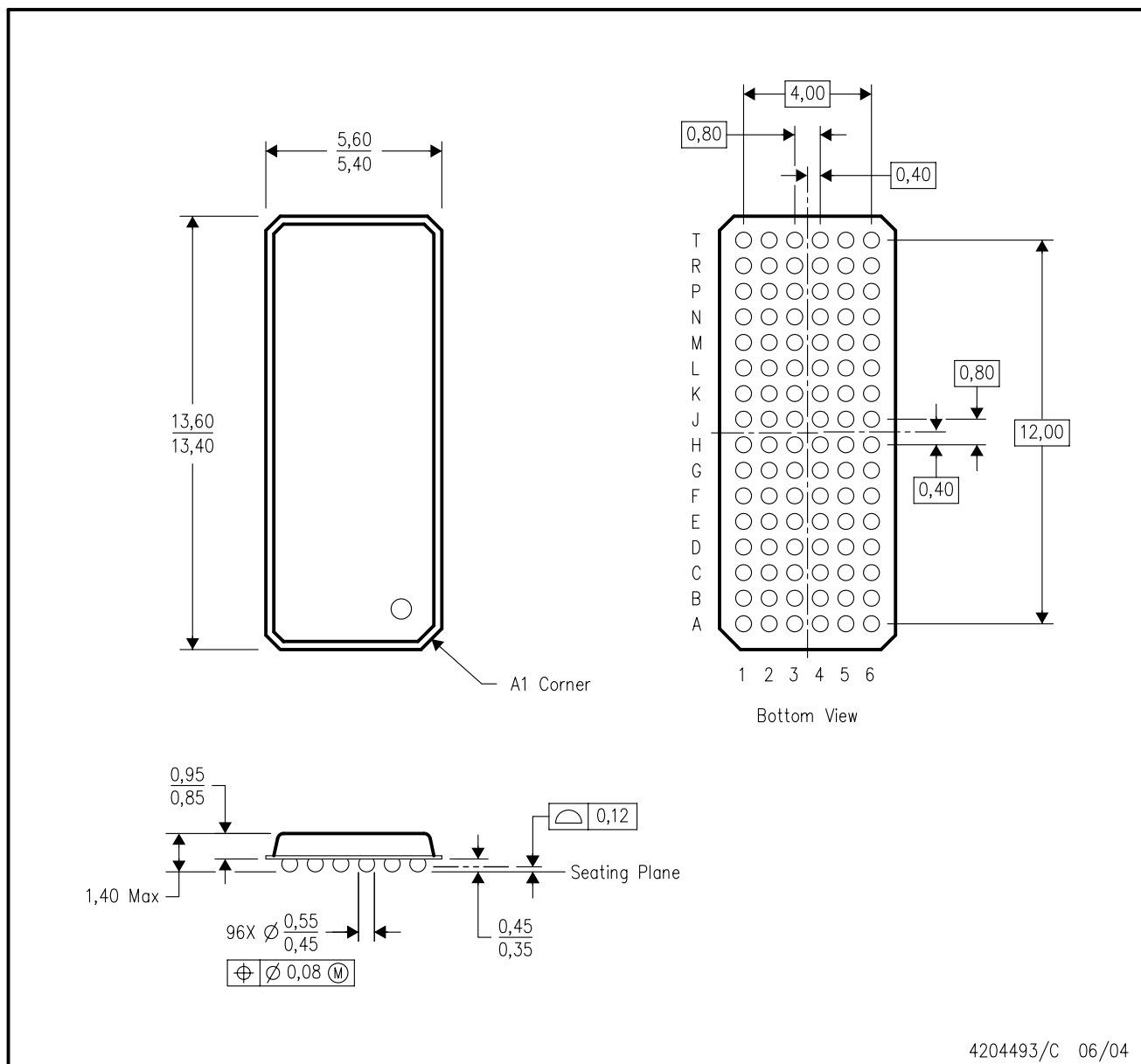
- NOTES: A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Falls within JEDEC MO-205 variation CC.  
D. This package is tin-lead (SnPb). Refer to the 96 ZKE package (drawing 4204493) for lead-free.



## MECHANICAL DATA

ZKE (R-PBGA-N96)

PLASTIC BALL GRID ARRAY



4204493/C 06/04

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