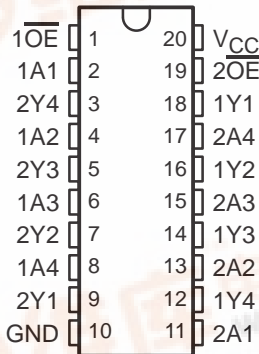


# SN54LVTH240, SN74LVTH240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

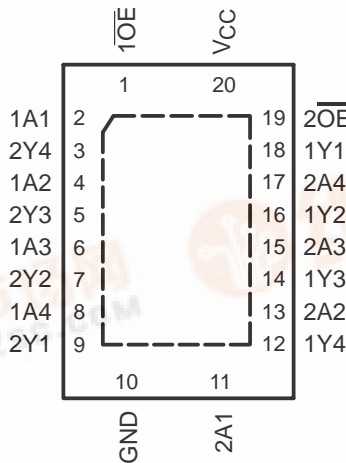
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- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

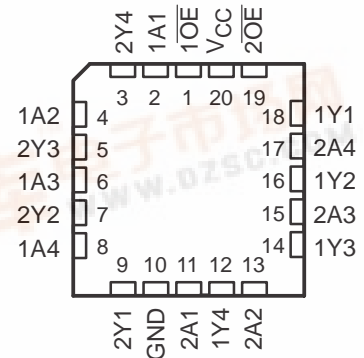
SN54LVTH240 ... J OR W PACKAGE  
SN74LVTH240 ... DB, DW, NS,  
OR PW PACKAGE  
(TOP VIEW)



SN74LVTH240 ... RGY PACKAGE  
(TOP VIEW)



SN54LVTH240 ... FK PACKAGE  
(TOP VIEW)



## description/ordering information

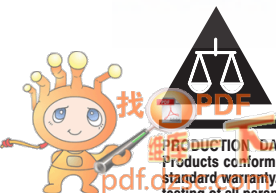
These octal buffers and line drivers are designed specifically for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Tape and reel	SN74LVTH240RGYR	LXH240
	SOIC – DW	Tube	SN74LVTH240DW	LVTH240
		Tape and reel	SN74LVTH240DWR	
	SOP – NS	Tape and reel	SN74LVTH240NSR	LVTH240
	SSOP – DB	Tape and reel	SN74LVTH240DBR	LXH240
	TSSOP – PW	Tube	SN74LVTH240PW	LXH240
		Tape and reel	SN74LVTH240PWR	
-55°C to 125°C	VFBGA – GQN	Tape and reel	SN74LVTH240GQNR	LXH240
	VFBGA – ZQN (Pb-free)		SN74LVTH240ZQNR	
	CDIP – J	Tube	SNJ54LVTH240J	SNJ54LVTH240J
	CFP – W	Tube	SNJ54LVTH240W	SNJ54LVTH240W
	LCCC – FK	Tube	SNJ54LVTH240FK	SNJ54LVTH240FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



SN54LVTH240, SN74LVTH240  
3.3-V ABT OCTAL BUFFERS/DRIVERS  
WITH 3-STATE OUTPUTS

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description/ordering information (continued)

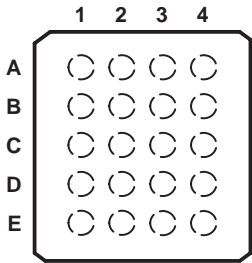
These devices are organized as two 4-bit buffer/line drivers with separate output-enable ( $\overline{\text{OE}}$ ) inputs. When  $\overline{\text{OE}}$  is low, the devices pass data from the A inputs to the Y outputs. When  $\overline{\text{OE}}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{\text{OE}}$  should be tied to  $V_{\text{CC}}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

These devices are fully specified for hot-insertion applications using  $I_{\text{off}}$  and power-up 3-state. The  $I_{\text{off}}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

SN74LVTH240 . . . GQN OR ZQN PACKAGE  
(TOP VIEW)



terminal assignments

	1	2	3	4
A	1A1	$1\overline{\text{OE}}$	$V_{\text{CC}}$	$2\overline{\text{OE}}$
B	1A2	2A4	2Y4	1Y1
C	1A3	2Y3	2A3	1Y2
D	1A4	2A2	2Y2	1Y3
E	GND	2Y1	2A1	1Y4

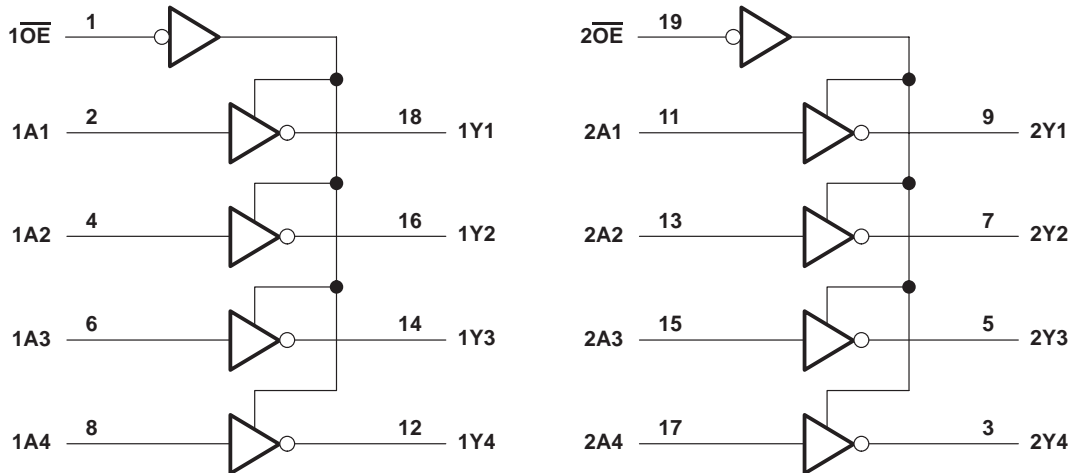
FUNCTION TABLE  
(each 4-bit buffer)

INPUTS		OUTPUT Y
$\overline{\text{OE}}$	A	
L	H	L
L	L	H
H	X	Z

# SN54LVTH240, SN74LVTH240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## logic diagram (positive logic)



Pin numbers shown are for the DB, DW, FK, J, NS, PW, RGY, and W packages.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_{OL}$ : SN54LVTH240	96 mA
SN74LVTH240	128 mA
Current into any output in the high state, $I_{OH}$ (see Note 2): SN54LVTH240	48 mA
SN74LVTH240	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ )	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ )	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DB package	70°C/W
(see Note 3): DW package	58°C/W
(see Note 3): GQN/ZQN package	78°C/W
(see Note 3): NS package	60°C/W
(see Note 3): PW package	83°C/W
(see Note 4): RGY package	37°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
  2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .
  3. The package thermal impedance is calculated in accordance with JESD 51-7.
  4. The package thermal impedance is calculated in accordance with JESD 51-5.

# SN54LVTH240, SN74LVTH240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

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## recommended operating conditions (see Note 5)

		SN54LVTH240		SN74LVTH240		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		$\mu$ s/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 5: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54LVTH240, SN74LVTH240

## 3.3-V ABT OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN54LVTH240			SN74LVTH240			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$		$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$			-1.2			-1.2	V
$V_{OH}$		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.2$			$V_{CC}-0.2$			V
		$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$	2.4			2.4			
		$V_{CC} = 3\text{ V}$	2			2			
$V_{OL}$		$V_{CC} = 2.7\text{ V}$		$I_{OL} = 100\text{ }\mu\text{A}$	0.2		$I_{OL} = 100\text{ }\mu\text{A}$	0.2	V
				$I_{OL} = 24\text{ mA}$	0.5		$I_{OL} = 24\text{ mA}$	0.5	
		$V_{CC} = 3\text{ V}$		$I_{OL} = 16\text{ mA}$	0.4		$I_{OL} = 16\text{ mA}$	0.4	
				$I_{OL} = 32\text{ mA}$	0.5		$I_{OL} = 32\text{ mA}$	0.5	
				$I_{OL} = 48\text{ mA}$	0.55		$I_{OL} = 48\text{ mA}$	0.55	
				$I_{OL} = 64\text{ mA}$			$I_{OL} = 64\text{ mA}$	0.55	
$I_I$	Control inputs	$V_{CC} = 0\text{ or }3.6\text{ V}$ , $V_I = 5.5\text{ V}$			10			10	$\mu\text{A}$
		$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$			$\pm 1$			$\pm 1$	
	Data inputs	$V_{CC} = 3.6\text{ V}$		$V_I = V_{CC}$	1			1	
				$V_I = 0$	-5			-5	
$I_{off}$		$V_{CC} = 0$ , $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$						$\pm 100$	$\mu\text{A}$
$I_{I(hold)}$	Data inputs	$V_{CC} = 3\text{ V}$		$V_I = 0.8\text{ V}$	75			75	$\mu\text{A}$
				$V_I = 2\text{ V}$	-75			-75	
		$V_{CC} = 3.6\text{ V}^\ddagger$ , $V_I = 0\text{ to }3.6\text{ V}$						500 -750	
$I_{OZH}$		$V_{CC} = 3.6\text{ V}$ , $V_O = 3\text{ V}$			5			5	$\mu\text{A}$
$I_{OZL}$		$V_{CC} = 3.6\text{ V}$ , $V_O = 0.5\text{ V}$			-5			-5	$\mu\text{A}$
$I_{OZPU}$		$V_{CC} = 0\text{ to }1.5\text{ V}$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $OE = \text{don't care}$			$\pm 100^*$			$\pm 100$	$\mu\text{A}$
$I_{OZPD}$		$V_{CC} = 1.5\text{ V to }0$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $OE = \text{don't care}$			$\pm 100^*$			$\pm 100$	$\mu\text{A}$
$I_{CC}$		$V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$		Outputs high	0.19			0.19	mA
				Outputs low	5			5	
				Outputs disabled	0.19			0.19	
$\Delta I_{CC}^\S$		$V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$			0.2			0.2	mA
$C_i$		$V_I = 3\text{ V or }0$			3			3	pF
$C_o$		$V_O = 3\text{ V or }0$			7			7	pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

§ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

# SN54LVTH240, SN74LVTH240

## 3.3-V ABT OCTAL BUFFERS/DRIVERS

### WITH 3-STATE OUTPUTS

SCBS679K – DECEMBER 1996 – REVISED SEPTEMBER 2003

switching characteristics over recommended ranges of supply voltage and operating free-air temperature,  $C_L = 50$  pF (unless otherwise noted) (see Figure 1)

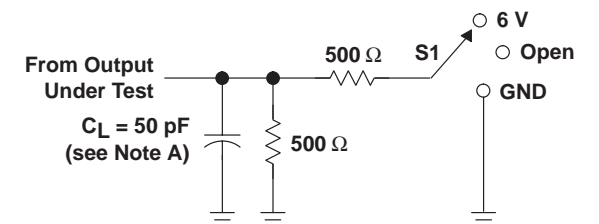
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH240				SN74LVTH240				UNIT	
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
t <sub>PLH</sub>	A	Y	0.9	4.3	5.1		1.1	2.2	3.8	4.6		ns
t <sub>PHL</sub>			1.2	4.7	4.9		1.3	2.6	4	4.2		
t <sub>PZH</sub>	$\overline{OE}$	Y	1	5.7	6.7		1.1	2.6	4.6	5.6		ns
t <sub>PZL</sub>			1.2	5.5	6.2		1.4	2.7	4.4	5		
t <sub>PHZ</sub>	$\overline{OE}$	Y	1	5.1	5.2		2	2.9	4.4	4.6		ns
t <sub>PLZ</sub>			1.1	5.4	5.4		1.8	3	4.3	4.3		

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

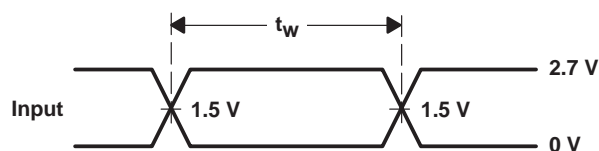
# SN54LVTH240, SN74LVTH240 3.3-V ABT OCTAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

SCBS679K – DECEMBER 1996 – REVISED SEPTEMBER 2003

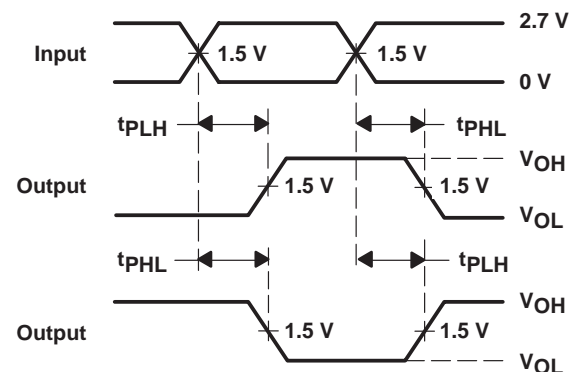
## PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

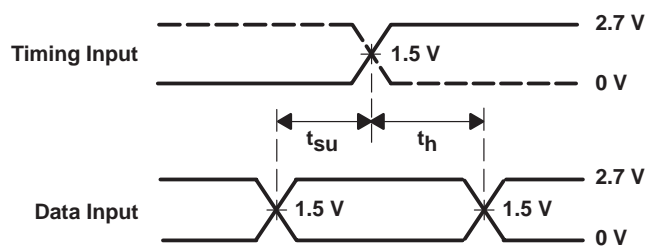


VOLTAGE WAVEFORMS  
PULSE DURATION

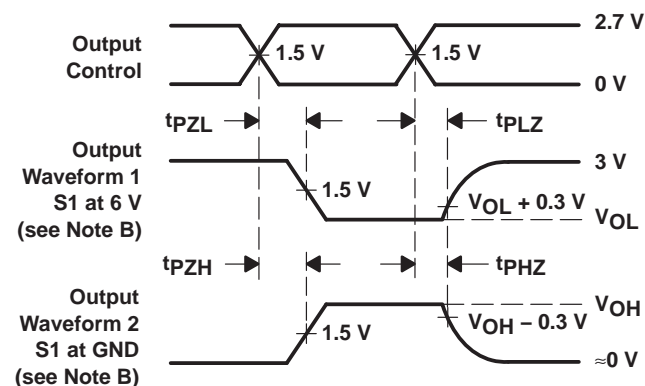


VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

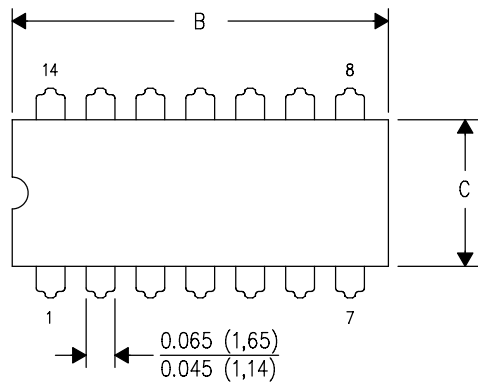
- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

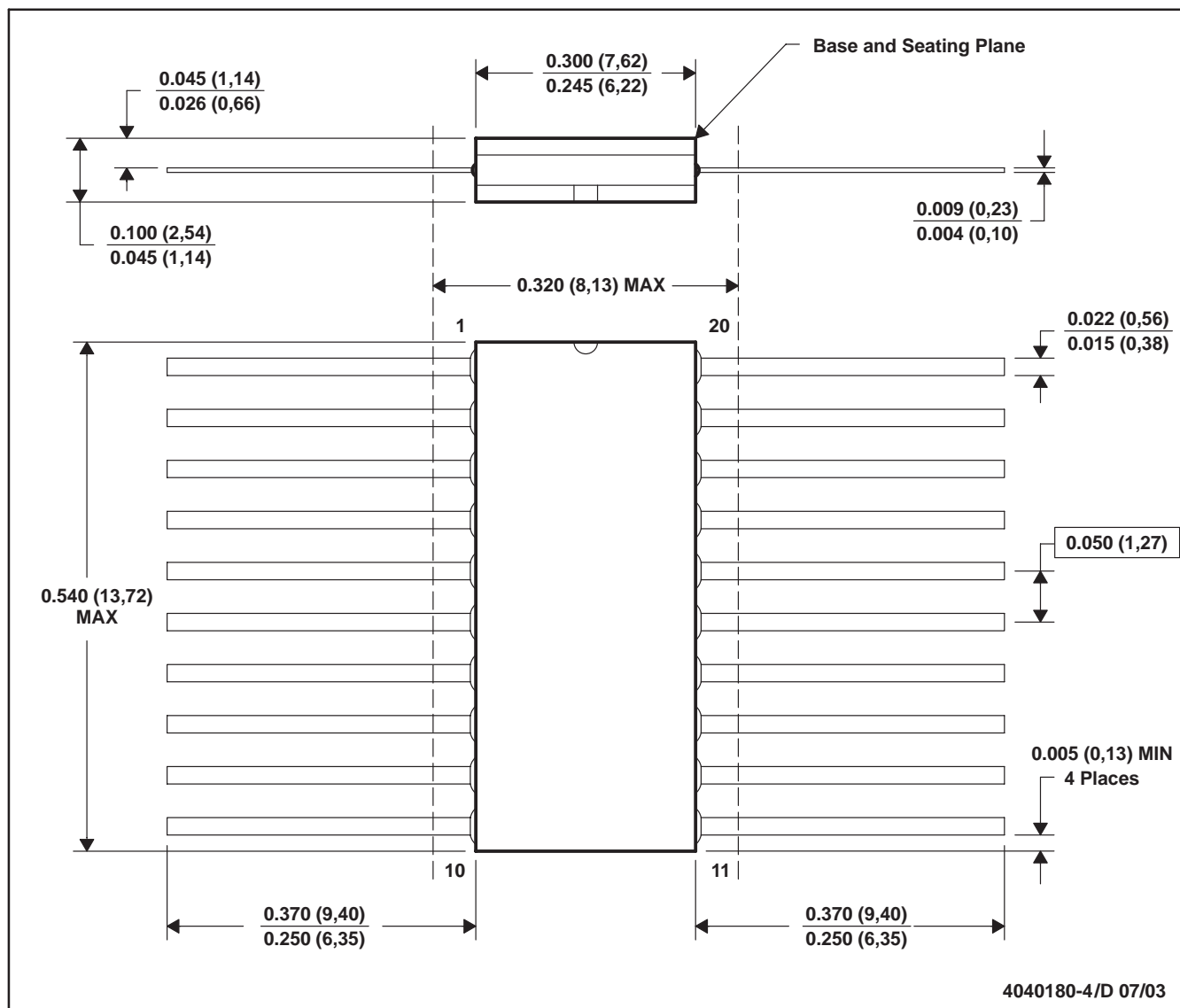


## MECHANICAL DATA

MCFP006B – JANUARY 1995 – REVISED JULY 2003

**W (R-GDFP-F20)**

## CERAMIC DUAL FLATPACK



- NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.  
C. This package can be hermetically sealed with a ceramic lid using glass frit.  
D. Index point is provided on cap for terminal identification only.  
E. Falls within Mil-Std 1835 GDFP2-F20

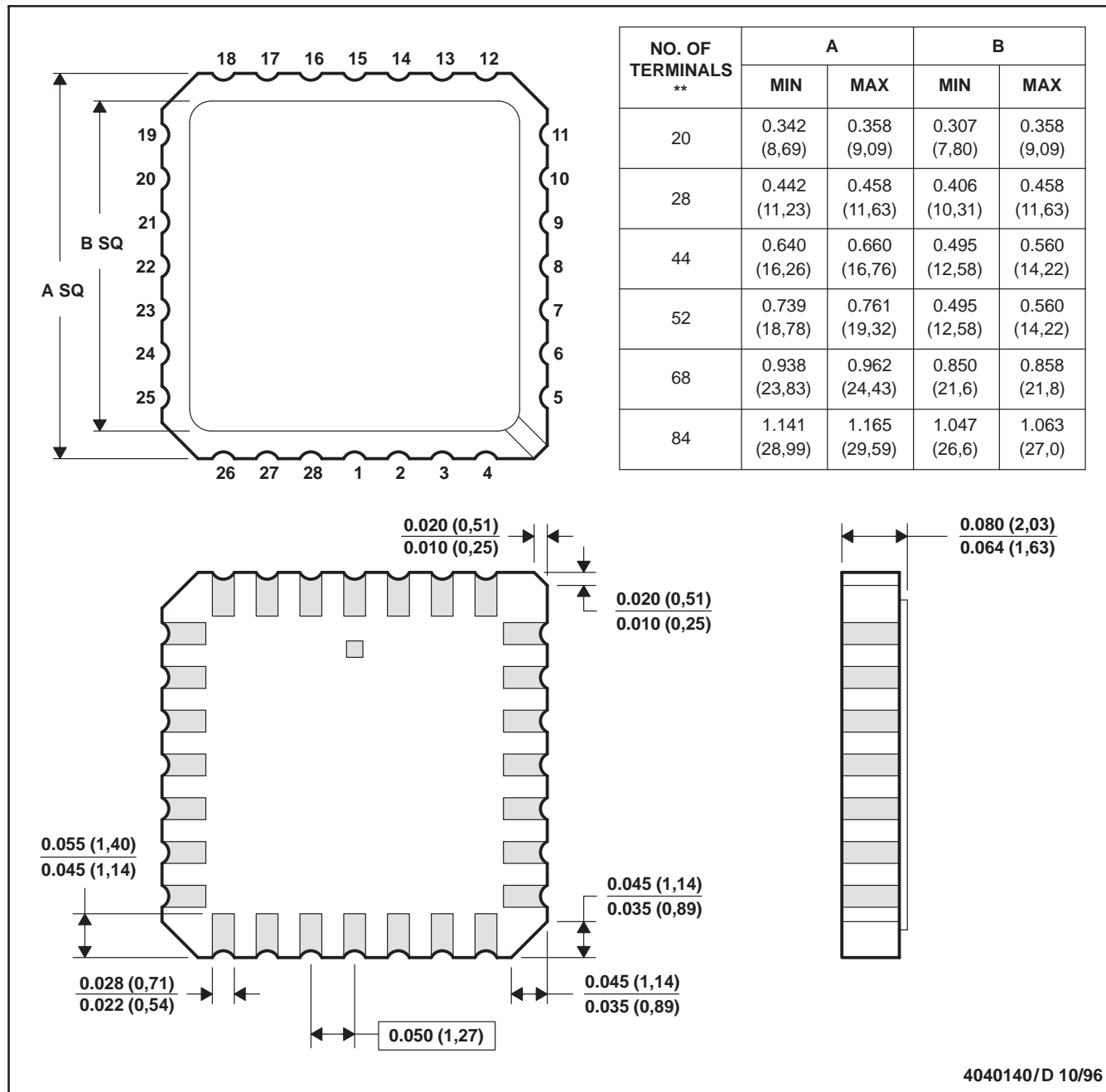
# MECHANICAL DATA

MLCC006B – OCTOBER 1996

FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



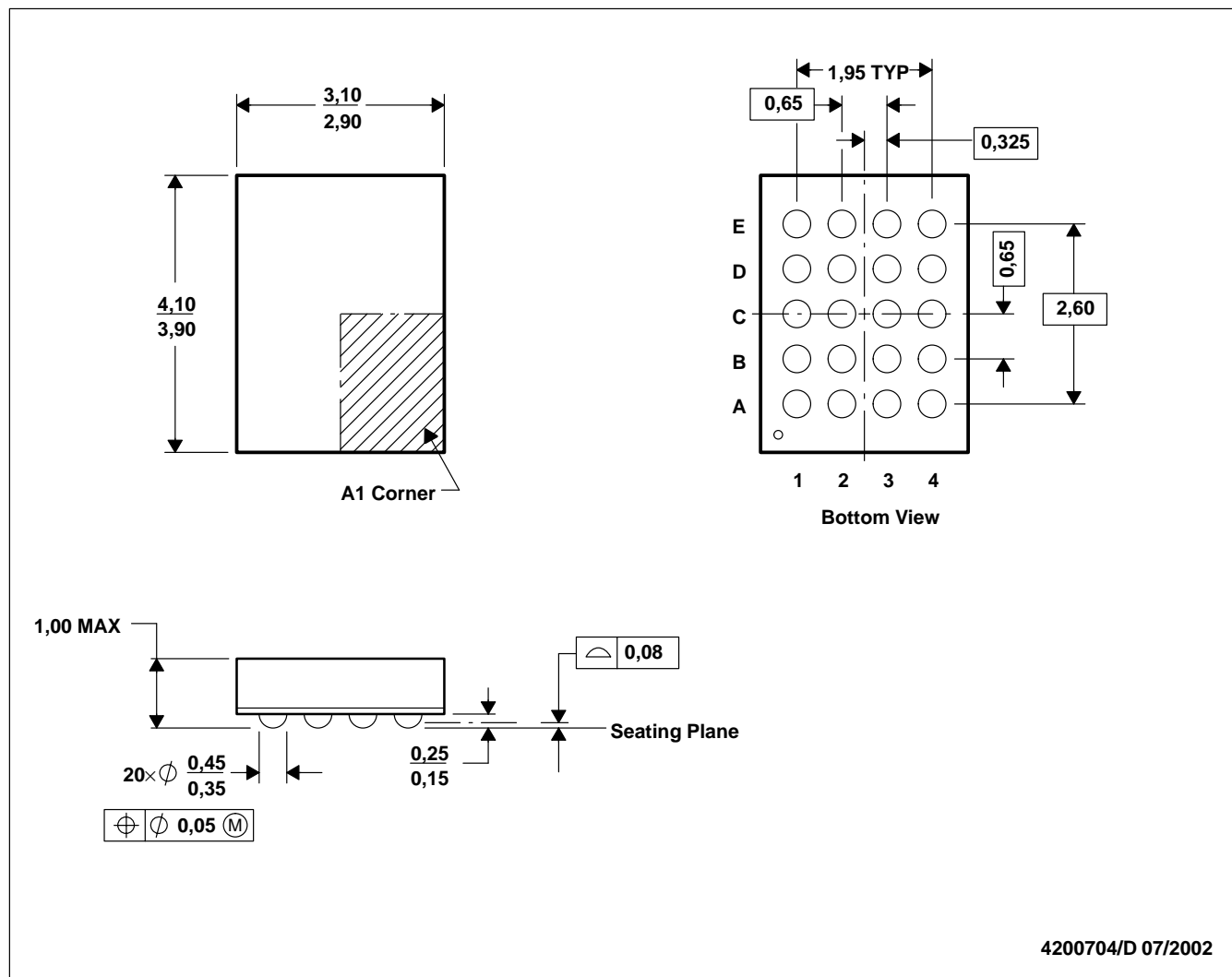
- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - The terminals are gold plated.
  - Falls within JEDEC MS-004

# MECHANICAL DATA

MPBG133C – APRIL 2000 – REVISED AUGUST 2002

GQN (R-PBGA-N20)

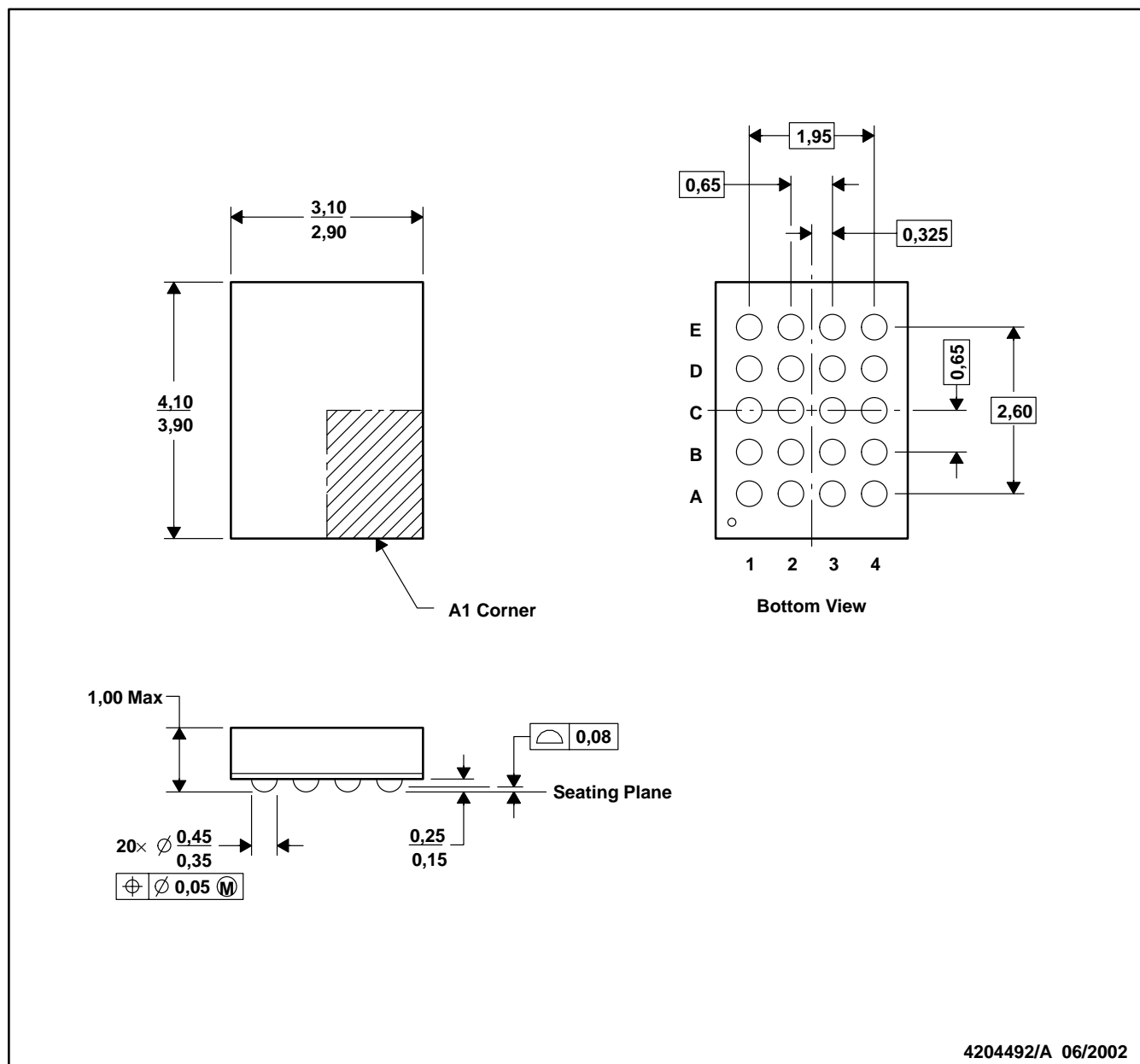
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. MicroStar Junior™ configuration
  - D. Falls within JEDEC MO-225 variation BC.
  - E. This package is tin-lead (SnPb). Refer to the 20 ZQN package (drawing 4204492) for lead-free.

## ZQN (R-PBGA-N20)

## PLASTIC BALL GRID ARRAY

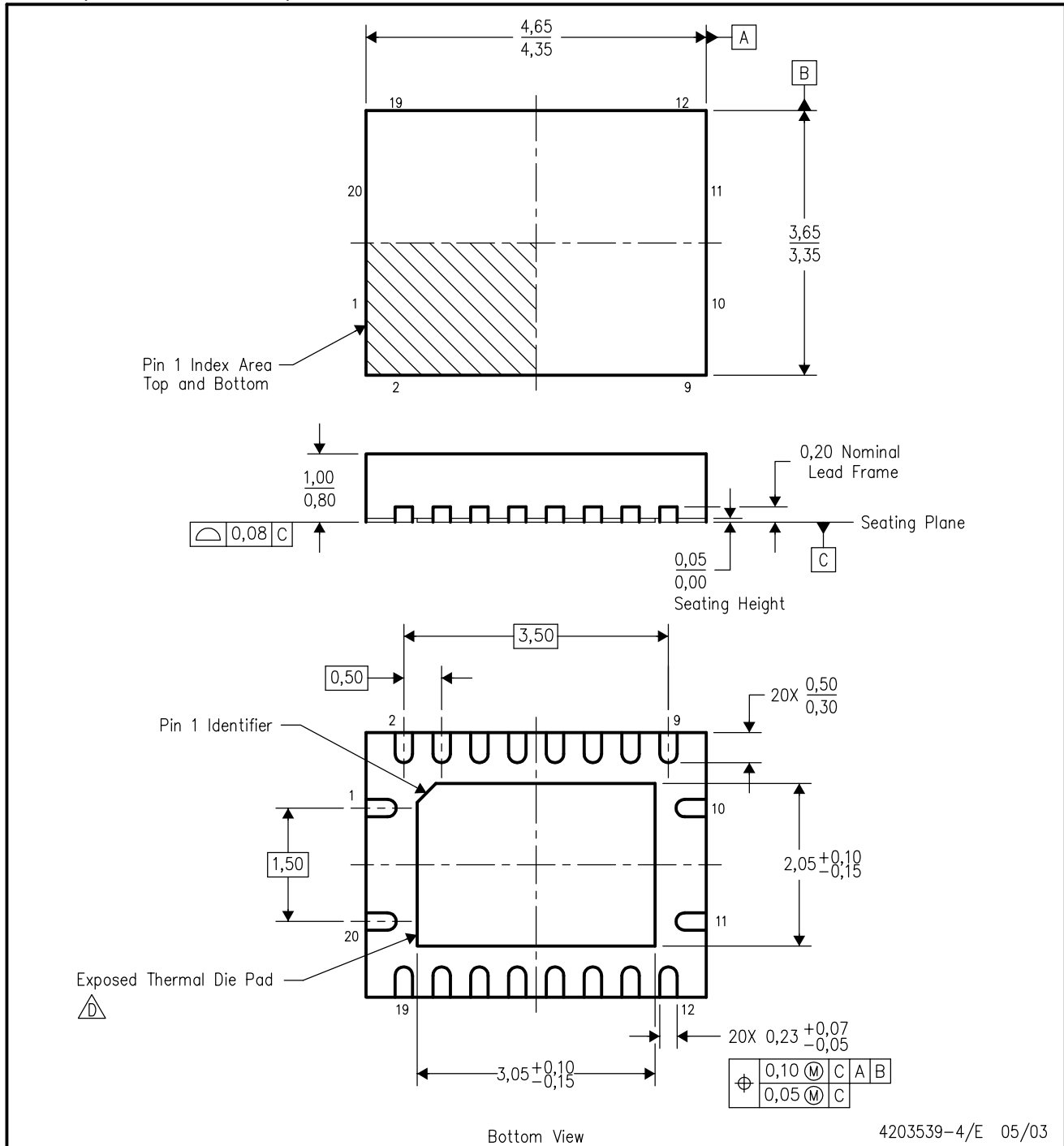


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. MicroStar Junior™ configuration.
  - D. Fall within JEDEC MO-225 variation BC.
  - E. This package is lead-free. Refer to the 20 GQN package (drawing 4200704) for tin-lead (SnPb).

# MECHANICAL DATA

RGY (R-PQFP-N20)

PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected ground leads.
  - E. Package complies to JEDEC MO-241 variation BC.

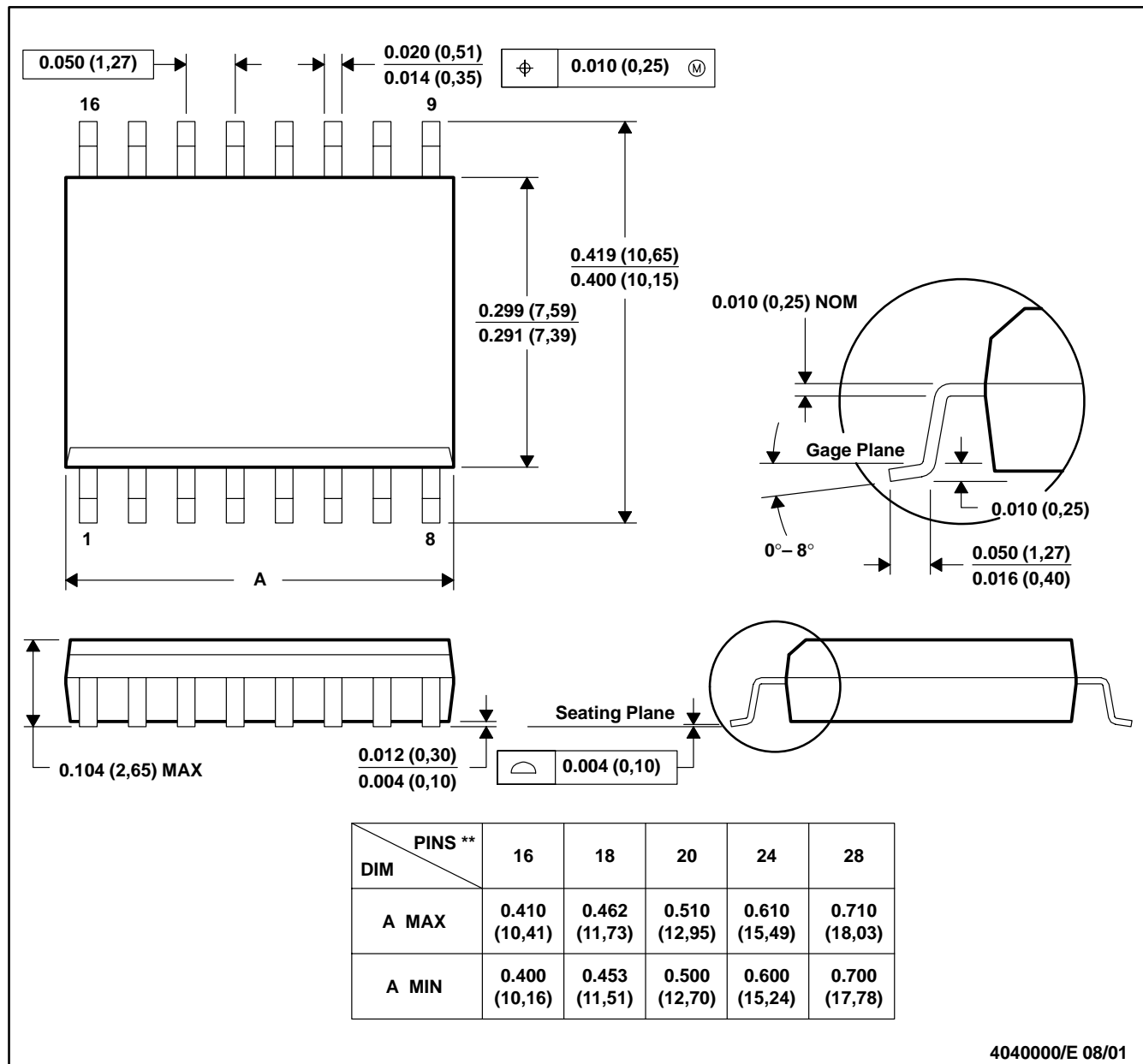
# MECHANICAL DATA

MSOI003E – JANUARY 1995 – REVISED SEPTEMBER 2001

DW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



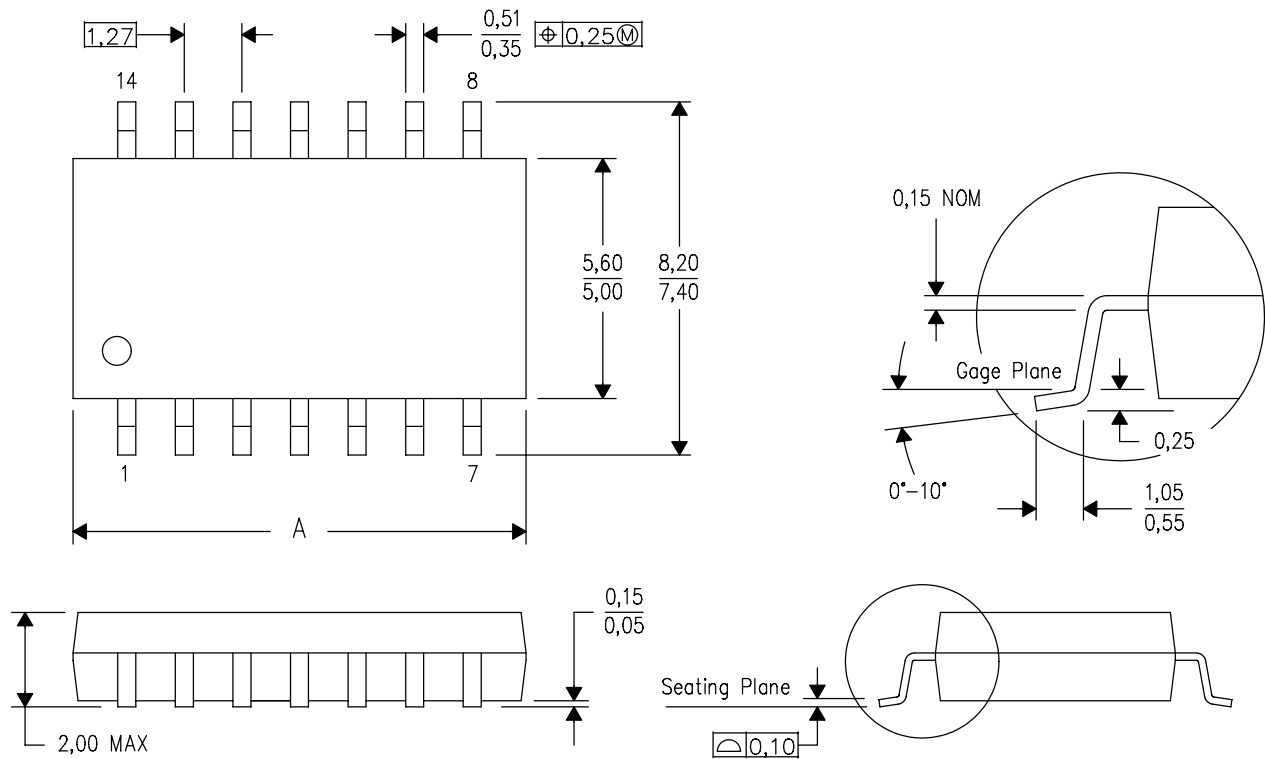
- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MS-013

## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

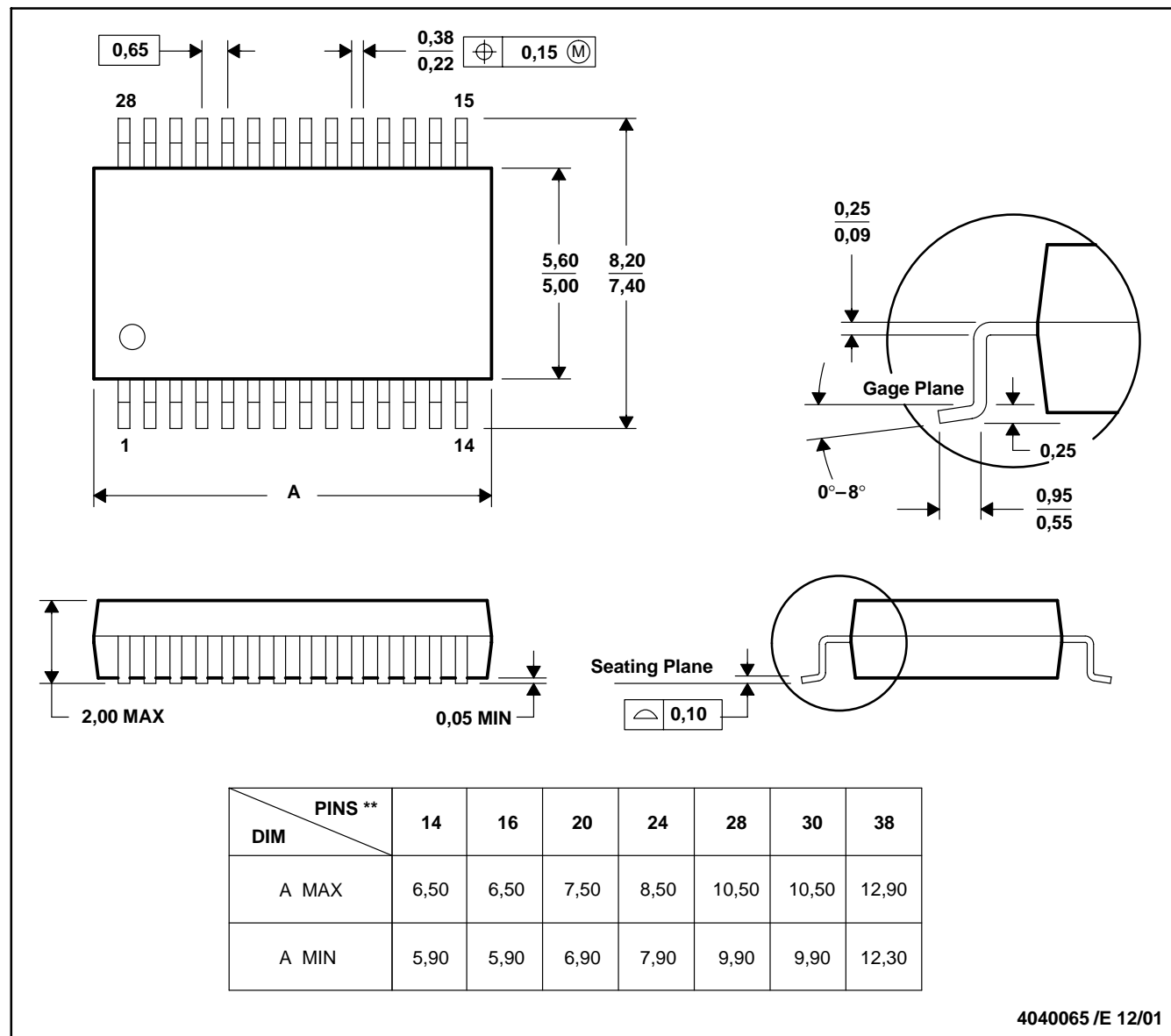
# MECHANICAL DATA

MSS0002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. Falls within JEDEC MO-150



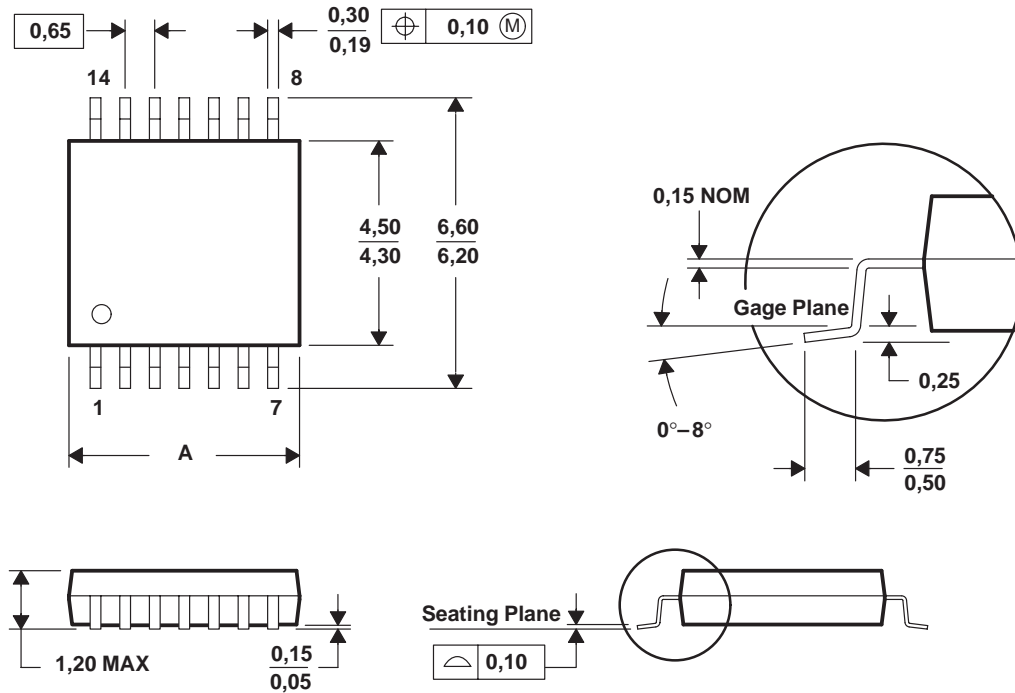
# MECHANICAL DATA

MTSS001C – JANUARY 1995 – REVISED FEBRUARY 1999

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



PINS ** DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
  - D. Falls within JEDEC MO-153

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