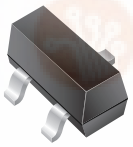
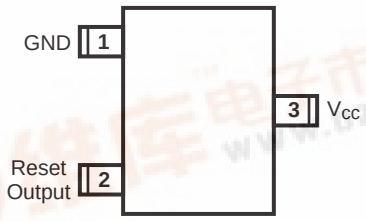
Microprocessor Reset Monitors



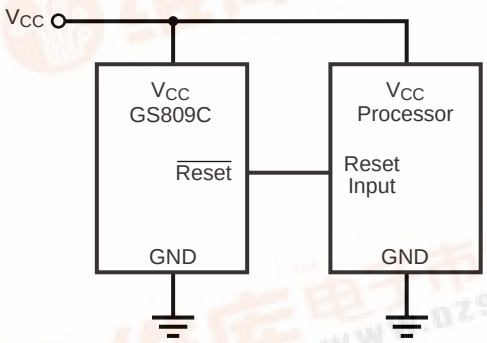
Pin Configuration
SOT-23 (Top View)



Description

- The GS809C and 810C are system supervisor circuits designed to monitor V_{CC} in digital systems and provide a reset signal to the host processor when necessary. No external components are required.
- When the processor power supply voltage drops below the reset threshold, the reset output is driven active, in less than 40µs (T_{D1}). Reset is maintained active for a time period (T_{D2}), after the V_{CC} rises above the threshold voltage.
- To prevent jitter, the reset threshold voltage has a built-in hysteresis of 0.4% of V_{TH}.
- The GS809C has an active-low $\overline{reset}$ output, while the GS810C has an active-high reset output. Both devices have push/pull output drives.
- The reset signal is guaranteed valid, down to V_{CC} = 1.0V.
- Low supply current of 3µA makes these devices well suited for battery powered applications. They are designed to reject fast transients from causing false resets.
- Both devices are available in a space-saving SOT-23 package.

Fig. 1 – Typical Application Diagram



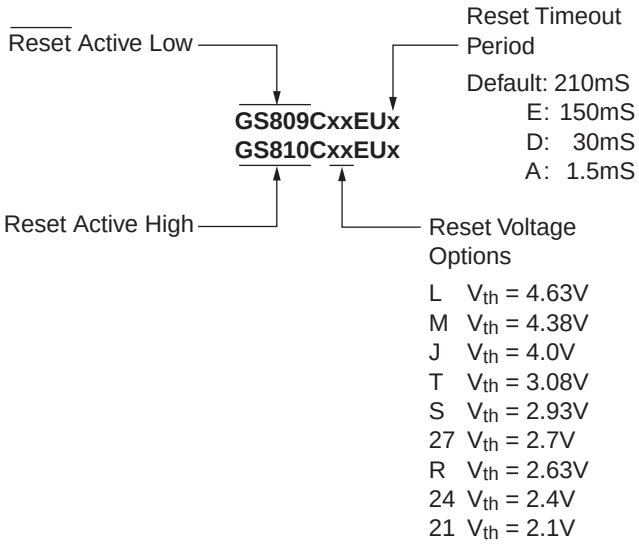
Applications

- Computers
- Battery Powered Equipment
- Critical uProcessor and uController power supply monitoring

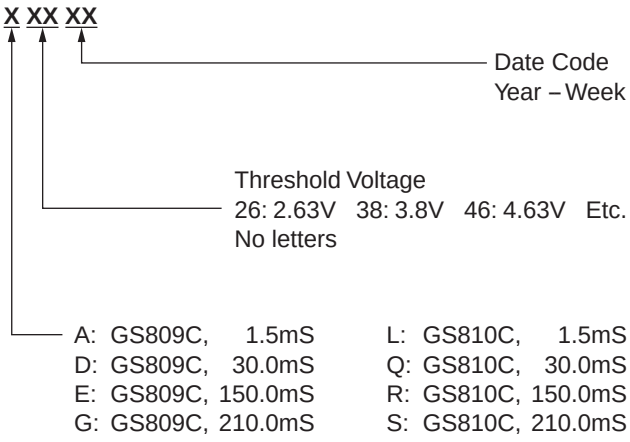
Features

- Tight reset voltage tolerances ± 1.5%
- 4 reset active timeout period options
- Low quiescent current: < 3µA
- 9 reset threshold options from 2.1V to 4.63V
- $\overline{Reset}$ output guaranteed down to 1.0V
- No external components
- V_{CC} Transient immunity
- Wide temperature range –40°C to +85°C

Ordering Information



Marking Information



Absolute Maximum Ratings(1)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	6.0	V
Reset/$\overline{\text{Reset}}$		–0.3 to (V_{CC} + 0.3)	V
Input Current, V_{CC}		20	mA
Output Current, Reset/Reset		20	mA
dV/dT (V_{CC})		100	V/µS
Operating Temperature Range	T_A	–40 to +85	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Power Dissipation ($T_A \leq 70°C$) SOT-23 (Derate 4mW/°C above 70°C)	P_D	260	mW

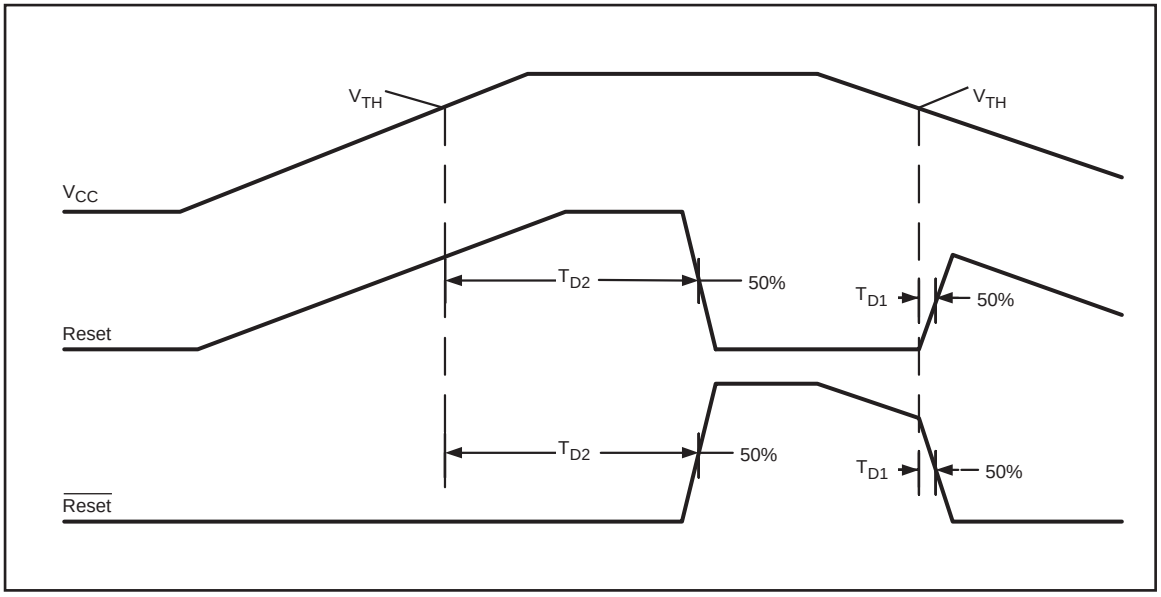
Note: (1) Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.

Electrical Characteristics T_A = 25°C unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{CC} Range	V_{RANGE}		1	–	5.5	V
		T_A = –40 to +85°C	1	–	5.5	
Supply Current	I_{CC}	Vcc = 3.0V	–	–	3.0	µA
		Vcc=3.0V, T_A= –40 to +85°C	–	–	5.0	
Reset Threshold	V_{TH}		V_{THNOM}–1.5%	V_{THNOM}	V_{THNOM}+1.5%	V
		T_A = –40 to +85°C	V_{THNOM}–2.0%	V_{THNOM}	V_{THNOM}+2.0%	
Threshold Hysteresis	$V_{TH\ HIST}$			0.4		%V_{TH}
Reset Threshold Temperature Coefficient			–	30	–	ppm/°C
Reset Output Voltage Low 809C/810C	V_{OL}	809C $V_{cc} < V_{TH\ min}$ 810C $V_{cc} > V_{TH\ max}$ T_A = –40 to +85°C I_{SINK} = 1.2mA	–	–	0.5	V
Reset Output Voltage High 809C/810C	V_{OH}	809C $V_{cc} > V_{TH\ max}$ 810C $V_{cc} < V_{TH\ min}$ T_A = –40 to +85°C I_{SOURCE} = 0.5mA	0.8V_{CC}	–	–	V
V_{CC} to Reset Delay	T_{D1}	$V_{CC} = V_{TH}$ – 100mV T_A = –40 to +85°C	–	40	–	µS
Reset Timeout Period	T_{D2}	T_A = –40 to +85°C	T_{D2NOM}–35%	T_{D2NOM}	T_{D2NOM}+35%	mS

Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

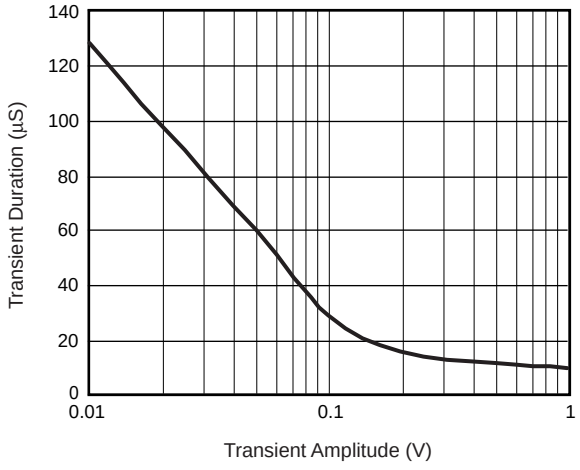
Fig. 2 – Timing Diagram



Supply (VCC) Transients

These devices have a certain immunity to fast negative going transients. The graph titled “Transient Rejection” shows the maximum allowable transient amplitude and duration to avoid triggering an unintended reset. As shown in the graph shorter transients can have larger amplitudes without triggering resets.

Fig. 3 – Transient Rejection



Ratings and Characteristic Curves (T_A = 25°C unless otherwise noted)

Fig. 4 – Reset Time vs. Temperature

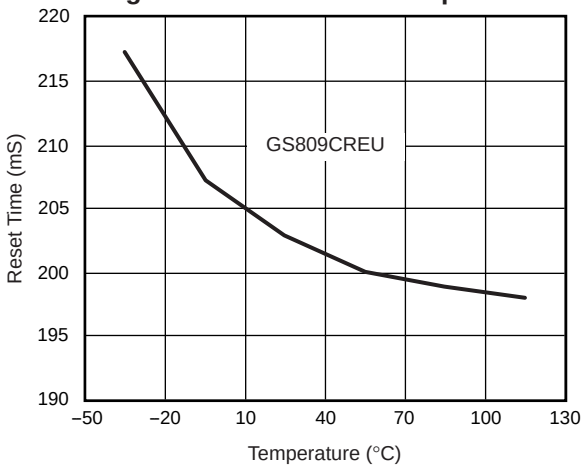


Fig. 5 – I_{CC} vs. Temperature

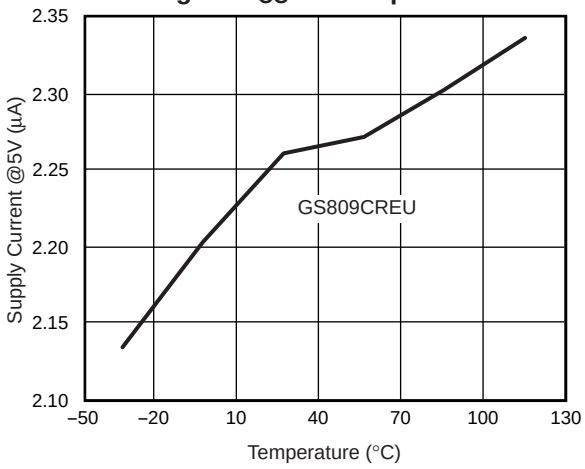


Fig. 6 – Reset V_{th} vs. Temperature

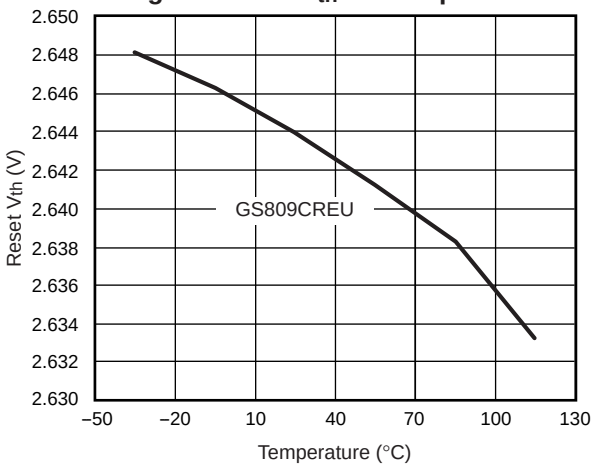


Fig. 7 – I_{CC} vs. V_{CC}

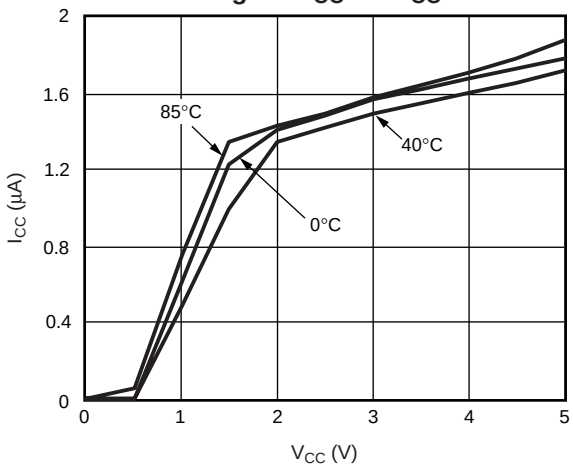
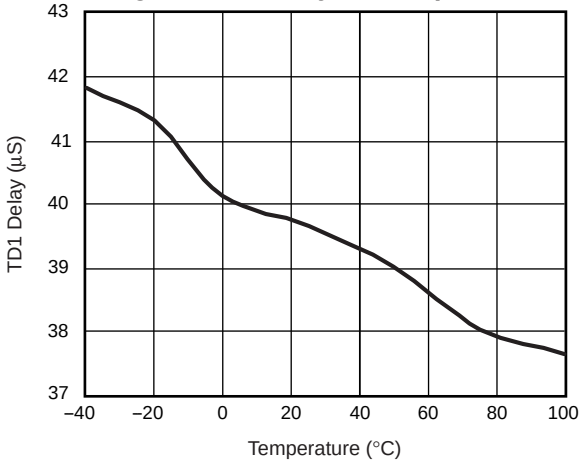


Fig. 8 – TD1 Delay vs. Temperature



Ratings and Characteristic Curves (TA = 25°C unless otherwise noted)

Fig. 9 – Threshold Hysteresis vs. Temperature

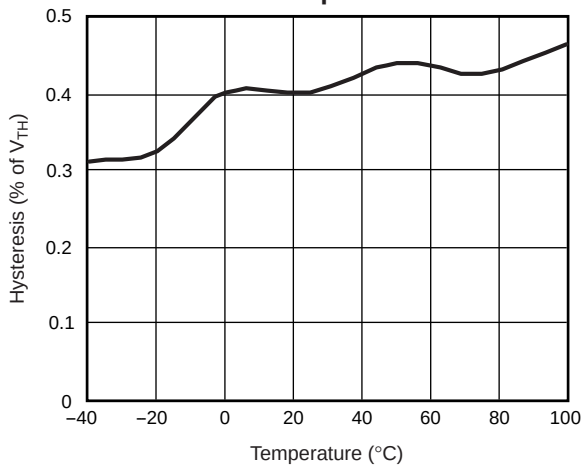
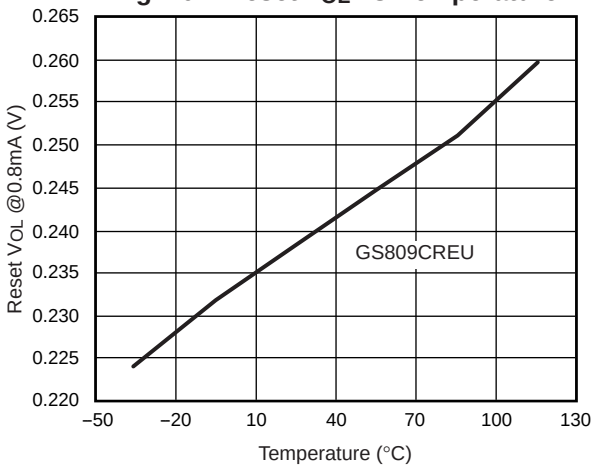


Fig. 10 – Reset V_{OL} vs. Temperature



SOT-23 Case Outline